CY7C1484BV25

# 72-Mbit (2 M × 36) Pipelined DCD Sync SRAM

## Features

- Supports bus operation up to 250 MHz
- Available speed grades are 250 MHz
- Registered inputs and outputs for pipelined operation
- Optimal for performance (double cycle deselect)
- Depth expansion without wait state
- 2.5 V core power supply ($V_{DD}$)
- 2.5 V I/O supply ($V_{DDQ}$)
- Fast clock to output times
  - 3.0 ns (for 250 MHz device)
- Provide high performance 3-1-1-1 access rate
- User selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed writes
- Asynchronous output enable
- CY7C1484BV25 available in JEDEC-standard Pb-free 100-pin TQFP package
- "ZZ" sleep mode option

## Functional Description

The CY7C1484BV25 SRAM integrates 2 M × 36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining Chip Enable ($\overline{CE}_1$), depth expansion Chip Enables ($CE_2$ and $\overline{CE}_3$), Burst Control inputs (ADSC, ADSP, and ADV), Write Enables ($\overline{BW}_X$ and $\overline{BWE}$), and Global Write ($\overline{GW}$). Asynchronous inputs include the Output Enable ($\overline{OE}$) and the ZZ pin.

Addresses and chip enables are registered at the rising edge of clock when either Address Strobe Processor ($\overline{ADSP}$) or Address Strobe Controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the Advance pin (ADV).

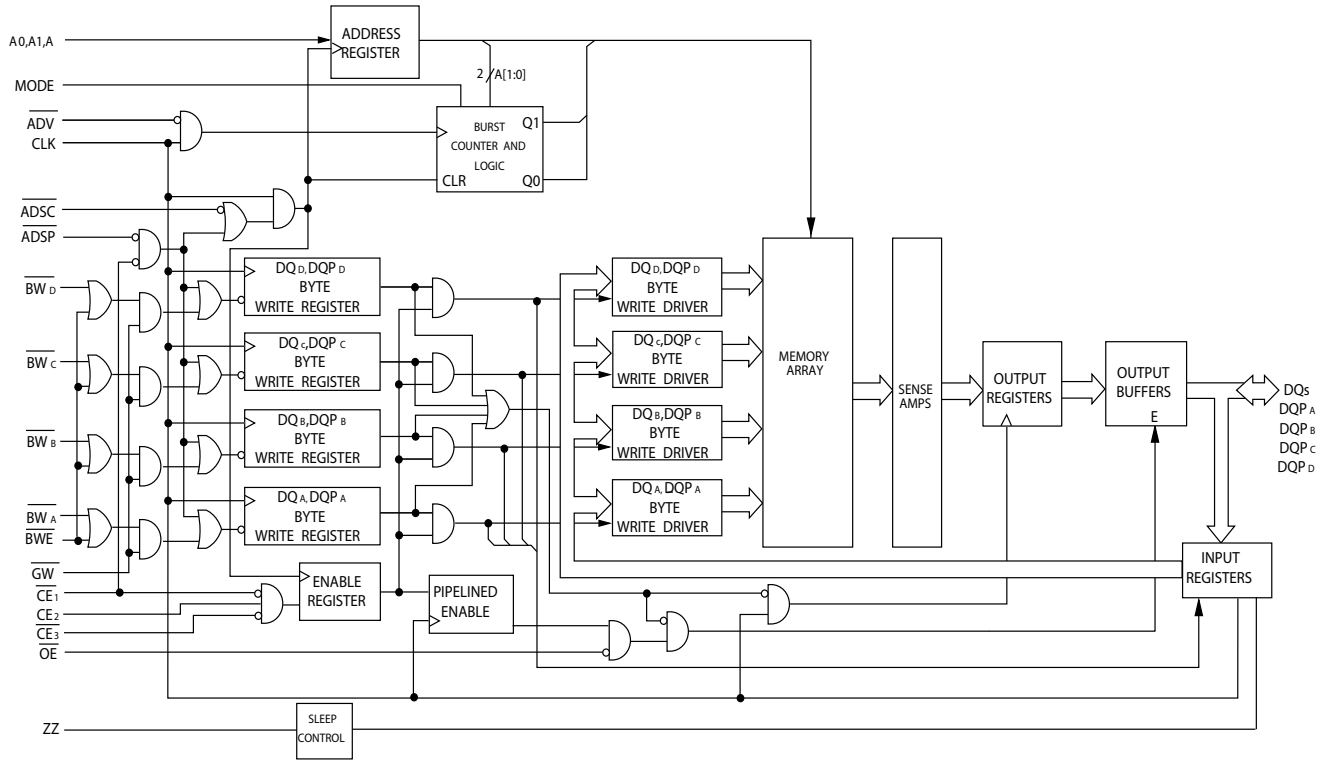
Address, data inputs, and write controls are registered on-chip to initiate a self timed write cycle. This part supports byte write operations (see Pin Definitions on page 5 and Truth Table on page 8 for more information). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. $\overline{GW}$ active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register, which delays turning off the output buffers an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

For a complete list of related documentation, click here.

## Selection Guide

| Description | 250 MHz | Unit |
|---|---|---|
| Maximum Access Time | 3.0 | ns |
| Maximum Operating Current | 450 | mA |
| Maximum CMOS Standby Current | 120 | mA |

## Logic Block Diagram – CY7C1484BV25

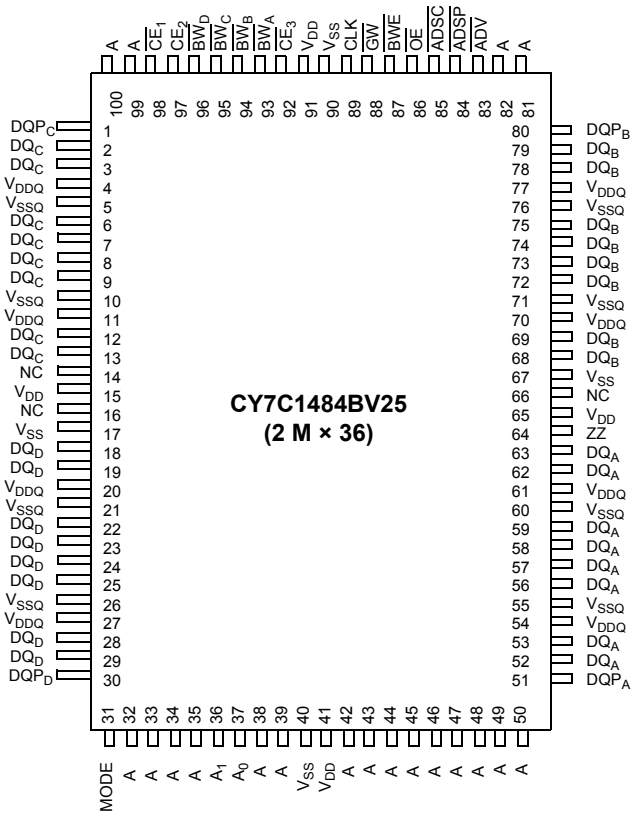


## Contents

**Pin Configurations** ..... **4**
**Pin Definitions** ..... **5**
**Functional Overview** ..... **6**
Single Read Accesses ..... 6
Single Write Accesses Initiated by ADSP ..... 6
Single Write Accesses Initiated by ADSC ..... 6
Burst Sequences ..... 6
Sleep Mode ..... 7
Interleaved Burst Address Table (MODE = Floating or VDD) ..... 7
Linear Burst Address Table (MODE = GND) ..... 7
ZZ Mode Electrical Characteristics ..... 7
**Truth Table** ..... **8**
**Truth Table for Read/Write** ..... **9**
**Maximum Ratings** ..... **10**
**Operating Range** ..... **10**
**Electrical Characteristics** ..... **10**
**Capacitance** ..... **11**
**Thermal Resistance** ..... **11**
**AC Test Loads and Waveforms** ..... **11**
**Switching Characteristics** ..... **12**
**Switching Waveforms** ..... **13**
**Ordering Information** ..... **17**
Ordering Code Definitions ..... 17
**Package Diagrams** ..... **18**
**Acronyms** ..... **19**
**Document Conventions** ..... **19**
Units of Measure ..... 19
**Document History Page** ..... **20**
**Sales, Solutions, and Legal Information** ..... **21**
Worldwide Sales and Design Support ..... 21
Products ..... 21
PSoC® Solutions ..... 21
Cypress Developer Community ..... 21
Technical Support ..... 21

## Pin Configurations

**Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout**



## Pin Definitions

| Pin Name | I/O | Description |
|---|---|---|
| $A_0$, $A_1$, A | Input-Synchronous | **Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, $CE_2$, and $\overline{CE}_3$ are sampled active. A1:A0 are fed to the 2-bit counter. |
| $\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$ | Input-Synchronous | **Byte Write Select Inputs, Active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK. |
| $\overline{GW}$ | Input-Synchronous | **Global Write Enable Input, Active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$). |
| $\overline{BWE}$ | Input-Synchronous | **Byte Write Enable Input, Active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write. |
| CLK | Input-Clock | **Clock Input**. Captures all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW during a burst operation. |
| $\overline{CE}_1$ | Input-Synchronous | **Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded. |
| $CE_2$ | Input-Synchronous | **Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. $CE_2$ is sampled only when a new external address is loaded. |
| $\overline{CE}_3$ | Input-Synchronous | **Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $CE_2$ to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded. |
| $\overline{OE}$ | Input-Asynchronous | **Output Enable, Asynchronous Input, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, DQ pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state. |
| $\overline{ADV}$ | Input-Synchronous | **Advance Input Signal, Sampled on the Rising Edge of CLK, Active LOW**. When asserted, it automatically increments the address in a burst cycle. |
| $\overline{ADSP}$ | Input-Synchronous | **Address Strobe from Processor, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH. |
| $\overline{ADSC}$ | Input-Synchronous | **Address Strobe from Controller, Sampled on the Rising Edge of CLK, Active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. |
| ZZ | Input-Asynchronous | **ZZ "Sleep" Input, Active HIGH**. When asserted HIGH, places the device in a non time-critical "sleep" condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down. |
| DQs, DQPs | I/O-Synchronous | **Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and $DQP_X$ are placed in a tri-state condition. |
| $V_{DD}$ | Power Supply | **Power Supply Inputs to the Core of the Device**. |
| $V_{SS}$ | Ground | **Ground for the Core of the Device**. |
| $V_{SSQ}$[1] | I/O Ground | **Ground for the I/O Circuitry**. |
| $V_{DDQ}$ | I/O Power Supply | **Power Supply for the I/O Circuitry**. |

**Note**
1. Applicable for TQFP package.

## Pin Definitions (continued)

| Pin Name | I/O | Description |
|---|---|---|
| MODE | Input-Static | **Selects Burst Order**. When tied to GND, selects linear burst sequence. When tied to $V_{DD}$ or left floating, selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode Pin has an internal pull up. |
| NC | – | **No Connects**. Not internally connected to the die |
| NC(144M, 288M, 576M, 1G) | – | **These Pins are Not Connected**. They are used for expansion to the 144M, 288M, 576M, and 1G densities. |

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1484BV25 supports secondary cache in systems using either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable and is determined by sampling the MODE input. Accesses are initiated with either the $\overline{ADSP}$ or $\overline{ADSC}$. The $\overline{ADV}$ input controls address advancement through the burst sequence. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW_X}$) inputs. $\overline{GW}$ overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Synchronous Chip Selects $\overline{CE_1}$, $CE_2$, $\overline{CE_3}$ and an asynchronous Output Enable ($\overline{OE}$) provide easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH. The address presented to the address inputs is stored into the address advancement logic and the address register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within $t_{CO}$ if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state; its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the $\overline{OE}$ signal controls the outputs. Consecutive single read cycles are supported.

The CY7C1484BV25 is a double cycle deselect part. After the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output tri-states immediately after the next clock rise.

### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the $DQ_X$ inputs is written into the corresponding address location in the memory core. If $\overline{GW}$ is HIGH, then the $\overline{BWE}$ and $\overline{BW_X}$ signals control the write operation. The CY7C1484BV25 provides byte write capability that is described in the Truth Table for Read/Write on page 9. Asserting $\overline{BWE}$ with the selected Byte Write input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations.

Because the CY7C1484BV25 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ inputs. Doing so tri-states the output drivers. As a safety precaution, DQ are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

### Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the $DQ_X$ is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations.

Because the CY7C1484BV25 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the $DQ_X$ inputs. Doing so tri-states the output drivers. As a safety precaution, $DQ_X$ are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

### Burst Sequences

The CY7C1484BV25 provides a 2-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed

specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input. Both read and write burst operations are supported.

Asserting $\overline{ADV}$ LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

### Sleep Mode

The ZZ input pin is asynchronous. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. CEs, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

### Interleaved Burst Address Table (MODE = Floating or $V_{DD}$)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

### Linear Burst Address Table (MODE = GND)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

### ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | ZZ $\geq V_{DD} - 0.2$ V | – | 120 | mA |
| $t_{ZZS}$ | Device operation to ZZ | ZZ $\geq V_{DD} - 0.2$ V | – | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | ZZ $\leq$ 0.2 V | $2t_{CYC}$ | – | ns |
| $t_{ZZI}$ | ZZ Active to sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ Inactive to exit sleep current | This parameter is sampled | 0 | – | ns |

## Truth Table

The truth table for CY7C1484BV25 follows. [2, 3, 4, 5, 6]

| Operation | Address Used | $\overline{CE_1}$ | $CE_2$ | $\overline{CE_3}$ | ZZ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | $\overline{OE}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselect Cycle, Power Down | None | H | X | X | L | X | L | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | L | X | L | L | X | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | X | H | L | L | X | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | L | X | L | H | L | X | X | X | L–H | Tri-State |
| Deselect Cycle, Power Down | None | L | X | H | L | H | L | X | X | X | L–H | Tri-State |
| Sleep Mode, Power Down | None | X | X | X | H | X | X | X | X | X | X | Tri-State |
| Read Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | L | L–H | Q |
| Read Cycle, Begin Burst | External | L | H | L | L | L | X | X | X | H | L–H | Tri-State |
| Write Cycle, Begin Burst | External | L | H | L | L | H | L | X | L | X | L–H | D |
| Read Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | L | L–H | Q |
| Read Cycle, Begin Burst | External | L | H | L | L | H | L | X | H | H | L–H | Tri-State |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L–H | Q |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L–H | Tri-State |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L–H | Q |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L–H | Tri-State |
| Write Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L–H | D |
| Write Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L–H | D |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L–H | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L–H | Tri-State |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L–H | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L–H | Tri-State |
| Write Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L–H | D |
| Write Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L–H | D |

**Notes**
2. X = Don't Care, H = Logic HIGH, L = Logic LOW.
3. $\overline{WRITE}$ = L when any one or more Byte Write Enable signals and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all Byte Write Enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
4. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the ADSP or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

## Truth Table for Read/Write

The read/write truth table for CY7C1484BV25 follows. [7, 8]

| Function | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW_D}$ | $\overline{BW_C}$ | $\overline{BW_B}$ | $\overline{BW_A}$ |
|---|---|---|---|---|---|---|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write Byte A – ($DQ_A$ and $DQP_A$) | H | L | H | H | H | L |
| Write Byte B – ($DQ_B$ and $DQP_B$) | H | L | H | H | L | H |
| Write Bytes B, A | H | L | H | H | L | L |
| Write Byte C – ($DQ_C$ and $DQP_C$) | H | L | H | L | H | H |
| Write Bytes C, A | H | L | H | L | H | L |
| Write Bytes C, B | H | L | H | L | L | H |
| Write Bytes C, B, A | H | L | H | L | L | L |
| Write Byte D – ($DQ_D$ and $DQP_D$) | H | L | L | H | H | H |
| Write Bytes D, A | H | L | L | H | H | L |
| Write Bytes D, B | H | L | L | H | L | H |
| Write Bytes D, B, A | H | L | L | H | L | L |
| Write Bytes D, C | H | L | L | L | H | H |
| Write Bytes D, C, A | H | L | L | L | H | L |
| Write Bytes D, C, B | H | L | L | L | L | H |
| Write All Bytes | H | L | L | L | L | L |
| Write All Bytes | L | X | X | X | X | X |

**Notes**
7. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
8. Table includes only a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write is based on which byte write is active.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on $V_{DD}$ Relative to GND .....–0.5 V to +3.6 V

Supply Voltage on $V_{DDQ}$ Relative to GND .... –0.5 V to +$V_{DD}$

DC Voltage Applied to Outputs in Tri-State .....–0.5 V to $V_{DDQ}$ + 0.5 V

DC Input Voltage .....–0.5 V to $V_{DD}$ + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0 °C to +70 °C | 2.5 V – 5% / + 5% | 2.5 V – 5% to $V_{DD}$ |
| Industrial | –40 °C to +85 °C | | |

## Electrical Characteristics

Over the Operating Range

| Parameter [9, 10] | Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | | 2.375 | 2.625 | V |
| $V_{DDQ}$ | I/O Supply Voltage | For 2.5 V I/O | | 2.375 | $V_{DD}$ | V |
| $V_{OH}$ | Output HIGH Voltage | For 2.5 V I/O, $I_{OH}$ = –1.0 mA | | 2.0 | – | V |
| $V_{OL}$ | Output LOW Voltage | For 2.5 V I/O, $I_{OL}$ = 1.0 mA | | – | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage [9] | For 2.5 V I/O | | 1.7 | $V_{DD}$ + 0.3 V | V |
| $V_{IL}$ | Input LOW Voltage [9] | For 2.5 V I/O | | –0.3 | 0.7 | V |
| $I_X$ | Input Leakage Current except ZZ and MODE | GND ≤ $V_I$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |
| | Input Current of MODE | Input = $V_{SS}$ | | –30 | – | µA |
| | | Input = $V_{DD}$ | | – | 5 | µA |
| | Input Current of ZZ | Input = $V_{SS}$ | | –5 | – | µA |
| | | Input = $V_{DD}$ | | – | 30 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{DDQ}$, Output Disabled | | –5 | 5 | µA |
| $I_{DD}$ [11] | $V_{DD}$ Operating Supply Current | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = 1/$t_{CYC}$ | 4.0 ns cycle, 250 MHz | – | 450 | mA |
| $I_{SB1}$ | Automatic CE Power Down Current—TTL Inputs | $V_{DD}$ = Max, Device Deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ = 1/$t_{CYC}$ | 4.0 ns cycle, 250 MHz | – | 200 | mA |
| $I_{SB2}$ | Automatic CE Power Down Current—CMOS Inputs | $V_{DD}$ = Max, Device Deselected, $V_{IN}$ ≤ 0.3 V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3 V, f = 0 | 4.0 ns cycle, 250 MHz | – | 120 | mA |
| $I_{SB3}$ | Automatic CE Power Down Current—CMOS Inputs | $V_{DD}$ = Max, Device Deselected, $V_{IN}$ ≤ 0.3 V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3 V, f = $f_{MAX}$ = 1/$t_{CYC}$ | 4.0 ns cycle, 250 MHz | – | 200 | mA |
| $I_{SB4}$ | Automatic CE Power Down Current—TTL Inputs | $V_{DD}$ = Max, Device Deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = 0 | 4.0 ns cycle, 250 MHz | – | 135 | mA |

**Notes**

9. Overshoot: $V_{IH(AC)}$ < $V_{DD}$ + 1.5 V (pulse width less than $t_{CYC}$/2). Undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than $t_{CYC}$/2).
10. Power up: assumes a linear ramp from 0 V to $V_{DD(minimum)}$ within 200 ms. During this time $V_{IH}$ < $V_{DD}$ and $V_{DDQ}$ ≤ $V_{DD}$.
11. The operation current is calculated with 50% read cycle and 50% write cycle.

## Capacitance

| Parameter [12] | Description | Test Conditions | 100-pin TQFP Package | Unit |
|---|---|---|---|---|
| $C_{ADDRESS}$ | Address Input Capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{DD}$ = 2.5 V, $V_{DDQ}$ = 2.5 V | 6 | pF |
| $C_{DATA}$ | Data Input Capacitance | | 5 | pF |
| $C_{CTRL}$ | Control Input Capacitance | | 8 | pF |
| $C_{CLK}$ | Clock Input Capacitance | | 6 | pF |
| $C_{IO}$ | Input/Output Capacitance | | 5 | pF |

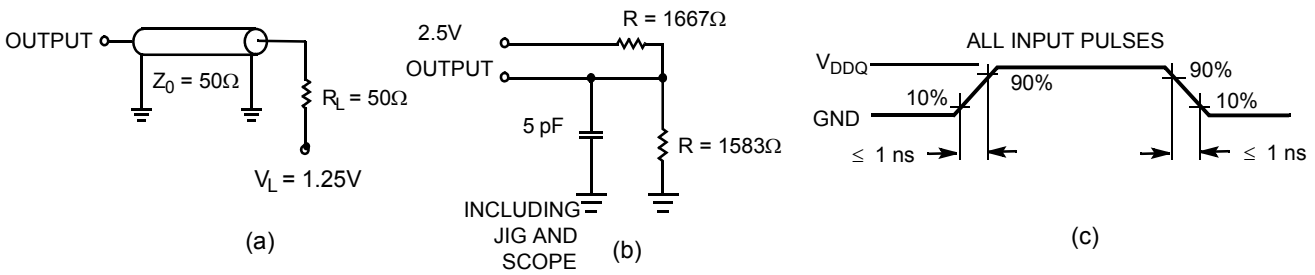
## Thermal Resistance

| Parameter [12] | Description | Test Conditions | 100-pin TQFP Package | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 24.63 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 2.28 | °C/W |

## AC Test Loads and Waveforms

**Figure 2. AC Test Loads and Waveforms**

**2.5 V I/O Test Load**




**Note**
12. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range

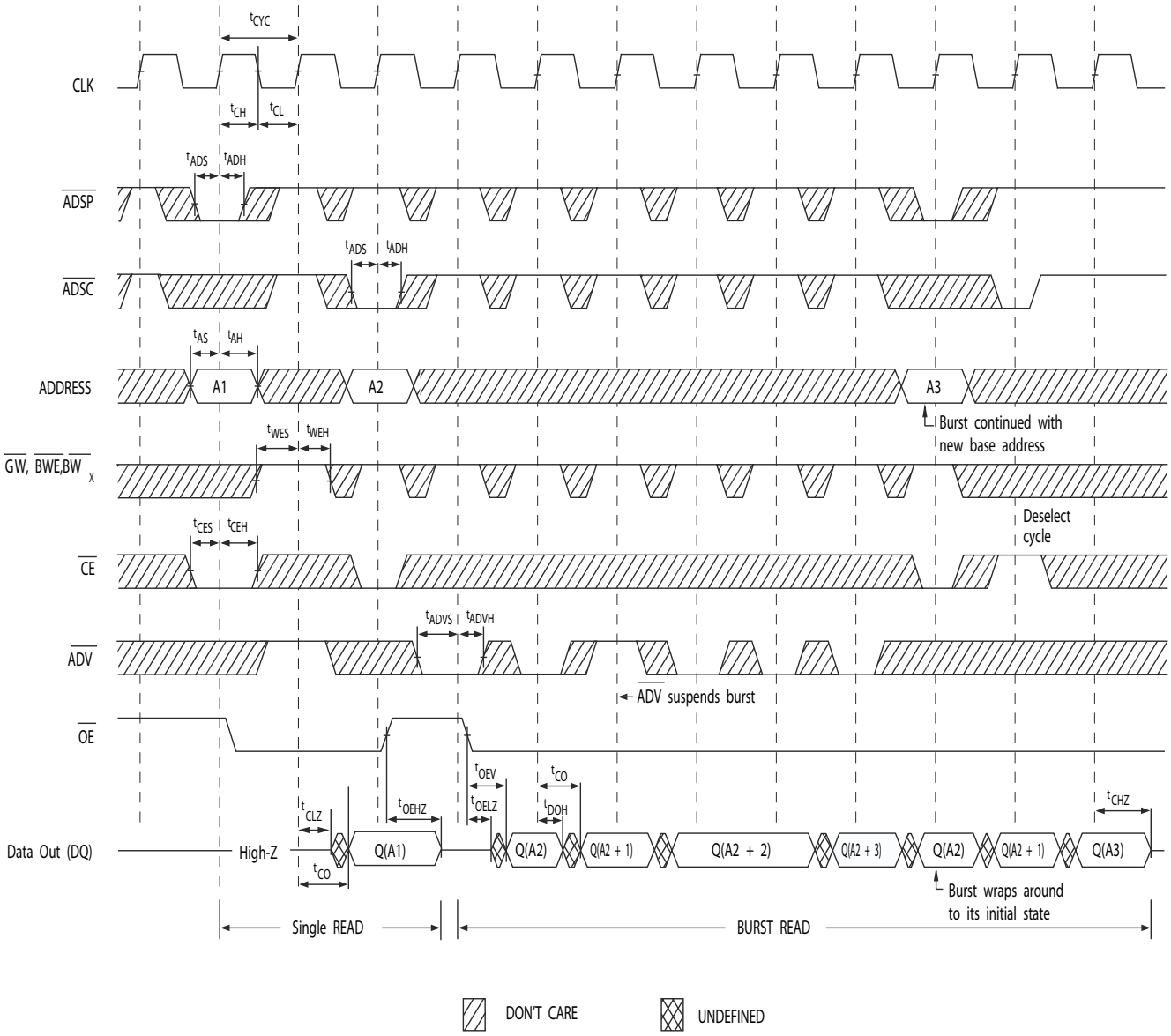
| Parameter [13, 14] | Description | 250 MHz | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{POWER}$ | $V_{DD}$(typical) to the First Access [15] | 1 | – | ms |
| **Clock** | | | | |
| $t_{CYC}$ | Clock Cycle Time | 4.0 | – | ns |
| $t_{CH}$ | Clock HIGH | 2.0 | – | ns |
| $t_{CL}$ | Clock LOW | 2.0 | – | ns |
| **Output Times** | | | | |
| $t_{CO}$ | Data Output Valid After CLK Rise | – | 3.0 | ns |
| $t_{DOH}$ | Data Output Hold After CLK Rise | 1.3 | – | ns |
| $t_{CLZ}$ | Clock to Low Z [16, 17, 18] | 1.3 | – | ns |
| $t_{CHZ}$ | Clock to High Z [16, 17, 18] | – | 3.0 | ns |
| $t_{OEV}$ | $\overline{OE}$ LOW to Output Valid | – | 3.0 | ns |
| $t_{OELZ}$ | $\overline{OE}$ LOW to Output Low Z [16, 17, 18] | 0 | – | ns |
| $t_{OEHZ}$ | $\overline{OE}$ HIGH to Output High Z [16, 17, 18] | – | 3.0 | ns |
| **Setup Times** | | | | |
| $t_{AS}$ | Address Setup Before CLK Rise | 1.4 | – | ns |
| $t_{ADS}$ | $\overline{ADSC}$, $\overline{ADSP}$ Setup Before CLK Rise | 1.4 | – | ns |
| $t_{ADVS}$ | $\overline{ADV}$ Setup Before CLK Rise | 1.4 | – | ns |
| $t_{WES}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Setup Before CLK Rise | 1.4 | – | ns |
| $t_{DS}$ | Data Input Setup Before CLK Rise | 1.4 | – | ns |
| $t_{CES}$ | Chip Enable Setup Before CLK Rise | 1.4 | – | ns |
| **Hold Times** | | | | |
| $t_{AH}$ | Address Hold After CLK Rise | 0.4 | – | ns |
| $t_{ADH}$ | $\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise | 0.4 | – | ns |
| $t_{ADVH}$ | $\overline{ADV}$ Hold After CLK Rise | 0.4 | – | ns |
| $t_{WEH}$ | $\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ Hold After CLK Rise | 0.4 | – | ns |
| $t_{DH}$ | Data Input Hold After CLK Rise | 0.4 | – | ns |
| $t_{CEH}$ | Chip Enable Hold After CLK Rise | 0.4 | – | ns |

**Notes**

13. Timing reference level is 1.25 V when $V_{DDQ}$ = 2.5 V.
14. Test conditions shown in (a) of Figure 2 on page 11 unless otherwise noted.
15. This part has an internal voltage regulator; $t_{POWER}$ is the time that the power is supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
16. $t_{CHZ}$, $t_{CLZ}$,$t_{OELZ}$, and $t_{OEHZ}$ are specified with AC test conditions shown in part (b) of Figure 2 on page 11. Transition is measured ±200 mV from steady-state voltage.
17. At any supplied voltage and temperature, $t_{OEHZ}$ is less than $t_{OELZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z before Low Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

## Switching Waveforms

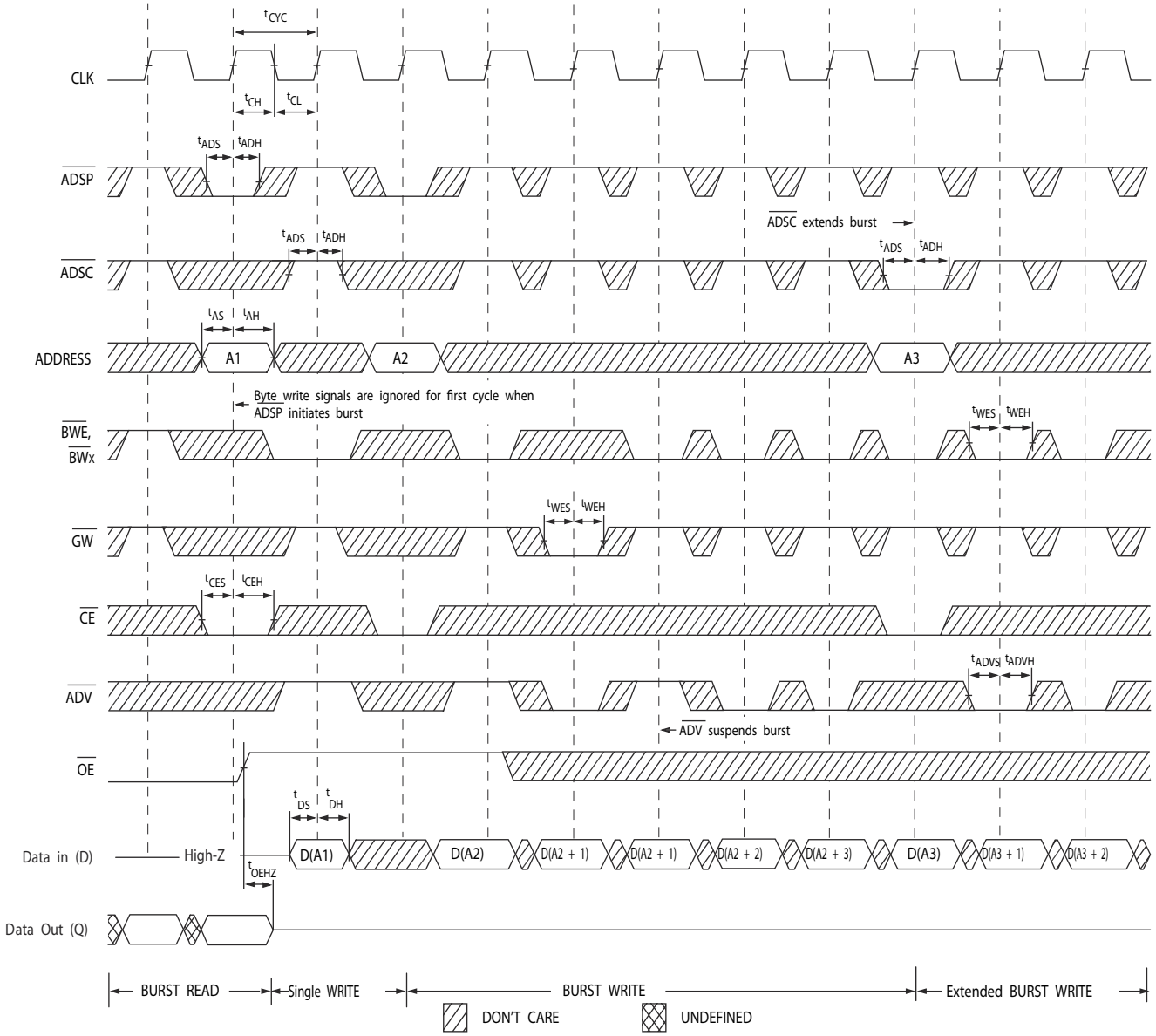
**Figure 3. Read Cycle Timing** [19]




**Note**
19. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, $CE_2$ is LOW, or $\overline{CE}_3$ is HIGH.

## Switching Waveforms (continued)

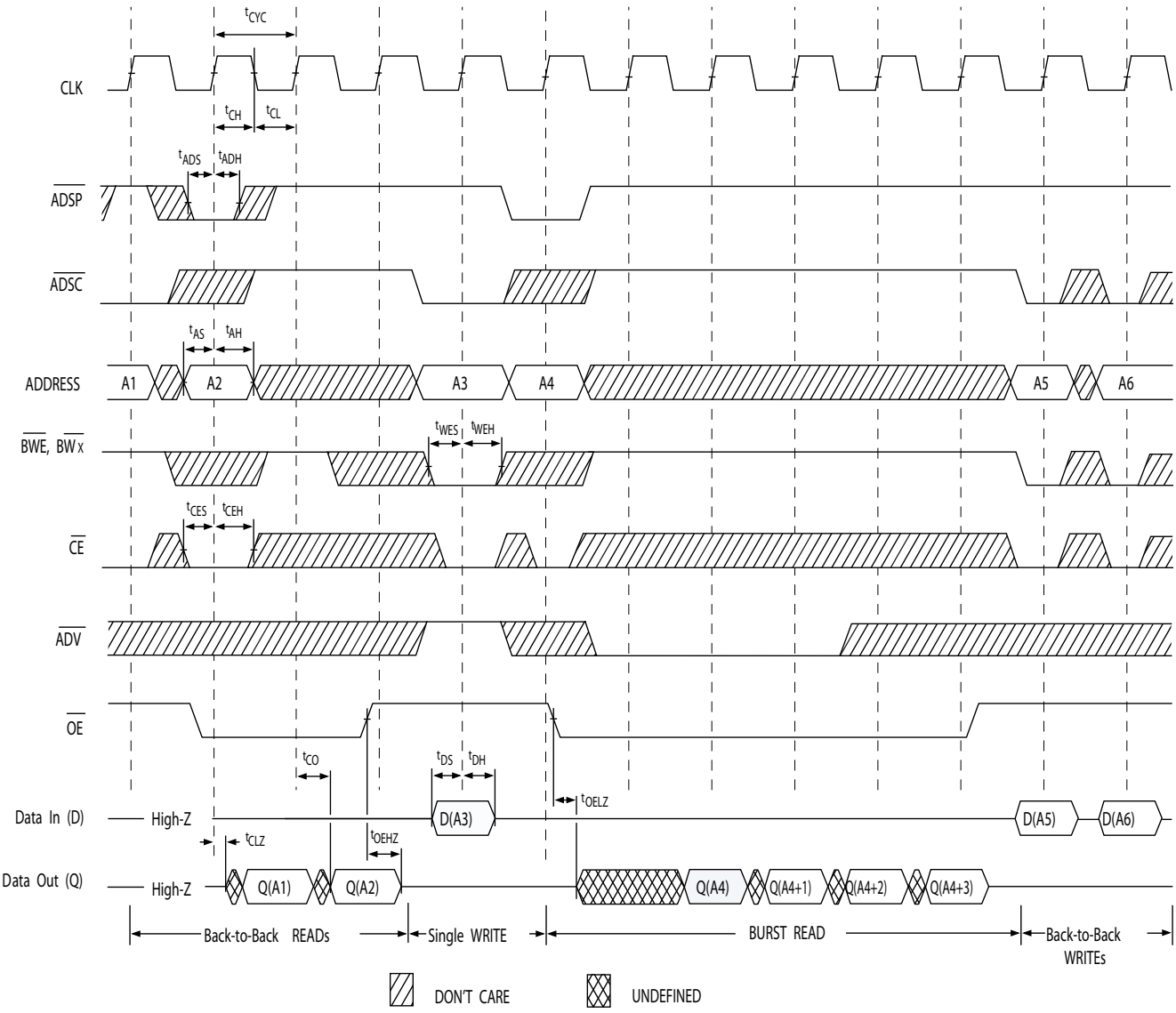
**Figure 4. Write Cycle Timing** [20, 21]




**Notes**
20. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, $CE_2$ is LOW, or $\overline{CE}_3$ is HIGH.
21. Full width write is initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW, and $\overline{BW}_X$ LOW.

## Switching Waveforms (continued)

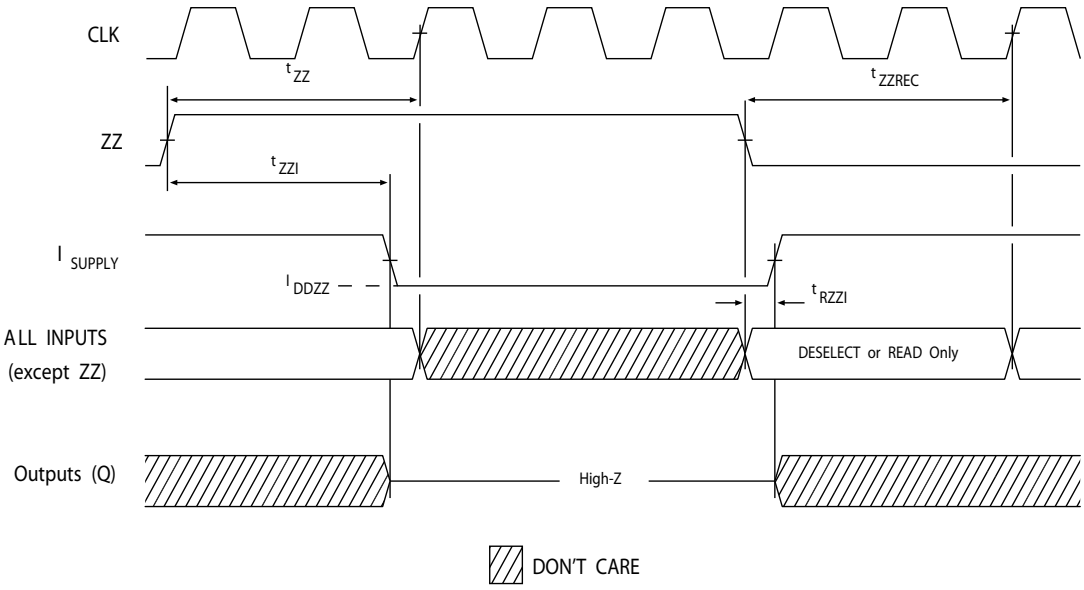
**Figure 5. Read/Write Cycle Timing** [22, 23, 24]




**Notes**
22. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, $CE_2$ is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH, $CE_2$ is LOW, or $\overline{CE}_3$ is HIGH.
23. The data bus (Q) remains in High Z following a write cycle unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
24. $\overline{GW}$ is HIGH.

## Switching Waveforms (continued)

**Figure 6. ZZ Mode Timing** [25, 26]



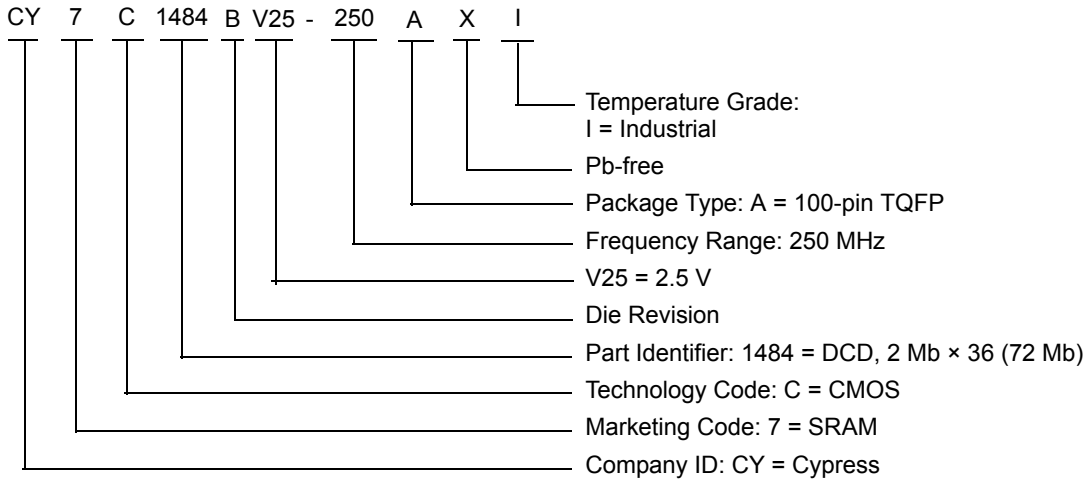

**Notes**
25. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
26. DQs are in High Z when exiting ZZ sleep mode.

## Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

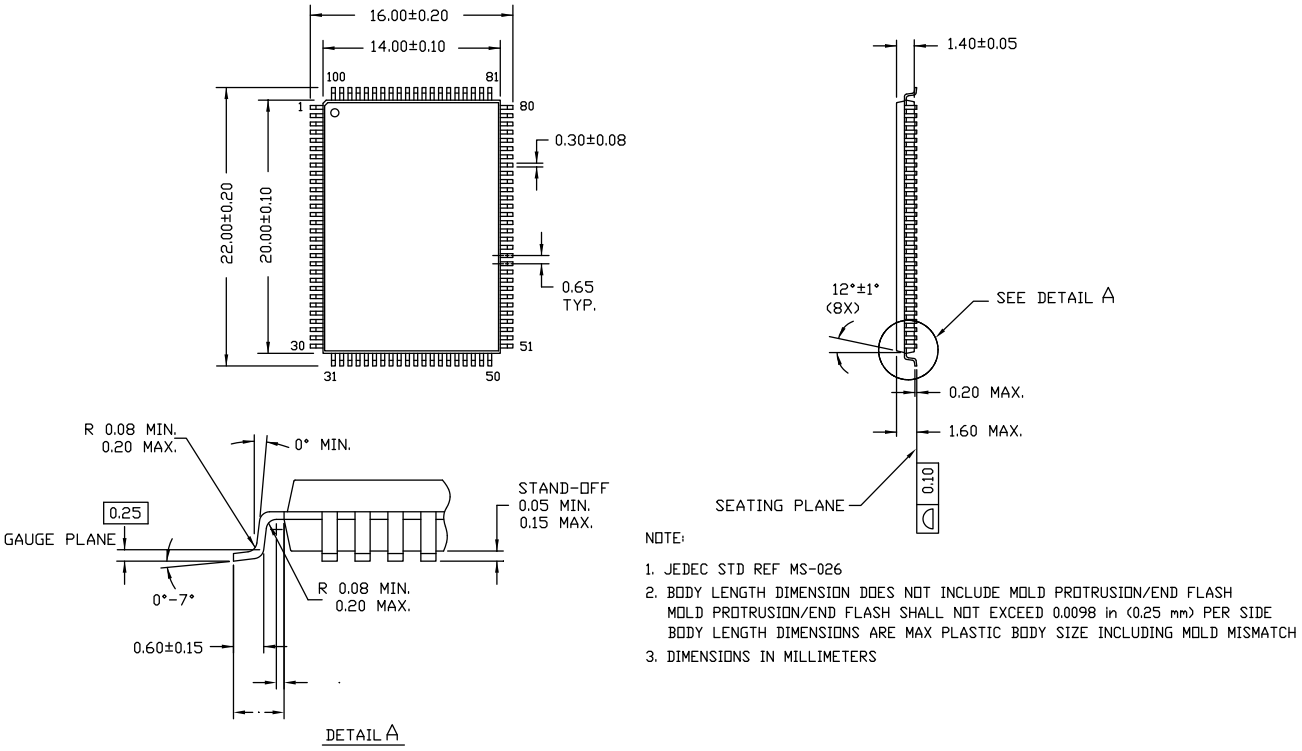
| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|---|---|---|---|---|
| 250 | CY7C1484BV25-250AXI | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Industrial |

### Ordering Code Definitions



## Package Diagrams

**Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050**




NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 *E

## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| EIA | Electronic Industries Alliance |
| I/O | Input/Output |
| JEDEC | Joint Electron Devices Engineering Council |
| $\overline{OE}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C1484BV25, 72-Mbit (2 M × 36) Pipelined DCD Sync SRAM<br>Document Number: 001-75258 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 3489504 | 01/10/2012 | GOPA | New data sheet. |
| *A | 3756097 | 09/27/2012 | PRIT | Changed status from Preliminary to Final. |
| *B | 3861547 | 01/08/2013 | PRIT | No technical updates.<br>Completing Sunset Review. |
| *C | 4573182 | 11/18/2014 | PRIT | Updated Functional Description:<br>Added “For a complete list of related documentation, click here.” at the end.<br>Updated Package Diagrams:<br>spec 51-85050 – Changed revision from *D to *E. |
| *D | 5071123 | 01/04/2016 | PRIT | Updated to new template.<br>Completing Sunset Review. |

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