



UG123: SiOCXO1-EVB Evaluation Board User's Guide

The Silicon Labs SiOCXO1-EVB (kit) is used to help evaluate Silicon Labs Precision Jitter Attenuation/Frequency Translation product line for Stratum 3/3E, IEEE 1588 and G.8262 SyncE applications.

EVB FEATURES:

- Flexible Output Termination
- Power Supply Filtering
- Optional Output Buffer
- Optional OCXO Voltage Control Adjust

1. Quick Start

Refer to [Figure 3.1 Functional Block Diagram on page 3](#), [Figure 3.2 SiOCXO1-EB Shown Populated with an OCXO on page 3](#), and [Figure 4.1 SiOCXO1-EB Configured with Si5348 EVB on page 5](#) to clarify the instructions below.

1. Connect power to J1, and note that start-up current could be on the order of 1 amp. Check the manufacturers warm-up time.
2. Connect SiOCXO1-EB output, J2, to the Si5348 REF clock input using the short SMA cable provided with the EVB kit.

2. Top Layer View of Board

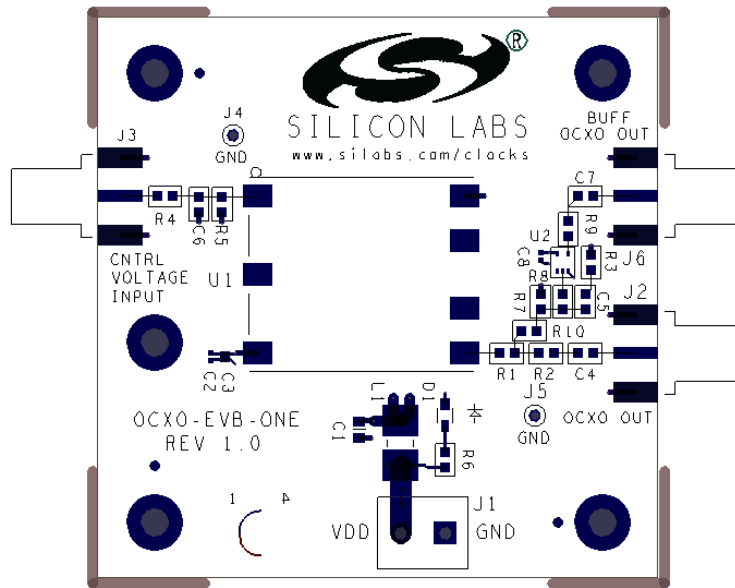


Figure 2.1. Top Layer View of Board

3. Functional Description

The SiOCXO1-EB is used in conjunction with Silicon Labs precision timing devices to facilitate characterization. The SiOCXO1-EB was designed to maximize output termination configurations as well as optional control voltage terminations. Resistors and capacitors are 0603, which makes it simple to remove and add various values. The SiOCXO1-EB bill of materials and PCB layouts are in Section 7. [Bill of Materials](#) and Section 6. [Schematic](#). The block diagram for the board is provided below:

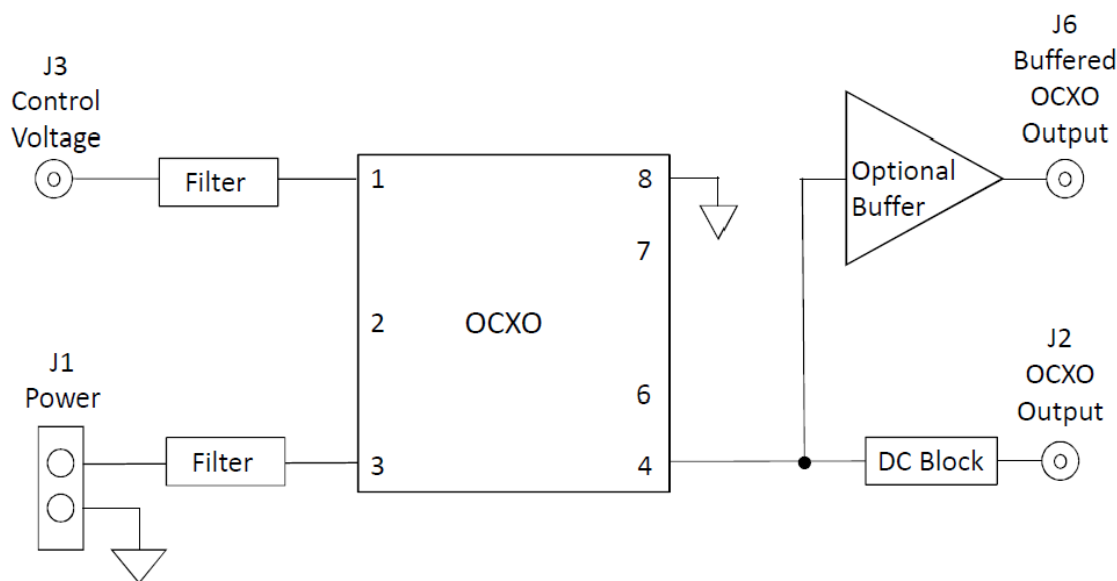


Figure 3.1. Functional Block Diagram

The SiOCXO1-EB is intended to be a general use board for a 7-pin OCXO with 22x25 nominal package size, such as the Rakon P/N STP3158 12.8 MHz pictured below. See Section 6. [Schematic](#) for example measurements carried out using this OCXO.

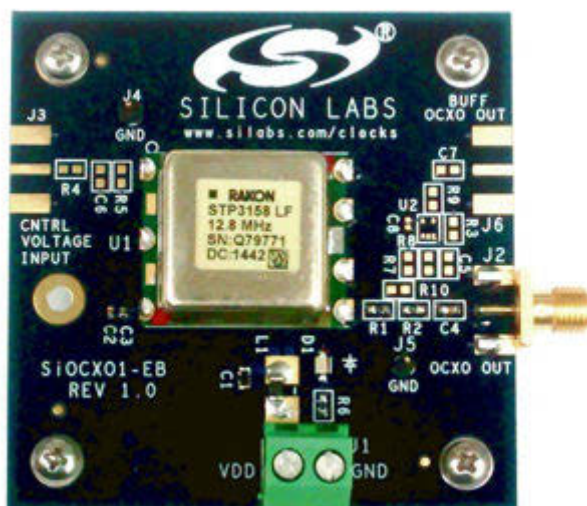


Figure 3.2. SiOCXO1-EB Shown Populated with an OCXO

3.1 Power Supply

The power supply voltage and current requirements are listed in the manufacturers data sheet. A 3.3 V $\pm 5\%$ supply is required. R6 may require modification if other voltages are used. Also, note the OCXO initial current can be on the order of 1A. Power supply filtering has been added to the evaluation board to minimize spurious response.

3.2 Output Termination and Optional Buffer

In most applications simple R C termination is used, as seen with R1 and C4 in [Figure 6.1 SiOCXO1-EB Schematic on page 7](#). This is a resistor to optimize impedance matching and a capacitor to block DC. Modifications can be made as required.

Optionally a buffer can be added to minimize loading on the OCXO's output, such as when driving cables. In this case U2, J6, C7, C8, R8, and R9 must be populated, while R2 can be depopulated.

3.3 Optional OCXO Frequency Adjust

Some OCXO's have an optional control voltage to adjust the output frequency, usually by a small amount such as 1 or 2 ppm. One example would be to discipline the OCXO to reduce the effects of OCXO aging. In this case, J3 and R4 must be populated as a minimum. C6 can be used for filtering or BW frequency limiting. Alternatively, R5 and C6 could be fixed or adjustable resistors to set a DC bias voltage.

4. Configuring the SiOCXO-EB

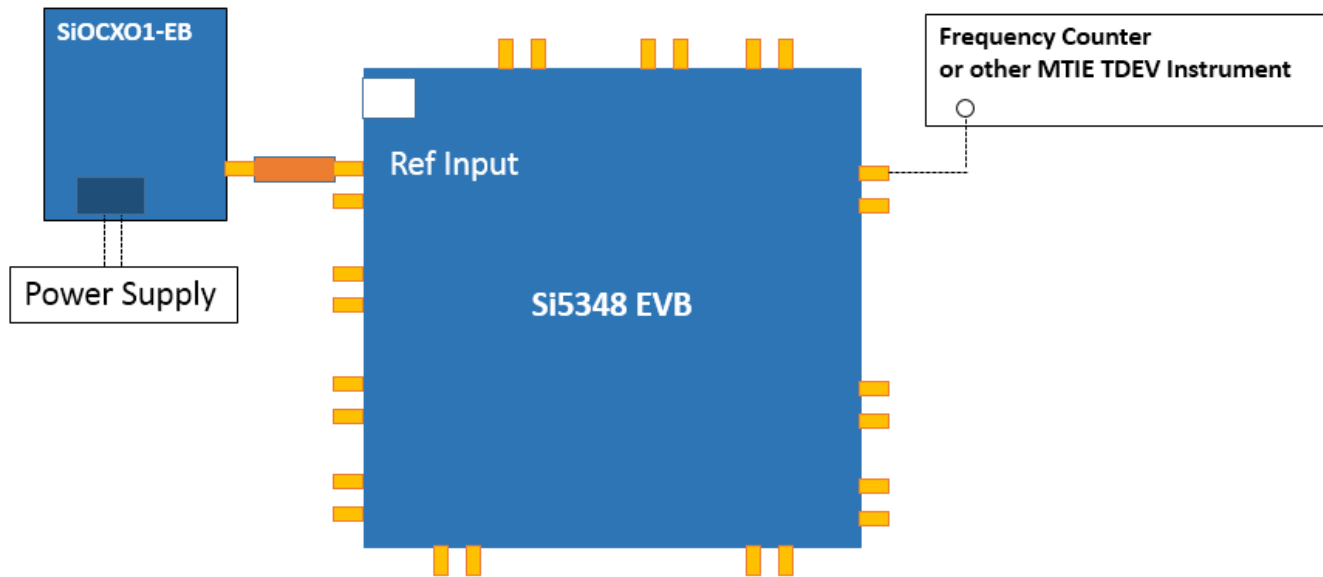


Figure 4.1. SiOCXO1-EB Configured with Si5348 EVB

The connection between the SiOCXO-EB and Si5348 EVB should be kept as short as possible. It is recommended to use a UPS Power Supply back-up for long term testing.

5. SiOCXO1-EB Functionality Test

1. Connect power to J1 (3.3 V).
2. Connect SiOCXO1-EB Output, J2, to an oscilloscope (terminate into 50 Ω).
3. Verify that the red LED is illuminated, the current draw matches closely to the specs, and the output matches the OCXO's data sheet.

5.1 Example Measurement Results Using STP3158LF 12.8 MHz OCXO from Rakon

Table 5.1. Current Specs for Rakon P/N STP3158 12.8 MHz at U1

| Example Current Draw | Expected Value (Data Sheet) | Example Measured Value |
|----------------------|-----------------------------|------------------------|
| Warm-up | ≤ 0.9 A | 0.72 A |
| Steady State | ≤ 0.3 A | 0.29 A |

Notes on Current Settling:

1. The system (including the LED and OCXO) initially drew 0.72–0.74 A of current from the 3.3 V power supply. At one minute, the current draw slightly decreased by 0.02–0.04A (warm-up time). Around the minute mark the current decreased rapidly to 0.32–0.37A. Then, the system decreased slightly to its consistent steady state current of 0.30 A within 20 minutes.
2. The LED draws around 10 mA, so subtract this from the power supply (system) current to get the current draw of the OCXO alone. These are the values reflected in the table above.

Steady State Output Waveform for Rakon P/N STP3158 12.8 MHz at U1

Verify the output is a 12.8 MHz LVCMOS waveform. For example, measure with a Tektronix TDS 20245, 200 MHz oscilloscope terminated with 50 Ω BNC T connector.

6. Schematic

Notes on U1 Layout:

- 1) U1 should be located close to J2.
- 2) Do not route traces underneath U1.
- 3) Do not place planes (copper pours) underneath the U1.
- 4) R7, R8 and C5 should be placed as to minimize stubs on the Fout to J2 trace.
- 5) R5, C6 should be placed as to minimize stubs on the J3 to VC trace.

Normally Not Populated

Control Voltage Circuit: J3, R4, C6, R5
Output Buffer: R8, C8, U2, R9, C7, J6
Output Termination: R7, C5, R3

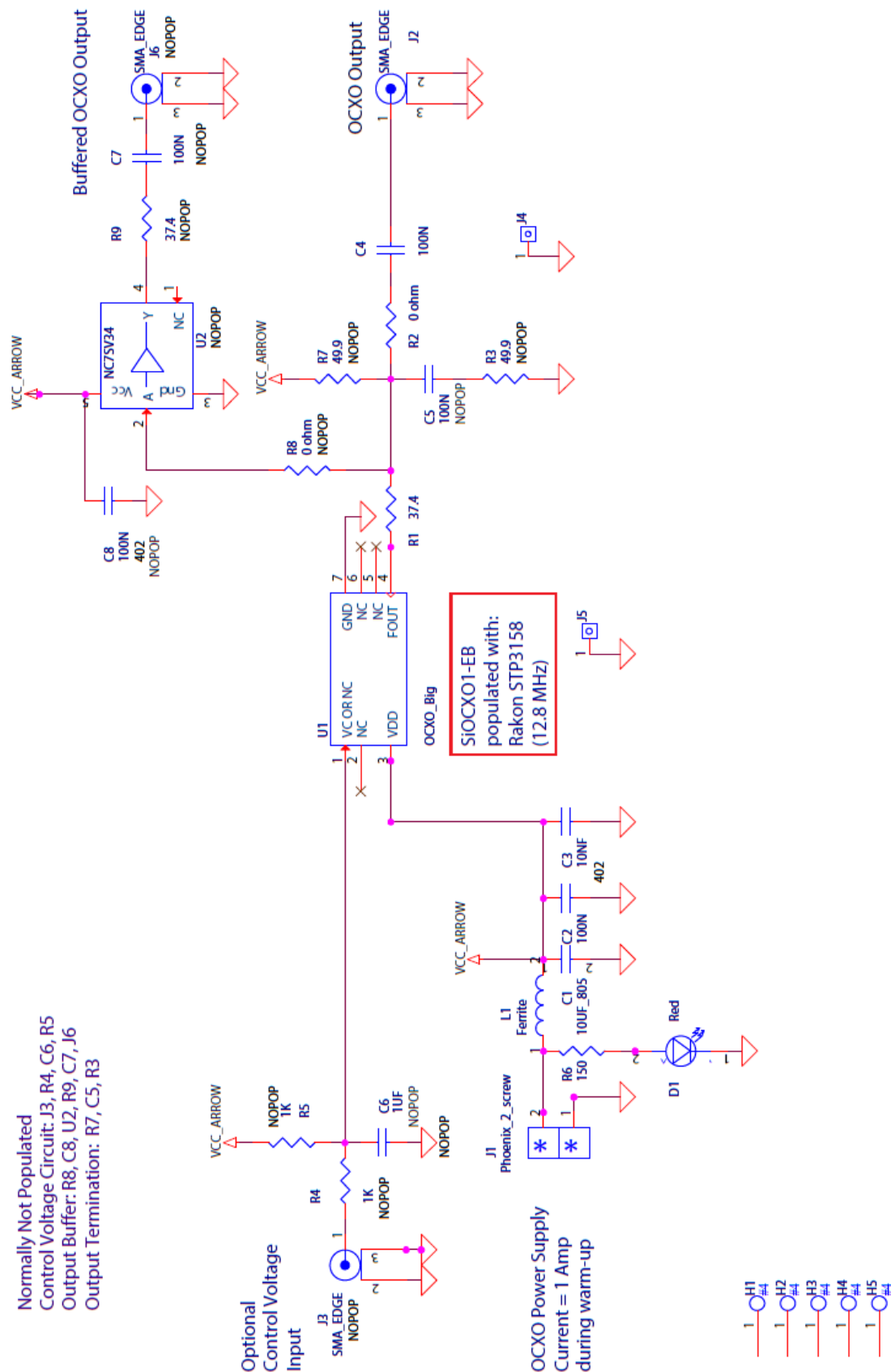


Figure 6.1. SiOCXO1-EB Schematic

7. Bill of Materials

Table 7.1. SiOCXO1-EB Bill of Materials

| Item | Quantity | Reference | Part | Manufacturer | Manufacturer Part Number | BOM | Digikey | Footprint | Comment |
|------|----------|----------------|-----------------|--------------|--------------------------|--------|-------------|----------------------|--------------------------------------------------------------------------------|
| 1 | 1 | C1 | 10UF_805 | Venkel | C0805Y5V6R3106ZN | | | 805 | |
| 2 | 2 | C2,C8 | 100N | Venkel | C0402X7R6R3-104KNE | | | 402 | |
| 3 | 1 | C3 | 10NF | Venkel | LIC0204X6S6R3-103MNE | | | 204 | |
| 4 | 2 | C4,C5 | 100N | Venkel | C0603X7R160-104KNE | | | 603 | |
| 7 | 1 | D1 | Red | Panasonic | LN1271RAL | | P493CT-ND | LED_gull_flip | |
| 8 | 5 | H1,H2,H3,H4,H5 | HOLE_NUM4 | | | | | plated-Num4hole | |
| 9 | 1 | J1 | Phoenix_2_screw | Phoenix | MKDSN1.5/2-5.08 | | 277-1247-ND | Phoenix2pinM_p2pitch | |
| 10 | 1 | J2 | SMA_EDGE | Johnson | 142-0701-801 | | J502-ND | SMA_EDGE_p062 | |
| 12 | 2 | J4,J5 | Jmpr_1pin | | | | | 1pin_p1pitch | |
| 13 | 1 | L1 | Ferrite | Steward | HI1612X560R-10 | | | 1612 | |
| 14 | 1 | R1 | 37.4 | Venkel | CR0603-16W-37R4FT | | | 603 | |
| 15 | 1 | R2 | 0 ohm | Venkel | CR0603-16W-000T | | | 603 | |
| 18 | 1 | R6 | 150 | Venkel | CR0603-16W-1500FT | | | 603 | |
| 21 | 1 | U1 | 12.8 MHz | Rakon | STP3158 | | | | Alternate = Connor Winfield OH300-50503CF-0 12.8M or AVX OO12.8000000M1 4070AT |
| 5 | 1 | C6 | 1UF | Venkel | C0603X7R6R3-105KNE | NO-POP | | 603 | |

| Item | Quantity | Reference | Part | Manufacturer | Manufacturer Part Number | BOM | Digikey | Footprint | Comment |
|------|----------|-----------|----------|--------------|--------------------------|--------|---------------|---------------|-----------------------------------|
| 6 | 1 | C7 | 100N | Venkel | C0603X7R160-104KNE | NO-POP | | 603 | |
| 11 | 2 | J3,J6 | SMA_EDGE | Johnson | 142-0701-801 | NO-POP | J502-ND | SMA_EDGE_p062 | |
| 16 | 2 | R3,R7 | 49.9 | Venkel | CR0603-16W-49R9FT | NO-POP | | 603 | |
| 17 | 2 | R4,R5 | 1K | Venkel | CR0603-16W-1001FT | NO-POP | | 603 | |
| 19 | 2 | R8,R10 | 0 ohm | Venkel | CR0603-16W-000T | NO-POP | | 603 | |
| 20 | 1 | R9 | 37.4 | Venkel | CR0603-16W-37R4FT | NO-POP | | 603 | |
| 22 | 1 | U2 | NC7SV34 | Fairchild | NC7SV34P5X | NO-POP | NC7SV34P5X-ND | SC-70-5 | Alternate = Fairchild NC7SZ126M5X |

Note: The OCXO must be populated if it is not.

8. Layout

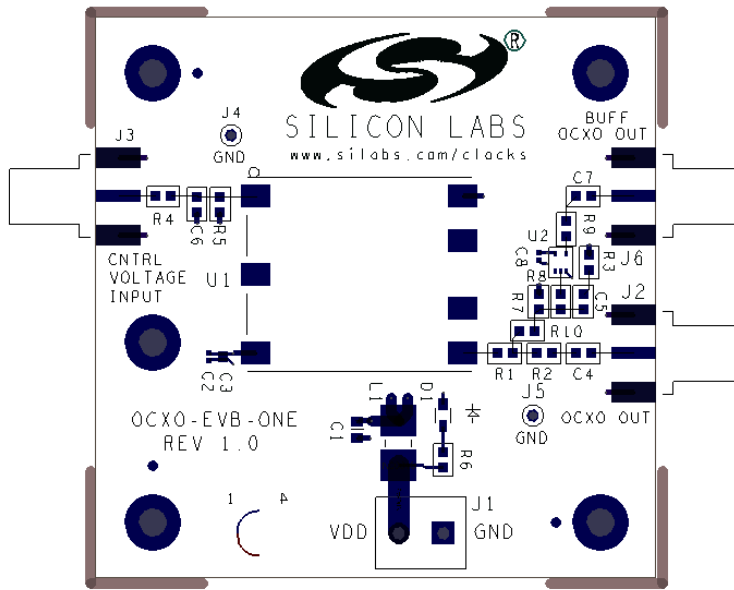


Figure 8.1. Layer 1: Primary Side

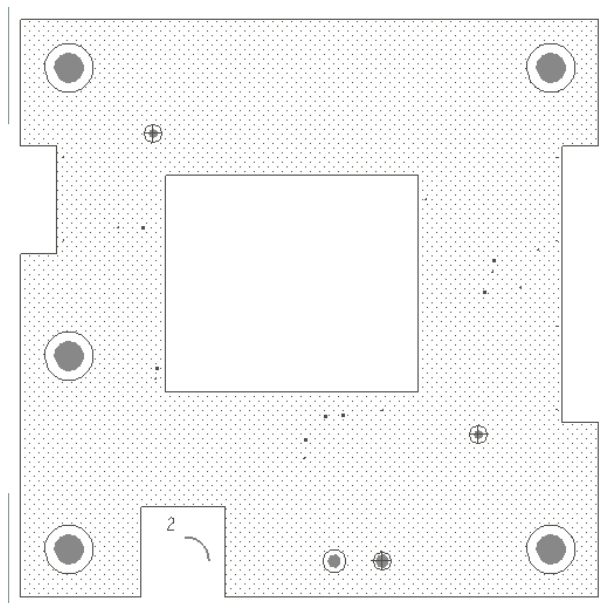


Figure 8.2. Layer 2: Ground

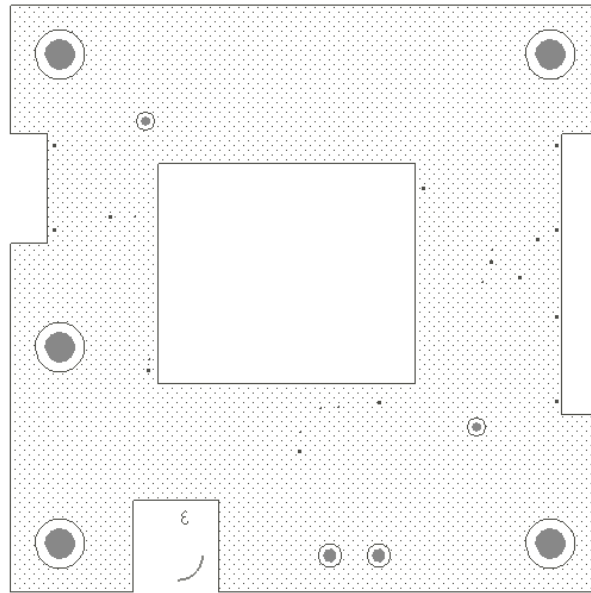


Figure 8.3. Layer 3: Power

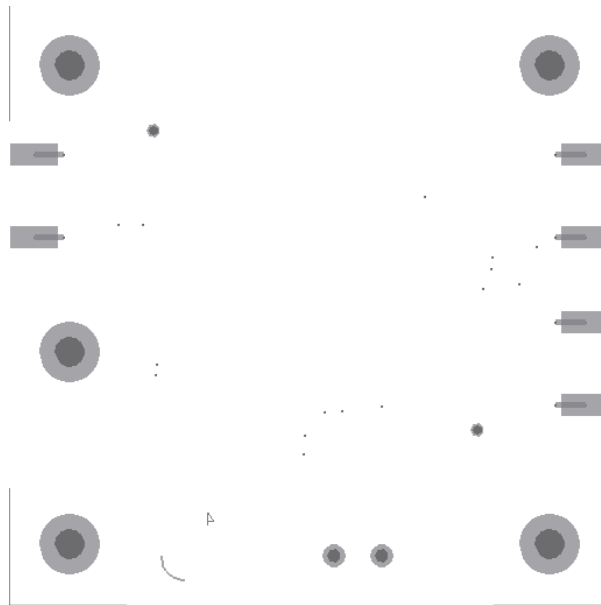


Figure 8.4. Layer 4: Secondary Side



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