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FDBL9401_F085

N-Channel PowerTrench[®] MOSFET

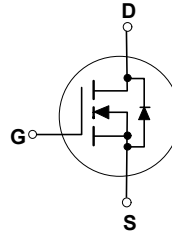
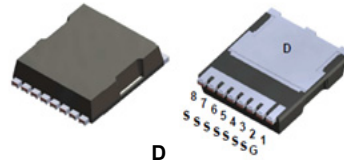
40 V, 300 A, 0.65 mΩ

Features

- Typical $R_{DS(on)}$ = 0.5 mΩ at $V_{GS} = 10V$, $I_D = 80 A$
- Typical $Q_g(tot)$ = 220 nC at $V_{GS} = 10V$, $I_D = 80 A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems



For current package drawing, please refer to the Fairchild website at <http://www.fairchildsemi.com/dwg/PS/PSOF08A.pdf>.

MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Rated	Units
V_{DSS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	300	A
	Pulsed Drain Current	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	1064	mJ
P_D	Power Dissipation	429	W
	Derate Above 25°C	2.86	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	°C/W

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^\circ C$, $L = 0.3mH$, $I_{AS} = 84A$, $V_{DD} = 40V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche.
- 3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package			
FDBL9401	FDBL9401_F085	MO-299A	-	-	-

FDBL9401_F085 N-Channel PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

$B_{V_{DS}}$	Drain-to-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 40\text{V}, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80\text{A}, T_J = 25^\circ\text{C}$	-	0.50	0.65	m Ω
		$V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	0.86	1.10	m Ω

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	15900	-	pF
C_{oss}	Output Capacitance		-	4025	-	pF
C_{rss}	Reverse Transfer Capacitance		-	604	-	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	-	2.6	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	-	220	296	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V				
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 20\text{V}, I_D = 80\text{A}$	-	73	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	41	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 20\text{V}, I_D = 80\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	-	-	221	ns
$t_{d(on)}$	Turn-On Delay		-	54	-	ns
t_r	Rise Time		-	82	-	ns
$t_{d(off)}$	Turn-Off Delay		-	106	-	ns
t_f	Fall Time		-	52	-	ns
t_{off}	Turn-Off Time		-	-	215	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}, V_{GS} = 0\text{V}$	-	-	1.25	V
		$I_{SD} = 40\text{A}, V_{GS} = 0\text{V}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	119	133	ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 32\text{V}$	-	228	274	nC

Note:

 4: The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

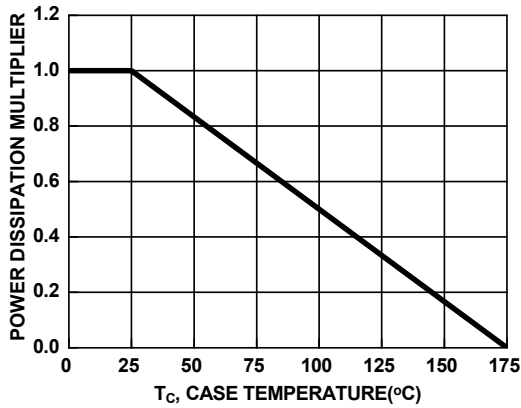


Figure 1. Normalized Power Dissipation vs. Case Temperature

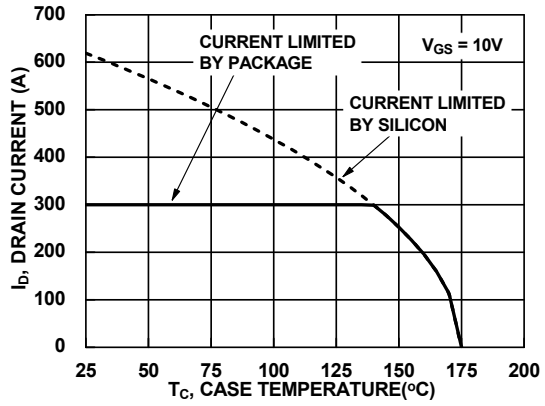


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

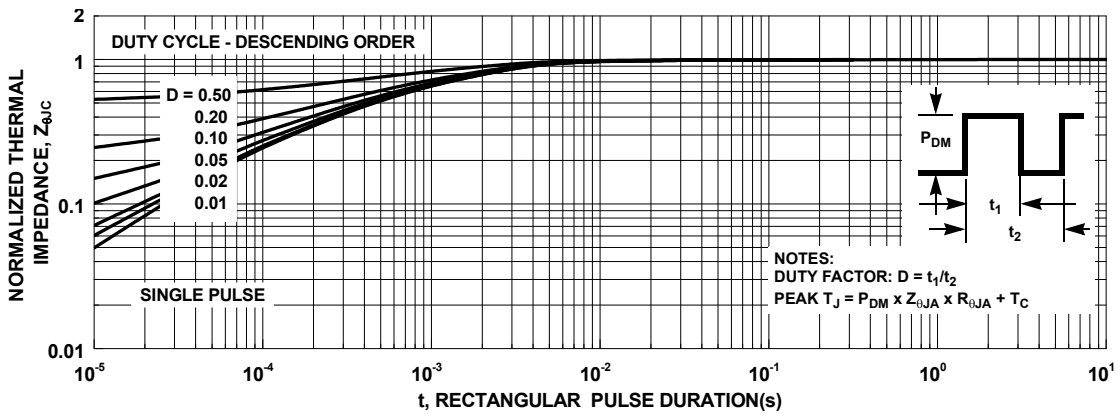


Figure 3. Normalized Maximum Transient Thermal Impedance

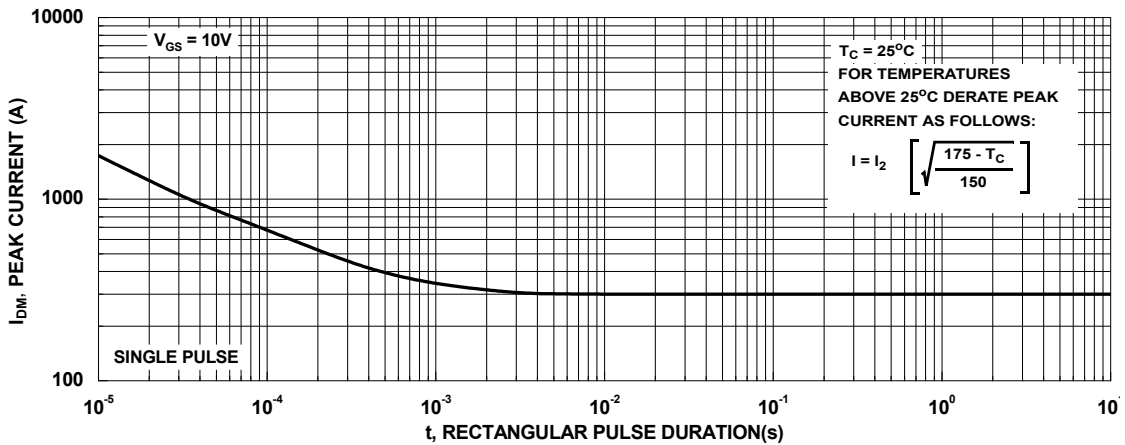


Figure 4. Peak Current Capability

Typical Characteristics

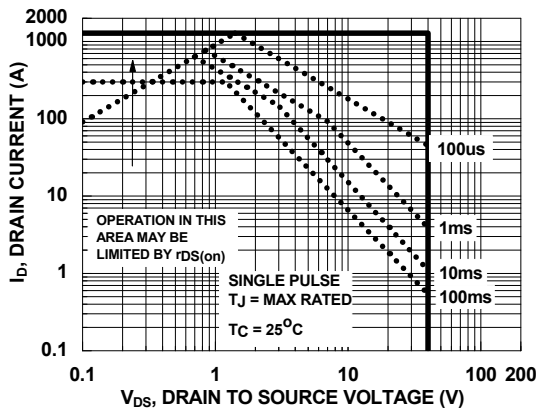
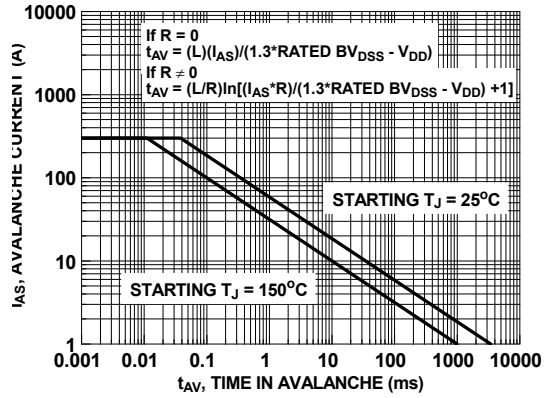


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

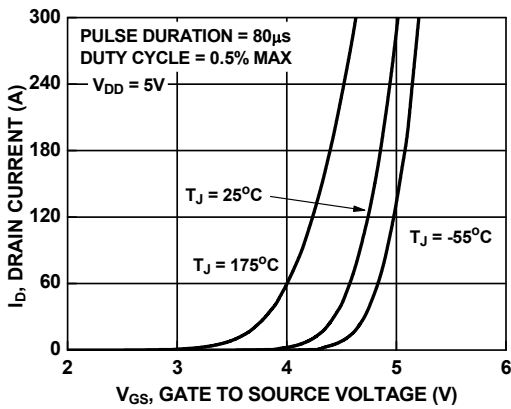


Figure 7. Transfer Characteristics

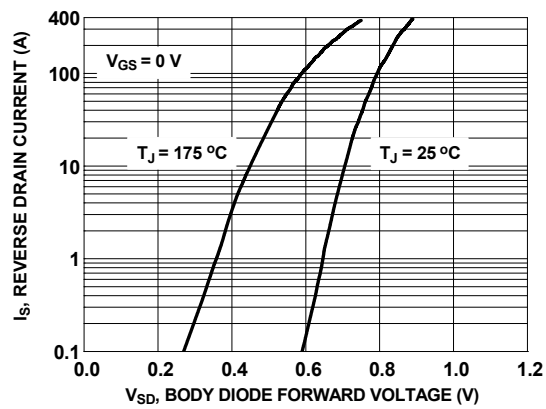


Figure 8. Forward Diode Characteristics

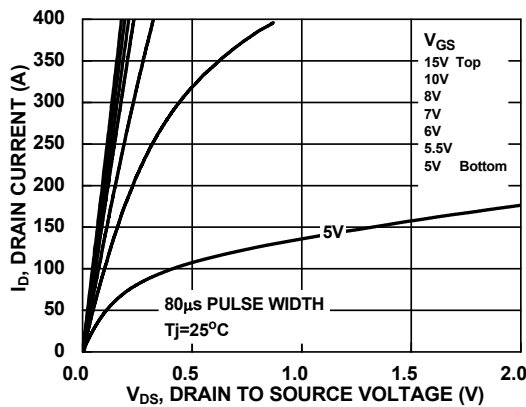


Figure 9. Saturation Characteristics

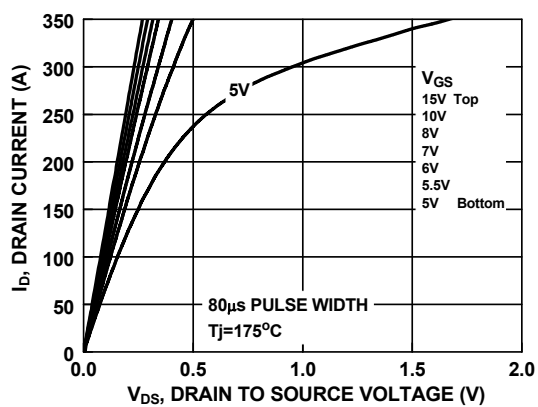


Figure 10. Saturation Characteristics

Typical Characteristics

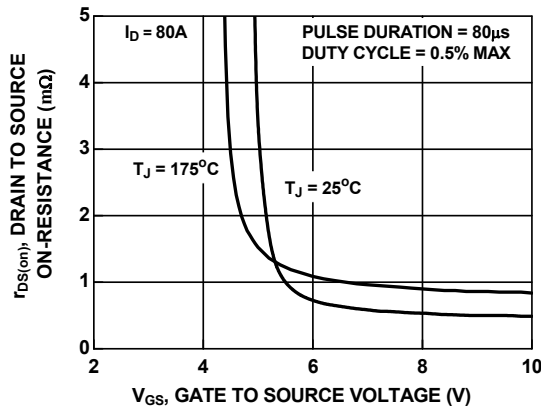


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

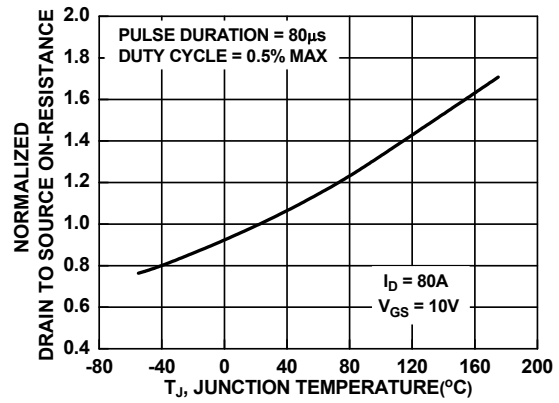


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

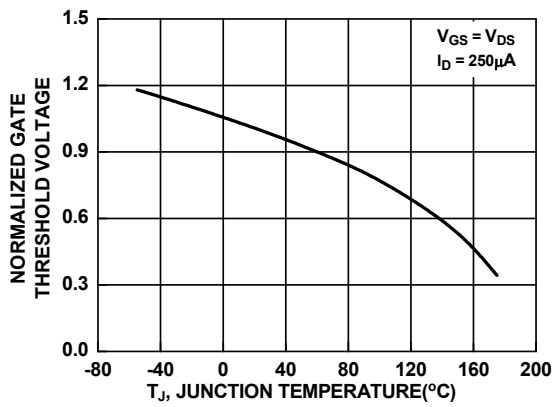


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

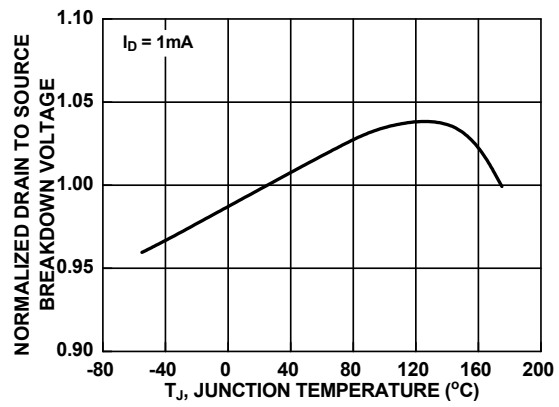


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

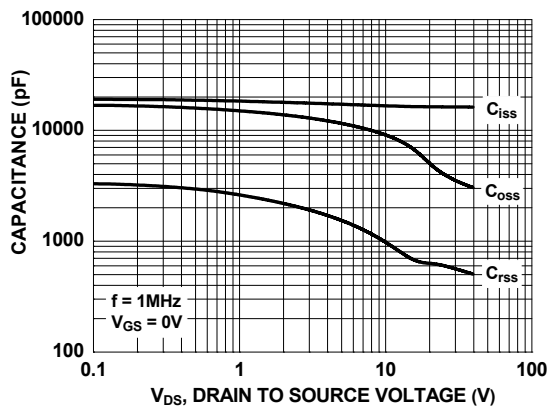


Figure 15. Capacitance vs. Drain to Source Voltage

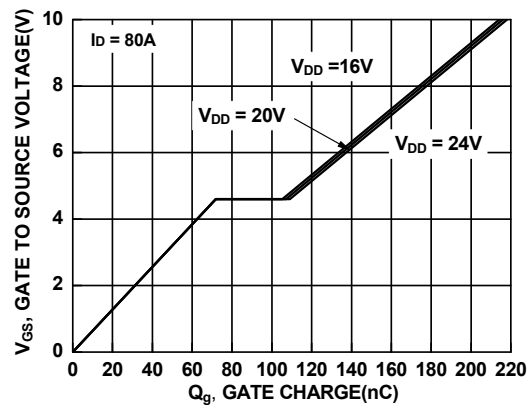







Figure 16. Gate Charge vs. Gate to Source Voltage



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