Arria V GX Starter Board

Reference Manual

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MNL-01069-1.4

Contents

Chapter 1. Overview

General Description 1–1
Board Component Blocks 1–2
Development Board Block Diagram 1–4
Handling the Board 1–4

Chapter 2. Board Components

Introduction 2–1
Board Overview 2–2
Featured Device: Arria V GX FPGA 2–5
I/O and Transceiver Resources 2–5
MAX V CPLD 5M2210 System Controller 2–7
FPGA Configuration 2–12
FPGA Programming over Embedded USB-Blaster 2–12
Flash Memory Programming 2–13
FPGA Programming from Flash Memory 2–14
FPGA Programming over External USB-Blaster 2–16
Status Elements 2–16
Setup Elements 2–17
Board Settings DIP Switch 2–18
JTAG Chain Control DIP Switch 2–18
PCI Express Link Width DIP Switch 2–18
CPU Reset Push Button 2–19
MAX V Reset Push Button 2–19
Image Load Push Button 2–19
Image Select Push Button 2–19
Clock Circuitry 2–20
On-Board Oscillators 2–20
Off-Board Clock Input/Output 2–22
General User Input/Output 2–23
User-Defined Push Buttons 2–23
User-Defined DIP Switch 2–24
User-Defined LEDs 2–24
General LEDs 2–24
HSMC LEDs 2–25
PCI Express LEDs 2–25
Character LCD 2–26
Components and Interfaces 2–27
PCI Express 2–28
10/100/1000 Ethernet 2–30
HSMC 2–31
SDI Video Output/Input 2–36
HDMI Video Output 2–38
Memory 2–39
DDR3 SDRAM 2–39
Synchronous SRAM 2–42
Flash 2–45
Power Supply 2–48

Power Distribution System 2–49
Power Measurement 2–50
Statement of China-RoHS Compliance 2–52
CE EMI Conformity Caution 2–52

Additional Information

Board Revision History Info–1
Document Revision History Info–1
How to Contact Altera Info–1
Typographic Conventions Info–2

1. Overview

This document describes the hardware features of the Arria® V GX starter board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Arria V GX starter board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs using Altera's Arria V GX FPGA device. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Arria V GX designs.

One high-speed mezzanine card (HSMC) connector is available to add additional functionality via a variety of HSMCs available from Altera® and various partners.

To see a list of the latest HSMCs available or to download a copy of the HSMC specification, refer to the Development Board Daughtercards page of the Altera website.

Design advancements and innovations, such as the PCI Express hard IP, partial reconfiguration, and hard memory controller implementation ensure that designs implemented in the Arria V GXs operate faster, with lower power, and have a faster time to market than previous FPGA families.

For more information on the following topics, refer to the respective documents:

- Arria V device family, refer to the *Arria V Device Handbook*.
- PCI Express MegaCore function, refer to the *PCI Express Compiler User Guide*.
- HSMC Specification, refer to the *High Speed Mezzanine Card (HSMC) Specification*.

Board Component Blocks

The starter board features the following major component blocks:

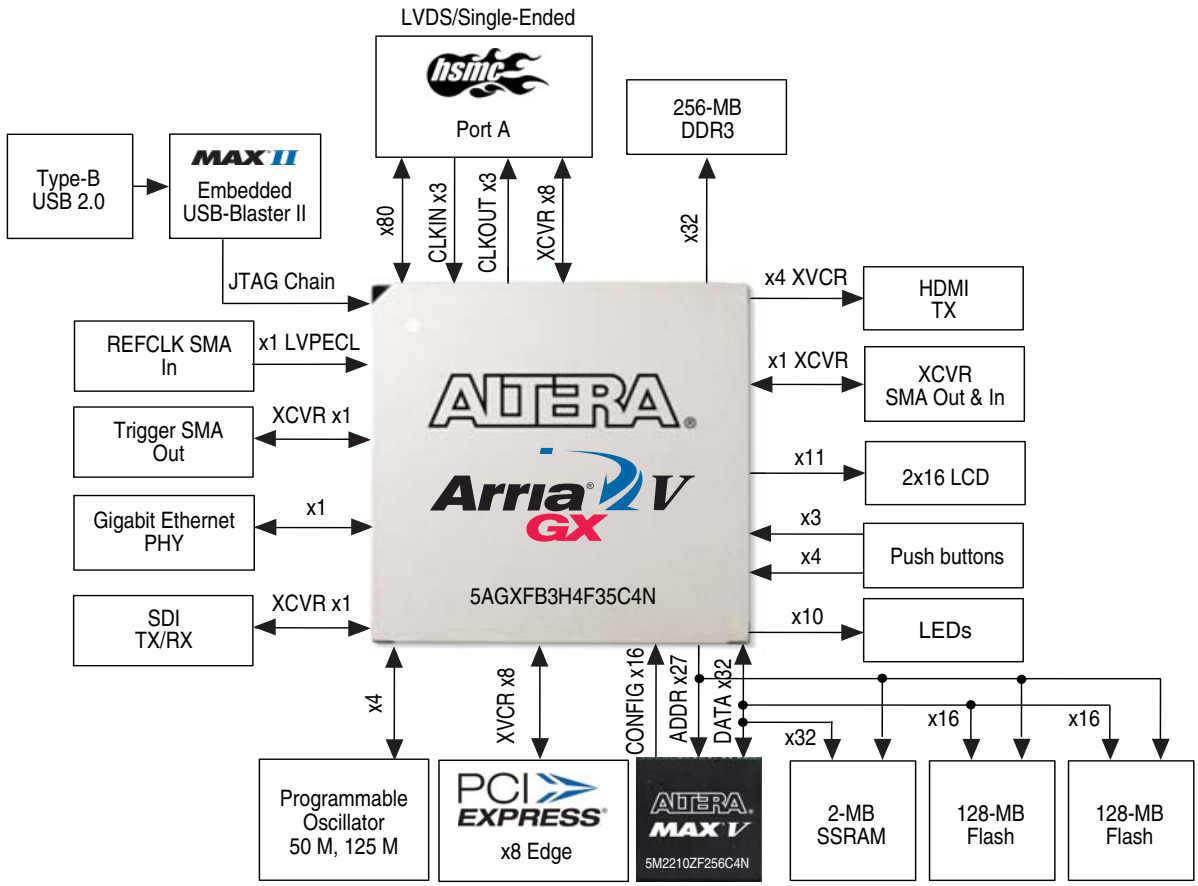
- One Arria V GX 5AGXFB3H4F35C4N FPGA in a 1152-pin FineLine BGA (FBGA) package
  - 362,000 LEs
  - 136,880 adaptive logic modules (ALMs)
  - 17,260 Kbit on-die block memory
  - 24 high-speed transceivers
  - 12 fractional phase locked loops (PLLs)
  - 2,090 18x19 multipliers
  - 544 general purpose input/output
  - 1.1-V core voltage
- MAX® V 5M2210ZF256C4N CPLD in a 256-pin FBGA package
- MAX II EPM570F100C5N CPLD in a 100-pin FBGA package
- FPGA configuration circuitry
  - MAX V CPLD 5M2210ZF256C4N System Controller and flash fast passive parallel (FPP) configuration
  - On-board USB-Blaster™ II for use with the Quartus® II Programmer
- Clocking circuitry
  - Programmable clock generator for FPGA reference clock input
  - 125-MHz LVDS oscillator for FPGA reference clock input
  - 148.5/148.35-MHz LVDS VCXO for FPGA reference clock input
  - 50-MHz single-ended oscillator for FPGA and CPLD clock input
  - 100-MHz single-ended oscillator for CPLD configuration clock input
  - SMA input (LVPECL)
- Memory
  - Two 128-Mbyte (MB) DDR3 SDRAM with a total of 32-bit data bus
  - 2-MB SSRAM
  - Two 128-MB synchronous flash

- General user I/O
  - LEDs and displays
    - Four user LEDs
    - One two-line character LCD display
    - Three configuration select LED
    - One configuration done LED
    - Four on-board USB-Blaster II status LEDs
    - Two HSMC interface transmit/receive LED (TX/RX)
    - Four PCI Express LEDs
    - Five Ethernet LEDs
    - One serial digital interface (SDI) carrier detect LED
  - Push buttons
    - One CPU reset push button
    - One configuration reset push button
    - Three general user push buttons
  - DIP switches
    - Four MAX V CPLD System Controller control switches
    - Three JTAG chain control switches
    - Three PCI Express link width switches
    - Four general user switches
- Power supply
  - 19-V (laptop) DC input
  - PCI Express edge connector power
- Mechanical
  - PCI card standard size (6.600" x 4.199")

Development Board Block Diagram

Figure 1–1 shows a block diagram of the Arria V GX starter board.

Figure 1–1. Arria V GX Starter Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces the major components on the Arria V GX starter board. Figure 2–1 illustrates the component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Arria V GX starter kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *Arria V GX Starter Kit User Guide*.

This chapter consists of the following sections:

- "Board Overview"
- "Featured Device: Arria V GX FPGA" on page 2–5
- "MAX V CPLD 5M2210 System Controller" on page 2–7
- "FPGA Configuration" on page 2–12
- "Clock Circuitry" on page 2–20
- "General User Input/Output" on page 2–23
- "Components and Interfaces" on page 2–27
- "Memory" on page 2–39
- "Power Supply" on page 2–48
- "Statement of China-RoHS Compliance" on page 2–52

Board Overview

This section provides an overview of the Arria V GX starter board, including an annotated board image and component descriptions. Figure 2–1 shows an overview of the board features.

Figure 2–1. Overview of the Arria V GX Starter Board Features

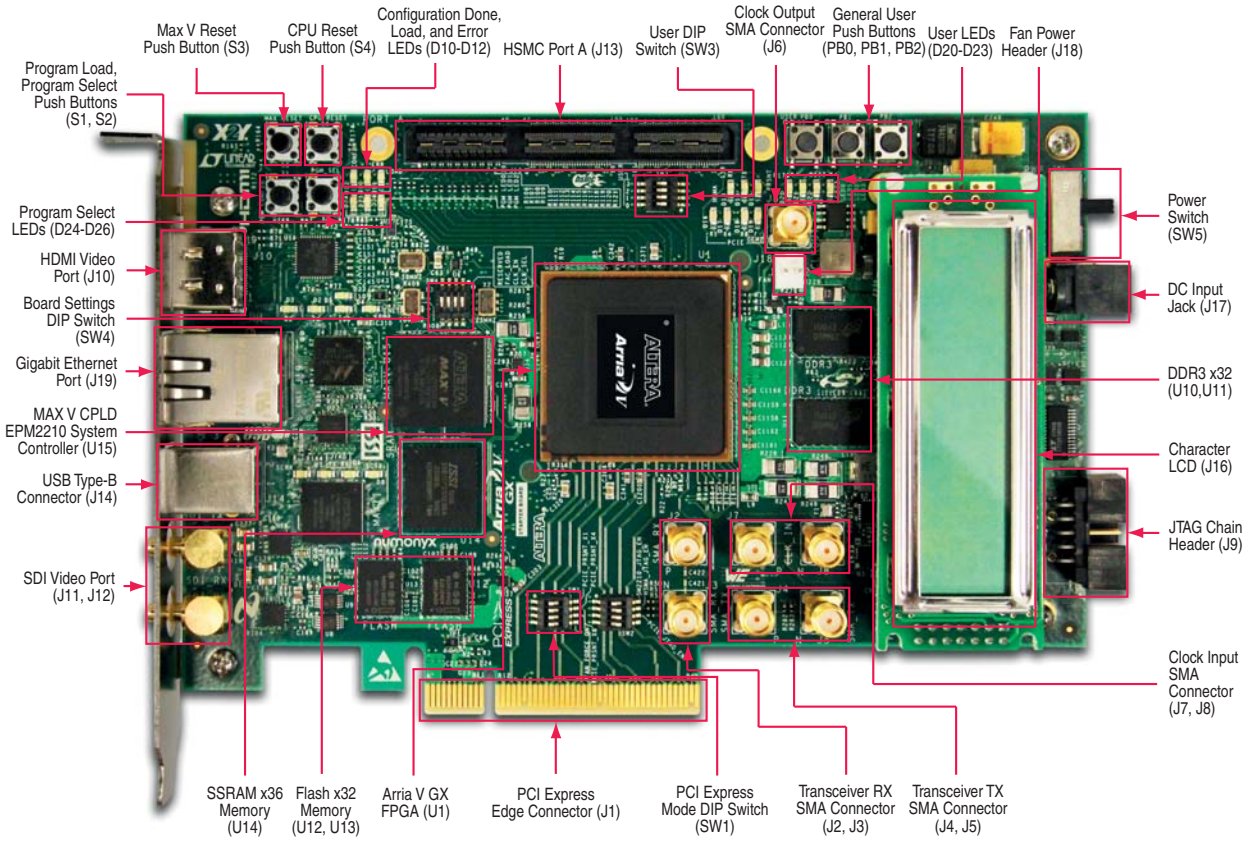


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Arria V GX Starter Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U1	FPGA	Arria V GX, 5AGXFB3H4F35C4N, 1152-pin FBGA.
U15	CPLD	MAX V CPLD, 5M2210ZF256C4N , 256-pin FBGA.
Configuration, Status, and Setup Elements		
J9	JTAG chain header	Provides access to the JTAG chain and disables the on-board USB-Blaster II when using an external USB-Blaster cable.
D6, D7	JTAG LEDs	Indicate transmit or receive activity of the JTAG chain. The TX and RX LEDs would flicker if the link is in use and active.
SW2	JTAG chain control DIP switch	Remove or include devices in the active JTAG chain.

Table 2–1. Arria V GX Starter Board Components (Part 2 of 3)

Board Reference	Type	Description
J14	On-Board USB-Blaster II	USB interface for programming and debugging the FPGA through embedded USB-Blaster II JTAG via a type-B USB cable.
SW4	Board settings DIP switch	Controls the MAX V CPLD 5M2210 System Controller functions such as clock enable, SMA clock input control, and which image to load from flash memory at power-up.
SW1	PCI Express DIP switch	Controls the PCI Express lane width by connecting `prsnt` pins together on the PCI Express edge connector.
S2	Image select push button	Toggles the configuration LEDs which selects the program image that loads from flash memory to the FPGA.
S1	Load image push button	Load image from flash memory to the FGPA based on the configuration LED setting.
D8, D9	System Console LEDs	Indicate transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active.
D12	Configuration done LED	Illuminates when the FPGA is configured.
D11	Load LED	Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA.
D10	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D30	Power LED	Illuminates when 5.0-V power is present.
D24, D25, D26	Configuration LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the `PGM_SEL` push button.
D2, D3, D4, D5, D33	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D13, D14	HSMC port A LEDs	You can configure these LEDs to indicate transmit or receive activity.
D15	HSMC port A present LED	Illuminates when a daughtercard is plugged into the HSMC port A.
D16, D17, D18, D19	PCI Express link LEDs	You can configure these LEDs to indicate the PCI Express link width (x1, x4, x8) and Gen2 link.
Clock Circuitry		
U4	Quad-output oscillator	Programmable oscillator with default frequencies of 125 MHz, 409.6 MHz, 156.25 MHz, and 100 MHz. The frequency is programmable using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X1	148.5-MHz oscillator	148.500-MHz voltage controlled crystal oscillator for serial digital interface (SDI) video. This oscillator is programmable to any frequency between 20–810 MHz using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X4	50-MHz oscillator	50.000-MHz crystal oscillator for general purpose logic.
X3	100-MHz oscillator	100.000-MHz crystal oscillator for the MAX V CPLD 5M2210 System Controller.
X2	125-MHz oscillator	125.000 MHz crystal oscillator for Gigabit Ethernet.
J7, J8	Clock input SMAs	Drive LVPECL-compatible clock inputs into the clock multiplexer buffer (U5).
J6	Clock output SMA	Drive out 2.5-V CMOS clock output from the FPGA.

Table 2–1. Arria V GX Starter Board Components (Part 3 of 3)

Board Reference	Type	Description
General User Input/Output		
D20–D23	User LEDs	Four user LEDs. Illuminates when driven low.
SW3	User DIP switch	Quad user DIP switches. When the switch is ON, a logic 0 is selected.
S4	CPU reset push button	Press to reset the FPGA logic.
S3	MAX V reset push button	Press to reset the MAX V CPLD 5M2210 System Controller.
S5, S6, S7	General user push buttons	Three user push buttons. Driven low when pressed.
Memory Devices		
U10, U11	DDR3 x32 memory	256-Mbyte DDR3 SDRAM with a 32-bit data bus. The 32-bit data bus consists of two x16 devices with a single address or command bus.
U14	SSRAM x36 memory	2-Mbyte standard synchronous RAM with a 32-bit data bus and 4-bit parity.
U12, U13	Flash x32 memory	Two 128-Mbyte synchronous flash devices with 16-bit data buses for non-volatile memory. The board supports two flash devices of 16-bit interface each, which combine to allow for 256-Mbyte synchronous flash with a 32-bit data bus.
Communication Ports		
J1	PCI Express edge connector	Gold-plated edge fingers connector for up to ×8 signaling in Gen1 or Gen2 mode.
J13	HSMC port A	Provides eight transceiver channels and 84 CMOS or 17 LVDS channels per the HSMC specification.
J19	Gigabit Ethernet connector	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode.
Video and Display Ports		
J16	Character LCD	Connector that interfaces to a provided 16 character × 2 line LCD module along with two standoffs.
J10	HDMI video port	A 19-pin HDMI connector that provides a HDMI video output of up to 1080i.
J11, J12	SDI video port	Two 75-Ω sub-miniature version B (SMB) connectors that provide a full-duplex SDI interface through a LMH0303 cable driver and LMH0384 cable equalizer.
Power Supply		
J1	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J17	DC input jack	Accepts a 14–20-V DC power supply. This input jack is not to be used while the board is plugged into a PCI Express slot.
SW5	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Arria V GX FPGA

The Arria V GX starter board features a Arria V GX 5AGXFB3H4F35C4N device (U1) in a 1152-pin FBGA package.

For more information about Arria V device family, refer to the *Arria V Device Handbook*.

Table 2–2 describes the features of the Arria V GX 5AGXFB3H4F35C4N device.

Table 2–2. Arria V GX Features

ALMs	Equivalent LEs	M10K RAM Blocks	Total RAM (Kbits)	18-bit × 19-bit Multipliers	PLLs	Transceivers	Package Type
136,880	362,000	1,726	17,260	2,090	12	24	1152-pin FBGA

Table 2–3 lists the Arria V GX component reference and manufacturing information.

Table 2–3. Arria V GX Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U1	FPGA, Arria V GX F1152, 362K LEs, leadfree	Altera Corporation	5AGXFB3H4F35C4N	www.altera.com

I/O and Transceiver Resources

Figure 2–2 illustrates the bank organization and I/O count for the Arria V GX 5AGXFB3H4F35C4N device in the 1152-pin FBGA package.

Figure 2–2. Arria V GX Device I/O Bank Diagram

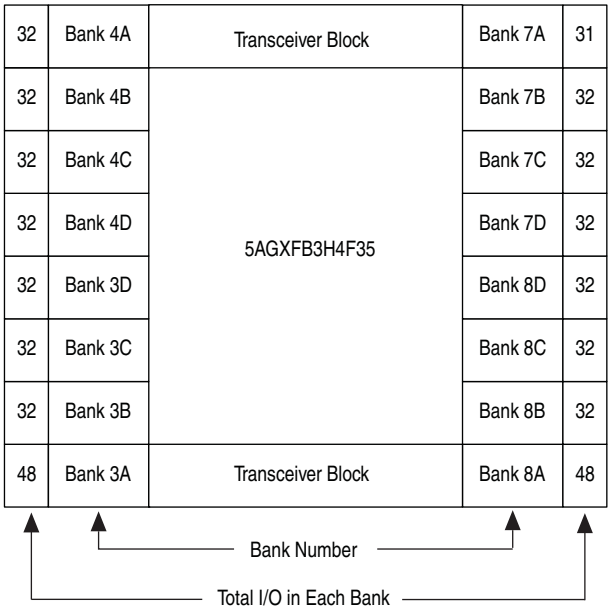


Figure 2–3 illustrates the transceiver channels on the left and right side of the Arria V GX 5AGXFB3H4F35C4N device in the 1152-pin FBGA package.

Figure 2–3. Arria V GX Device Transceiver Bank Diagram

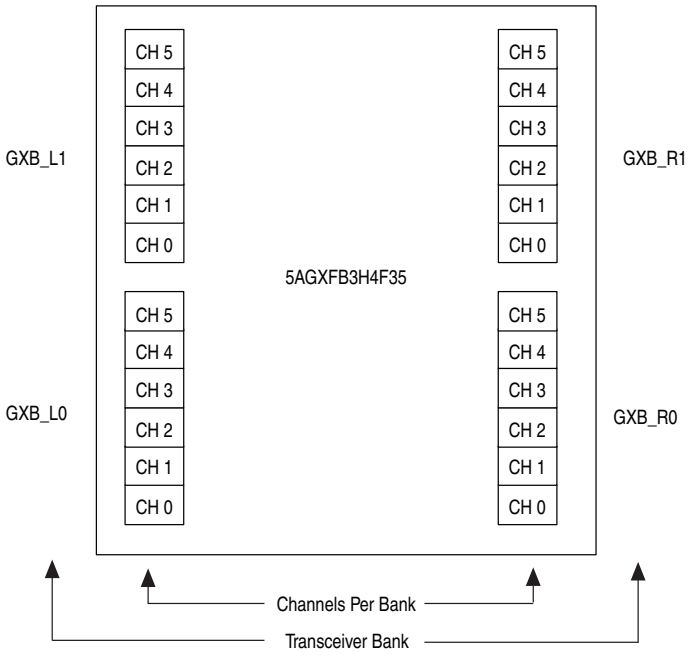


Table 2–4 lists the Arria V GX device I/O and transceiver pin count and usage by function on the board.

Table 2–4. Arria V GX Device I/O and Transceiver Pin Count

Function	I/O Standard	I/O Count	Special Pins
DDR3	1.5-V SSTL	70	One differential x4 DQS pin
Flash, SSRAM, and MAX V FSM bus	2.5-V CMOS	87	—
MAX V CPLD 5M2210 System Controller	2.5-V CMOS	10	—
PCI Express x8	2.5-V CMOS + XCVR	42	One reference clock
HSMA port A	2.5-V CMOS + LVDS + XCVR	116	Eight XCVR, 17 LVDS, six clock inputs/outputs, I^2C
Gigabit Ethernet	2.5-V CMOS + LVDS	20	One LVDS
On-Board USB-Blaster II	2.5-V CMOS	20	—
SDI video	2.5-V CMOS	15	One reference clock
HDMI video	2.5-V CMOS	14	One reference clock
Push buttons	2.5-V CMOS	4	One DEV_CLRn
DIP switches	2.5-V CMOS	4	—
Character LCD	2.5-V CMOS	11	—
LEDs	2.5-V CMOS	7	—
Clock or Oscillators	2.5-V CMOS + LVDS + PCML	21	11 reference clock
Total I/O Used:		**441**	

MAX V CPLD 5M2210 System Controller

The board utilizes the 5M2210 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash
- Power measurement
- Fan control (shared with the FPGA)
- Control registers for clocks
- Control and status registers for remote system update

Figure 2–4 illustrates the MAX V CPLD 5M2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–4. MAX V CPLD 5M2210 System Controller Block Diagram

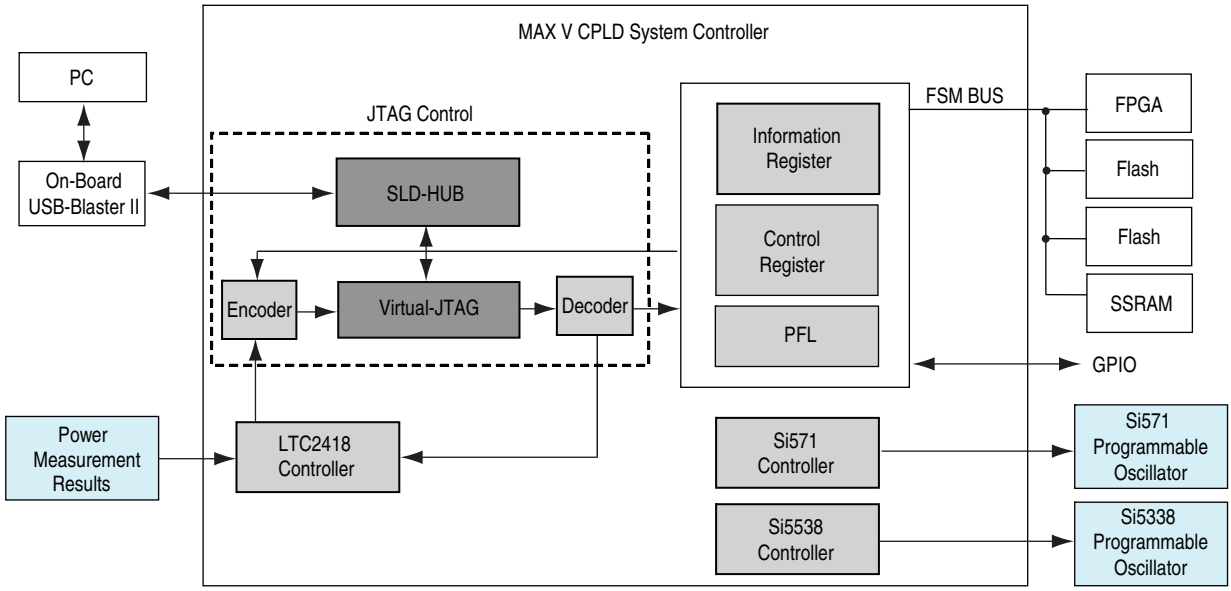


Table 2–5 lists the I/O signals present on the MAX V CPLD 5M2210 System Controller. The signal names and functions are relative to the MAX V device (U15).

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 1 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
N4	5M2210_JTAG_TMS	2.5-V	MAX V JTAG TMS
B9	CLK125_EN	2.5-V	125 MHz oscillator enable
E9	CLK50_EN	2.5-V	50 MHz oscillator enable
J5	CLK_CONFIG	2.5-V	100 MHz configuration clock input
A15	CLK_ENABLE	2.5-V	DIP switch for clock oscillator enable
A13	CLK_SEL	2.5-V	DIP switch for clock select—SMA or oscillator
J12	CLKIN_50_MAXV	2.5-V	50 MHz clock input

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 2 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
C9	CLOCK_SCL	2.5-V	Programmable oscillator I2C clock
D9	CLOCK_SDA	2.5-V	Programmable oscillator I2C data
D10	CPU_RESETN	2.5-V	FPGA reset push button
M1	EXTRA_SIG0	2.5-V	USB-Blaster II interface. Reserved for future use.
T13	EXTRA_SIG1	2.5-V	USB-Blaster II interface. Reserved for future use.
T15	EXTRA_SIG2	2.5-V	USB-Blaster II interface. Reserved for future use.
A2	FACTORY_LOAD	2.5-V	DIP switch to load factory or user design at power-up
R14	FACTORY_REQUEST	2.5-V	On-Board USB-Blaster II request to send FACTORY command
N12	FACTORY_STATUS	2.5-V	On-Board USB-Blaster II FACTORY command status
C8	FAN_FORCE_ON	2.5-V	DIP switch to on or off the fan
N7	FLASH_ADVN	2.5-V	FSM bus flash memory address valid
R5	FLASH_CEN0	2.5-V	FSM bus flash memory chip enable 0
M7	FLASH_CEN1	2.5-V	FSM bus flash memory chip enable 1
R6	FLASH_CLK	2.5-V	FSM bus flash memory clock
M6	FLASH_OEN	2.5-V	FSM bus flash memory output enable
T5	FLASH_RDYBSYN0	2.5-V	FSM bus flash memory ready 0
R7	FLASH_RDYBSYN1	2.5-V	FSM bus flash memory ready 1
P7	FLASH_RESETN	2.5-V	FSM bus flash memory reset
N6	FLASH_WEN	2.5-V	FSM bus flash memory write enable
K1	FPGA_CONF_DONE	2.5-V	FPGA configuration done LED
D3	FPGA_CONFIG_D0	2.5-V	FPGA configuration data
C2	FPGA_CONFIG_D1	2.5-V	FPGA configuration data
C3	FPGA_CONFIG_D2	2.5-V	FPGA configuration data
E3	FPGA_CONFIG_D3	2.5-V	FPGA configuration data
D2	FPGA_CONFIG_D4	2.5-V	FPGA configuration data
E4	FPGA_CONFIG_D5	2.5-V	FPGA configuration data
D1	FPGA_CONFIG_D6	2.5-V	FPGA configuration data
E5	FPGA_CONFIG_D7	2.5-V	FPGA configuration data
F3	FPGA_CONFIG_D8	2.5-V	FPGA configuration data
E1	FPGA_CONFIG_D9	2.5-V	FPGA configuration data
F4	FPGA_CONFIG_D10	2.5-V	FPGA configuration data
F2	FPGA_CONFIG_D11	2.5-V	FPGA configuration data
F1	FPGA_CONFIG_D12	2.5-V	FPGA configuration data
F6	FPGA_CONFIG_D13	2.5-V	FPGA configuration data
G2	FPGA_CONFIG_D14	2.5-V	FPGA configuration data
G3	FPGA_CONFIG_D15	2.5-V	FPGA configuration data
N3	FPGA_CVP_CONFDONE	2.5-V	FPGA configuration via protocol done LED
J3	FPGA_DCLK	2.5-V	FPGA configuration clock

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 3 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
N1	FPGA_NCONFIG	2.5-V	FPGA configuration active
J4	FPGA_NSTATUS	2.5-V	FPGA configuration ready
H1	FPGA_PR_DONE	2.5-V	FPGA partial reconfiguration done
P2	FPGA_PR_ERROR	2.5-V	FPGA partial reconfiguration error
E2	FPGA_PR_READY	2.5-V	FPGA partial reconfiguration ready
F5	FPGA_PR_REQUEST	2.5-V	FPGA partial reconfiguration request
E14	FSM_A0	2.5-V	FSM address bus
C14	FSM_A1	2.5-V	FSM address bus
C15	FSM_A2	2.5-V	FSM address bus
E13	FSM_A3	2.5-V	FSM address bus
E12	FSM_A4	2.5-V	FSM address bus
D15	FSM_A5	2.5-V	FSM address bus
F14	FSM_A6	2.5-V	FSM address bus
D16	FSM_A7	2.5-V	FSM address bus
F13	FSM_A8	2.5-V	FSM address bus
E15	FSM_A9	2.5-V	FSM address bus
E16	FSM_A10	2.5-V	FSM address bus
F15	FSM_A11	2.5-V	FSM address bus
G14	FSM_A12	2.5-V	FSM address bus
F16	FSM_A13	2.5-V	FSM address bus
G13	FSM_A14	2.5-V	FSM address bus
G15	FSM_A15	2.5-V	FSM address bus
G12	FSM_A16	2.5-V	FSM address bus
G16	FSM_A17	2.5-V	FSM address bus
H14	FSM_A18	2.5-V	FSM address bus
H15	FSM_A19	2.5-V	FSM address bus
H13	FSM_A20	2.5-V	FSM address bus
H16	FSM_A21	2.5-V	FSM address bus
J13	FSM_A22	2.5-V	FSM address bus
R3	FSM_A23	2.5-V	FSM address bus
P5	FSM_A24	2.5-V	FSM address bus
T2	FSM_A25	2.5-V	FSM address bus
J14	FSM_D0	2.5-V	FSM data bus
J15	FSM_D1	2.5-V	FSM data bus
K16	FSM_D2	2.5-V	FSM data bus
K13	FSM_D3	2.5-V	FSM data bus
K15	FSM_D4	2.5-V	FSM data bus
K14	FSM_D5	2.5-V	FSM data bus
L16	FSM_D6	2.5-V	FSM data bus

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 4 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
L11	FSM_D7	2.5-V	FSM data bus
L15	FSM_D8	2.5-V	FSM data bus
L12	FSM_D9	2.5-V	FSM data bus
M16	FSM_D10	2.5-V	FSM data bus
L13	FSM_D11	2.5-V	FSM data bus
M15	FSM_D12	2.5-V	FSM data bus
L14	FSM_D13	2.5-V	FSM data bus
N16	FSM_D14	2.5-V	FSM data bus
M13	FSM_D15	2.5-V	FSM data bus
N15	FSM_D16	2.5-V	FSM data bus
N14	FSM_D17	2.5-V	FSM data bus
P15	FSM_D18	2.5-V	FSM data bus
P14	FSM_D19	2.5-V	FSM data bus
D13	FSM_D20	2.5-V	FSM data bus
D14	FSM_D21	2.5-V	FSM data bus
F11	FSM_D22	2.5-V	FSM data bus
J16	FSM_D23	2.5-V	FSM data bus
F12	FSM_D24	2.5-V	FSM data bus
K12	FSM_D25	2.5-V	FSM data bus
M14	FSM_D26	2.5-V	FSM data bus
N13	FSM_D27	2.5-V	FSM data bus
R1	FSM_D28	2.5-V	FSM data bus
P4	FSM_D29	2.5-V	FSM data bus
N5	FSM_D30	2.5-V	FSM data bus
P6	FSM_D31	2.5-V	FSM data bus
B8	HSMA_PRSNTN	2.5-V	HSMC port A present
D6	INT_TSD_SDA	2.5-V	Internal TSD I^2C bus
E6	INT_TSD_SCL	2.5-V	Internal TSD I^2C bus
C4	LTC3880_SDA_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
B4	LTC3880_SCL_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
B1	LTC3880_ALERT_N_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
C5	LTC3880_GPIO0_N_2.5V	2.5-V	1.1-V VCC core power supply to PMBus
L6	JTAG_5M2210_TDI	2.5-V	MAX V CPLD on-board JTAG chain data in
M5	JTAG_5M2210_TDO	2.5-V	MAX V CPLD on-board JTAG chain data out
P3	JTAG_TCK	2.5-V	JTAG chain clock
P11	M570_CLOCK	2.5-V	25-MHz clock to on-board USB-Blaster II for sending FACTORY command
P12	M570_PCIE_JTAG_EN	2.5-V	Low signal to disable the on-board USB-Blaster II when PCI Express is the master to the JTAG chain

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 5 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
P10	MAX5_BEN0	2.5-V	FSM bus MAX V byte enable 0
R11	MAX5_BEN1	2.5-V	FSM bus MAX V byte enable 1
T12	MAX5_BEN2	2.5-V	FSM bus MAX V byte enable 2
N11	MAX5_BEN3	2.5-V	FSM bus MAX V byte enable 3
T11	MAX5_CLK	2.5-V	FSM bus MAX V clock
R10	MAX5_CSN	2.5-V	FSM bus MAX V chip select
M10	MAX5_OEN	2.5-V	FSM bus MAX V output enable
N10	MAX5_WEN	2.5-V	FSM bus MAX V write enable
E11	MAX_CONF_DONEN	2.5-V	On-board USB-Blaster II configuration done LED
A4	MAX_ERROR	2.5-V	FPGA configuration error LED
A6	MAX_LOAD	2.5-V	FPGA configuration active LED
M9	MAX_RESETN	2.5-V	MAX V reset push button
B10	MSEL0	2.5-V	FPGA mode select 0
B3	MSEL1	2.5-V	FPGA mode select 1
C10	MSEL2	2.5-V	FPGA mode select 2
C12	MSEL3	2.5-V	FPGA mode select 3
C6	MSEL4	2.5-V	FPGA mode select 4
B7	OVERTEMP	2.5-V	Temperature monitor fan enable
C7	PCIE_JTAG_EN	2.5-V	DIP switch to enable the PCI Express JTAG master
D12	PGM_CONFIG	2.5-V	Load the flash memory image identified by the PGM LEDs
B14	PGM_LED0	2.5-V	Flash memory PGM select indicator 0
C13	PGM_LED1	2.5-V	Flash memory PGM select indicator 1
B16	PGM_LED2	2.5-V	Flash memory PGM select indicator 2
B13	PGM_SEL	2.5-V	Toggles the PGM_LED[2:0] LED sequence
D5	SDI_RX_BYPASS	2.5-V	SDI equalization bypass
E8	SDI_RX_EN	2.5-V	SDI receive enable
D11	SDI_TX_EN	2.5-V	SDI transmit enable
R12	SECURITY_MODE	2.5-V	Reserved for future use
E7	SENSE_CS0N	2.5-V	Power monitor chip select
A5	SENSE_SCK	2.5-V	Power monitor SPI clock
D7	SENSE_SDI	2.5-V	Power monitor SPI data in
B6	SENSE_SDO	2.5-V	Power monitor SPI data out
D4	SI571_EN	2.5-V	Si571 programmable VCXO enable
R4	USB_CFG0	2.5-V	Reserved for future use
T4	USB_CFG1	2.5-V	Reserved for future use
P8	USB_CFG2	2.5-V	Reserved for future use
T7	USB_CFG3	2.5-V	Reserved for future use
N8	USB_CFG4	2.5-V	Reserved for future use
R8	USB_CFG5	2.5-V	Reserved for future use

Table 2–5. MAX V CPLD 5M2210 System Controller Device Pin-Out (Part 6 of 6)

Board Reference (U15)	Schematic Signal Name	I/O Standard	Description
T8	USB_CFG6	2.5-V	Reserved for future use
T9	USB_CFG7	2.5-V	Reserved for future use
R9	USB_CFG8	2.5-V	Reserved for future use
P9	USB_CFG9	2.5-V	Reserved for future use
M8	USB_CFG10	2.5-V	Reserved for future use
T10	USB_CFG11	2.5-V	Reserved for future use
H5	USB_CLK	2.5-V	On-board USB-Blaster II clock

Table 2–6 lists the MAX V CPLD 5M2210 System Controller component reference and manufacturing information.

Table 2–6. MAX II CPLD 5M2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U15	IC - MAX V CPLD 2210 LES, 256 FBGA 1.8 V VCCINT	Altera Corporation	5M2210ZF256C4N	www.altera.com

FPGA Configuration

This section describes the FPGA, flash memory, and MAX V CPLD 5M2210 System Controller device programming methods supported by the Arria V GX starter board.

The Arria V GX starter board supports the following three configuration methods:

- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- External USB-Blaster for configuring the FPGA using an external USB-Blaster that connects to the JTAG programming header.
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or pressing the PGM_CONFIG push button (S1).

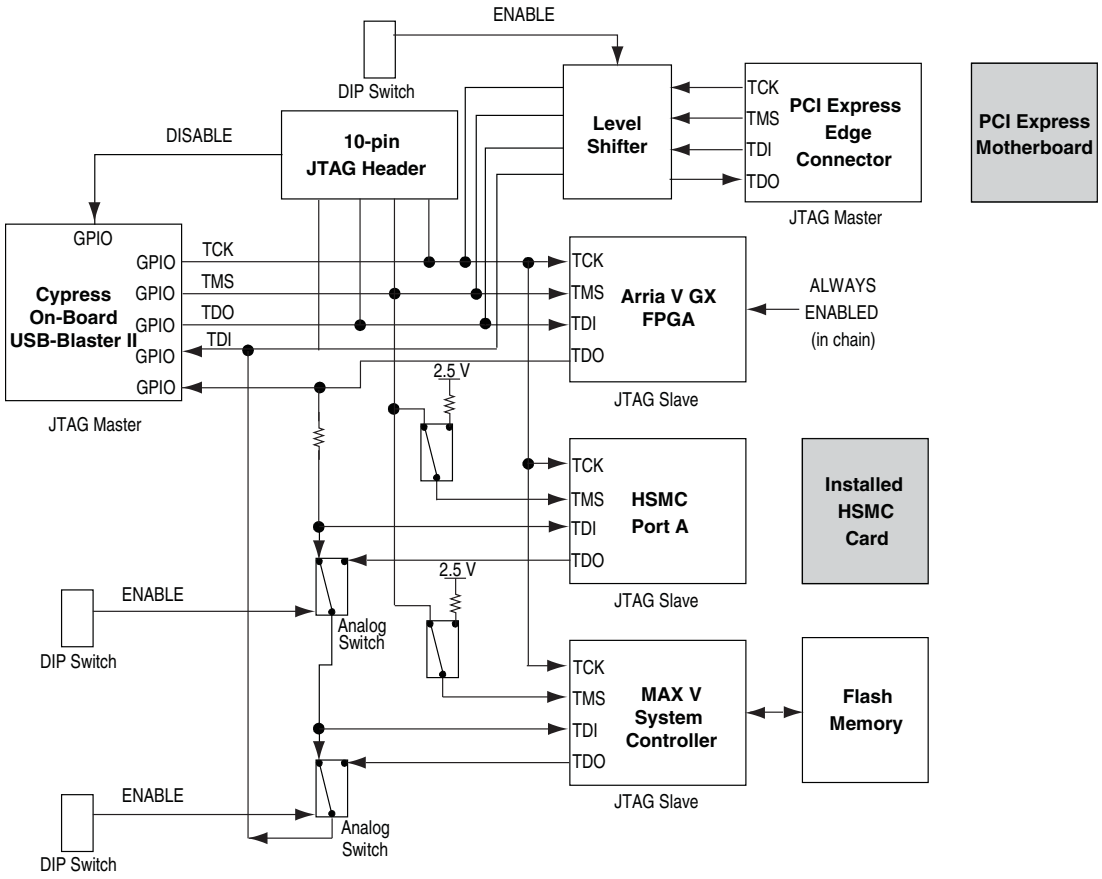
FPGA Programming over Embedded USB-Blaster

This configuration method implements a USB Type-B connector (J14), a USB 2.0 PHY device (U23), and an Altera MAX II CPLD EPM570F100C5N (U21) to allow FPGA configuration using a USB cable. This USB cable connects directly between the USB port on the board and a USB port of a PC running the Quartus II software.

The embedded USB-Blaster in the MAX II CPLD EPM570F100C5N normally masters the JTAG chain. To prevent contention between the JTAG masters, the embedded USB-Blaster is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG connector.

Figure 2–5 illustrates the JTAG chain.

Figure 2–5. JTAG Chain



The JTAG DIP switch (SW2) controls the jumpers shown in Figure 2–5. To connect a device or interface in the chain, their corresponding switch must be in the OFF position. Slide all the switches in the ON position to only have the FPGA in the chain.

The MAX V CPLD 5M2210 System Controller must be in the chain to use some of the GUI interfaces.

Flash Memory Programming

Flash memory programming is possible through a variety of methods.

The default method is to use the factory design—Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

FPGA Programming from Flash Memory

On either power-up or by pressing the program configuration push button, PGM_CONFIG (S1), the MAX V CPLD 5M2210 System Controller's PFL configures the FPGA from the flash memory. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 16-bit data is then written to the dedicated configuration pins in the FPGA during configuration.

Pressing the PGM_CONFIG push button (S1) loads the FPGA with a hardware page based on which PGM_LED[2:0] LED (D11, D12, D13) illuminates.

Table 2–7 defines the design that loads when you press the PGM_CONFIG push button.

Table 2–7. PGM_LED Settings *(1)*

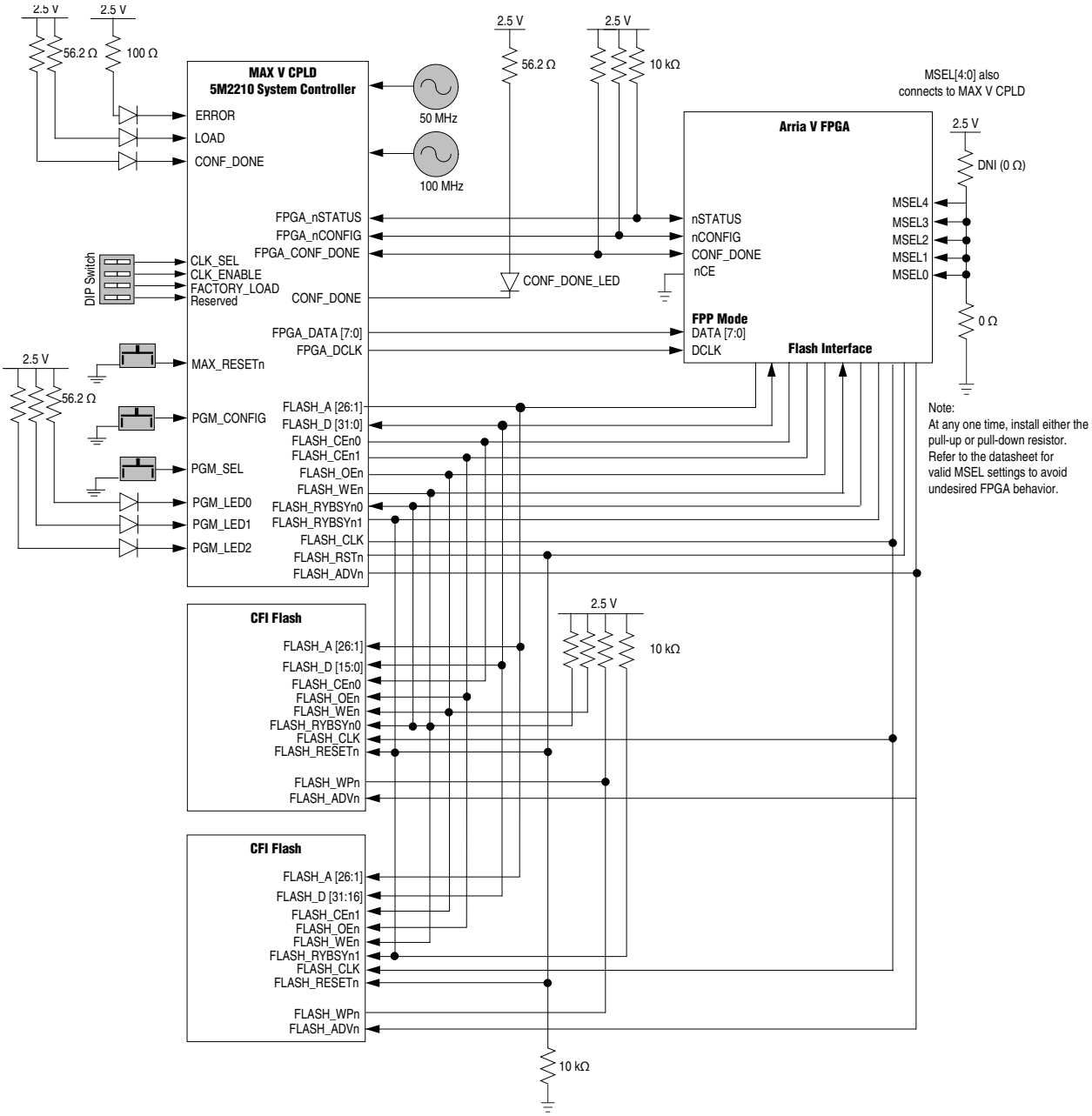
PGM_LED0	PGM_LED1	PGM_LED2	Design
ON	OFF	OFF	Factory
OFF	ON	OFF	User design 1
OFF	OFF	ON	User design 2

Note to Table 2–7:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Figure 2–6 shows the PFL configuration.

Figure 2–6. PFL Configuration



For information about the flash memory map storage, refer to the *Arria V GX Starter Kit User Guide*.

FPGA Programming over External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG header (J9).

For more information on the following topics, refer to the respective documents:

- Board Update Portal and PFL design, refer to the *Arria V GX Starter Kit User Guide*.
- PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide.*

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–8 lists the LED board references, names, and functional descriptions.

Table 2–8. Board-Specific LEDs (Part 1 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Description
D30	Power	5.0-V	Blue LED. Illuminates when 5.0 V power is active.
D12	MAX_CONF_DONEn	2.5-V	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX V CPLD 5M2210 System Controller.
D11	MAX_LOAD	2.5-V	Green LED. Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D10	MAX_ERROR	2.5-V	Red LED. Illuminates when the MAX V CPLD 5M2210 System Controller fails to configure the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D24 D25 D26	PGM_LED[0] PGM_LED[1] PGM_LED[2]	2.5-V	Green LEDs. Illuminates to indicate which hardware page loads from flash memory when you press the PGM_SEL push button.
D6, D7 D8, D9	JTAG_RX, JTAG_TX SC_RX, SC_TX	2.5-V	Green LEDs. Illuminates to indicate USB-Blaster II receive and transmit activities.
D2	ENET_LED_TX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D3	ENET_LED_RX	2.5-V	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.
D33	ENET_LED_LINK10	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D5	ENET_LED_LINK100	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D4	ENET_LED_LINK1000	2.5-V	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.

Table 2–8. Board-Specific LEDs (Part 2 of 2)

Board Reference	Schematic Signal Name	I/O Standard	Description
D1	SDI_RX_CDn	3.3-V	Green LED. Illuminates to indicate that input signal is detected at the SDI RX port. Driven by the SDI cable equalizer.
D15	HSMA_PRSNTn	3.3-V	Green LED. Illuminates when HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.

Table 2–9 lists the board-specific LEDs component references and manufacturing information.

Table 2–9. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D1 – D9, D11 – D15, D24 – D26, D33	Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
D10	Red LED	Lumex Inc.	SML-LXT0805IW-TR	www.lumex.com
D30	Blue LED	Lumex Inc.	SML-LX0805USBC-TR	www.lumex.com

Setup Elements

The starter board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG settings DIP switch
- PCI Express control DIP switch
- CPU reset push button
- MAX V reset push button
- Image load push button
- Image select push button

Table 2–10 lists the switch and push button component references and manufacturing information.

Table 2–10. Switch and Push Button Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW1, SW2, SW4	Four-position DIP switch	C&K Components/ ITT Industries	TDA04H0SB1	www.ittcannon.com
S1–S4	Push button	Panasonic	EVQPAC07K	www.panasonic.com

Board Settings DIP Switch

The board settings DIP switch (SW4) controls various features specific to the board and the MAX V CPLD 5M2210 System Controller logic design. Table 2–11 lists the switch controls and descriptions.

Table 2–11. Board Settings DIP Switch Controls

Switch	Schematic Signal Name	Description	Default
1	CLK_SEL	ON: Select SMA input clock OFF: Select programmable oscillator clock	OFF
2	CLK_EN	ON: Disable On-board oscillator OFF: Enable On-board oscillator	OFF
3	FACTORY_LOAD	ON: Load the user design from flash at power up. OFF: Load the factory design from flash for Arria V at power up.	OFF
4	SECURITY	Reserved for future use.	OFF

JTAG Chain Control DIP Switch

The JTAG chain control DIP switch (SW2) either remove or include devices in the active JTAG chain. The Arria V GX is always in the JTAG chain. Table 2–12 lists the switch controls and its descriptions.

Table 2–12. JTAG Chain Control Switch

Switch	Schematic Signal Name	Description	Default
1	5M2210_JTAG_EN	ON : Bypass MAX V CPLD 5M2210 System Controller OFF : MAX V CPLD 5M2210 System Controller in-chain	OFF
2	HSMA_JTAG_EN	ON : Bypass HSMA OFF : HSMA in-chain	ON
3	PCIE_JTAG_EN	ON : Bypass PCI Express edge connector OFF : PCI Express edge connector in-chain	ON
4	NC	Not used	ON

PCI Express Link Width DIP Switch

The PCI Express link width DIP switch (SW1) enable or disable different link width configurations. Table 2–13 lists the switch controls and descriptions.

Table 2–13. PCI Express Link Width DIP Switch Controls (Part 1 of 2)

Switch	Schematic Signal Name	Description	Default
1	PCIE_PRSNT2n_x1	ON : Enable x1 presence detect OFF : Disable x1 presence detect	ON
2	PCIE_PRSNT2n_x4	ON : Enable x4 presence detect OFF : Disable x4 presence detect	ON

Table 2–13. PCI Express Link Width DIP Switch Controls (Part 2 of 2)

Switch	Schematic Signal Name	Description	Default
3	PCIE_PRSNT2n_x8	ON : Enable x8 presence detect OFF : Disable x8 presence detect	ON
4	FAN_FORCE_ON	ON : Enable fan OFF : Disable fan	OFF

CPU Reset Push Button

The CPU reset push button, CPU_RESETn (S4), is an input to the Arria V GX DEV_CLRn pin and is an open-drain I/O from the MAX V CPLD System Controller. This push button is the default reset for both the FPGA and CPLD logic. The MAX V CPLD 5M2210 System Controller also drives this push button during power-on-reset (POR).

MAX V Reset Push Button

The MAX V reset push button, MAX_RESETn (S3), is an input to the MAX V CPLD 5M2210 System Controller. This push button is the default reset for the CPLD logic.

Image Load Push Button

The image load push button, PGM_CONFIG (S1), is an input to the MAX V CPLD 5M2210 System Controller. This input forces a FPGA reconfiguration from the flash memory. The location in the flash memory is based on the settings of PGM_LED[2:0], which is controlled by the image select push button, PGM_SEL. Valid settings include PGM_LED0, PGM_LED1, or PGM_LED2 on the three pages in flash memory reserved for FPGA designs.

Image Select Push Button

The program select push button, PGM_SEL (S2), is an input to the MAX V CPLD System Controller. This push button toggles the PGM_LED[2:0]sequence that selects which location in the flash memory is used to configure the FPGA. Refer to Table 2–7 for the PGM_LED[2:0] sequence definitions.

Clock Circuitry

This section describes the board's clock inputs and outputs.

On-Board Oscillators

The starter board includes programmable oscillators with a frequency of 100-MHz, 125-MHz, 156.25-MHz, and 409.60-MHz.

Figure 2–7 shows the default frequencies of all external clocks going to the Arria V GX starter board.

Figure 2–7. Arria V GX Starter Board Clocks

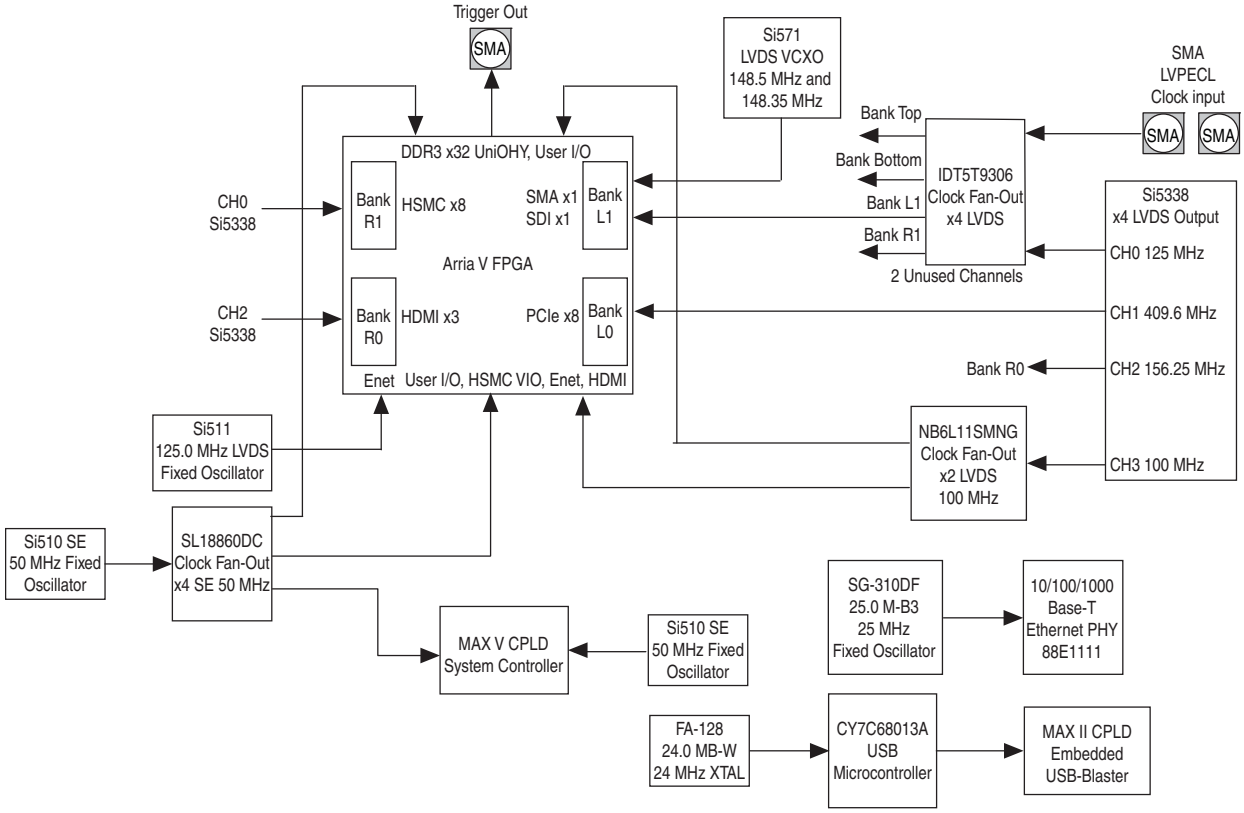


Table 2–14 lists the oscillators, its I/O standard, and voltages required for the starter board.

Table 2–14. On-Board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Arria V GX Pin Number	Application
X4	CLKIN_50_TOP	50.000 MHz	2.5V CMOS	A16	Nios II and MAX V
	CLKIN_50_BOT			AP29	
	CLKIN_50_MAXV			—	
X3	CLLK_CONFIG	100.000 MHz	2.5V CMOS	—	Fast FPGA configuration

Table 2–14. On-Board Oscillators

Source	Schematic Signal Name	Frequency	I/O Standard	Arria V GX Pin Number	Application
U5	REFCLK2_QL1_P	125.000 MHz	LVDS (fanout buffer)	U26	Left transceiver bank
	REFCLK2_QL1_N			U27	
	CLKINBOT_125_P			AP32	Bottom edge
	CLKINBOT_125_N			AP31	
	CLKINTOP_125_P			A3	Top edge
	CLKINTOP_125_N			B3	
	REFCLK2_QR1_P			U9	HSMC port A
	REFCLK2_QR1_N			U8	
X2	CLK_125_P	125.000 MHz	LVDS	AH17	10/100/1000 Ethernet
	CLK_125_N			AG17	
X1	CLK_148_P	148.500 MHz	LVDS	R26	HD-SDI video
	CLK_148_N			R27	
U4	Si5338A_CLK0_125_P	125.000 MHz	LVDS (fanout buffer)	—	LVDS fanout buffer
	Si5338A_CLK0_125_N			—	
	REFCLK1_QL0_P	409.600 MHz	LVDS	W26	SMA
	REFCLK1_QL0_N			W27	
	REFCLK1_QR0_P	156.250 MHz	LVDS	W9	HSMC port A
	REFCLK1_QR0_N			W8	
	Si5338A_CLK3_100_P	100.000 MHz	LVDS (fanout buffer)	—	LVDS fanout buffer
	Si5338A_CLK3_100_N			—	
U3	CLKINTOP_100_P	100.000 MHz	LVDS	A19	Top edge—DDR3
	CLKINTOP_100_N			A20	
	CLKINBOT_100_P		LVDS	AH18	Bottom edge
	CLKINBOT_100_N			AG18	

Off-Board Clock Input/Output

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 2–15 lists the clock inputs for the starter board.

Table 2–15. Off-Board Clock Inputs

Source	Schematic Signal Name	I/O Standard	Arria V GX Pin Number	Description
SMA	CLKIN_SMA_P	LVPECL	—	Input to LVDS fan-out buffer (drives one REFCLK)
	CLKIN_SMA_N	LVPECL	—	
Samtec HSMC	HSMA_CLK_IN0	2.5-V	AL5	Single-ended input from the installed HSMC cable or board.
Samtec HSMC	HSMA_CLK_IN_P1	LVDS/2.5-V	AN3	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N1	LVDS/LVTTL	AP2	
Samtec HSMC	HSMA_CLK_IN_P2	LVDS/LVTTL	C1	LVDS input from the installed HSMC cable or board. Can also support 2x LVTTL inputs.
	HSMA_CLK_IN_N2	LVDS/LVTTL	C2	
Samtec HSMC	REFCLK3_QR1_P	LVDS	R9	LVDS input from the installed HSMC cable or board.
	REFCLK3_QR1_N	HCSL	R8	
PCI Express Edge	PCIE_REFCLK_P	LVDS	AA27	LVDS input from the PCI Express edge connector.
	PCIE_REFCLK_N	HCSL	AA28	

Table 2–16 lists the clock outputs for the starter board.

Table 2–16. Off-Board Clock Outputs

Source	Schematic Signal Name	I/O Standard	Arria V GX Pin Number	Description
Samtec HSMC	HSMA_CLK_OUT0	2.5V CMOS	AL6	FPGA CMOS output (or GPIO)
Samtec HSMC	HSMA_CLK_OUT_P1	LVDS/2.5V CMOS	AD8	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N1	LVDS/2.5V CMOS	AC8	
Samtec HSMC	HSMA_CLK_OUT_P2	LVDS/2.5V CMOS	L9	LVDS output. Can also support 2x CMOS outputs.
	HSMA_CLK_OUT_N2	LVDS/2.5V CMOS	M8	
SMA	CLKOUT_SMA	2.5V CMOS	C3	FPGA CMOS output (or GPIO)

Table 2–17 lists the crystal oscillators component references and manufacturing information.

Table 2–17. Crystal Oscillator Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U4	Programmable LVDS quad-clock 125M, 409.6M, 156.25M, 100M defaults	Silicon Labs	Si5338A-A01343-GM	www.silabs.com
X1	148.50 MHz LVDS voltage controlled crystal oscillator	Silicon Labs	571FDB000159DG	www.silabs.com

Table 2–17. Crystal Oscillator Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
X3	100 MHz crystal oscillator, ±50 ppm, CMOS, 2.5 V	Silicon Labs	510GBA100M000BAGx	www.silabs.com
X4	50 MHz crystal oscillator, ±50 ppm, CMOS, 2.5 V	Silicon Labs	510GBA50M0000BAGx	www.silabs.com
X2	125 MHz crystal oscillator, ±50 ppm, LVDS, 2.5 V	Silicon Labs	511FBA125M000BAGx	www.silabs.com

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push buttons, DIP switches, LEDs, and character LCD.

User-Defined Push Buttons

The starter board includes three user-defined push buttons. For information on the system and safe reset push buttons, refer to "Setup Elements" on page 2–17.

Board references S5, S6, and S7 are push buttons that allow you to interact with the Arria V GX. When you press and hold down the switch, the device pin is set to logic 0; when you release the switch, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 2–18 lists the user-defined push button schematic signal names and their corresponding Arria V GX device pin numbers.

Table 2–18. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
S5	USER_PB0	A14	2.5-V	User-defined push buttons
S6	USER_PB1	B15	2.5-V	
S7	USER_PB2	B14	2.5-V	

Table 2–19 lists the user-defined push button component reference and the manufacturing information.

Table 2–19. User-Defined Push Button Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S5 to S7	Push button	Dawning Precision Co.	TS-A02SA-2-S100	www.dawning2.com.tw

User-Defined DIP Switch

Board reference SW3 is a four-pin DIP switch. This switch is user-defined and provides additional FPGA input control. There are no board-specific functions for this switch.

Table 2–20 lists the user-defined DIP switch schematic signal names and their corresponding Arria V GX pin numbers.

Table 2–20. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference (SW3)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
1	USER_DIPSW0	D15	2.5-V	User-defined DIP switch that connects to the FPGA. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected.
2	USER_DIPSW1	D14	2.5-V	
3	USER_DIPSW2	D13	2.5-V	
4	USER_DIPSW3	E15	2.5-V	

Table 2–21 lists the user-defined DIP switch component reference and the manufacturing information.

Table 2–21. User-Defined DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW3	Four-position DIP switch	C&K Components/ ITT Industries	TDA04H0SB1	www.ittcannon.com

User-Defined LEDs

The starter board includes general and HSMC user-defined LEDs. This section describes all user-defined LEDs. For information on board specific or status LEDs, refer to "Status Elements" on page 2–16.

General LEDs

Board references D20 through D23 are four user-defined LEDs. The status and debugging signals are driven to the LEDs from the designs loaded into the Arria V GX. There are no board-specific functions for these LEDs.

Table 2–22 lists the general LED schematic signal names and their corresponding Arria V GX pin numbers.

Table 2–22. General LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
D20	USER_LED0	C16	2.5-V	User-defined LEDs. Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.
D21	USER_LED1	C14	2.5-V	
D22	USER_LED2	C13	2.5-V	
D23	USER_LED3	D16	2.5-V	

Table 2–23 lists the general LED component reference and the manufacturing information.

Table 2–23. General LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D20 to D23	Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com

HSMC LEDs

Each HSMC port has two LEDs located nearby. There are no board-specific functions for the HSMC LEDs. The LEDs are labeled TX and RX, and are intended to display data flow to and from the connected HSMC daughtercards. The LEDs are driven by the Arria V GX.

Table 2–24 lists the HSMC LED schematic signal names and their corresponding Arria V GX pin numbers.

Table 2–24. HSMC LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
D13	HSMA_RX_LED	D8	2.5-V	User-defined LEDs. Labeled RX for HSMC port A.
D14	HSMA_TX_LED	D9	2.5-V	User-defined LEDs. Labeled TX for HSMC port A.

Table 2–25 lists the HSMC LED component reference and the manufacturing information.

Table 2–25. HSMC LED Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D13, D14	Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com

PCI Express LEDs

Board references D16 through D19 are four PCI Express LEDs for link width indication. There are no board-specific functions for the PCI Express LEDs. You can configure the LEDs to display the functions as listed in Table 2–26. The LEDs are driven by the Arria V GX.

Table 2–26 lists the PCI Express LED schematic signal names and their corresponding Arria V GX GX pin numbers.

Table 2–26. PCI Express LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
D16	PCIE_LED_X1	G17	2.5-V	Green LED. Configure this LED to display the PCI Express link width x1.
D17	PCIE_LED_X4	G16	2.5-V	Green LED. Configure this LED to display the PCI Express link width x4.

Table 2–26. PCI Express LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
D18	PCIE_LED_X8	G15	2.5-V	Green LED. Configure this LED to display the PCI Express link width x8.
D19	PCIE_LED_G2	F17	2.5-V	Green LED. Configure this LED to display the PCI Express Gen2 link.

Table 2–25 lists the PCI Express LED component reference and the manufacturing information.

Table 2–27. PCI Express LED Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D16 to D19	Yellow LEDs	Lumex Inc.	SML-LXT0805YW-TR	www.lumex.com

Character LCD

The starter board includes a single 14-pin 0.1" pitch dual-row header that interfaces to a 16 character × 2 line Lumex character LCD display. The character LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 2–28 summarizes the character LCD pin assignments. The signal names and directions are relative to the Arria V GX.

Table 2–28. Character LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J16)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
7	LCD_DATA0	C19	2.5-V	LCD data bus
8	LCD_DATA1	D19	2.5-V	LCD data bus
9	LCD_DATA2	D18	2.5-V	LCD data bus
10	LCD_DATA3	D17	2.5-V	LCD data bus
11	LCD_DATA4	E17	2.5-V	LCD data bus
12	LCD_DATA5	G19	2.5-V	LCD data bus
13	LCD_DATA6	E18	2.5-V	LCD data bus
14	LCD_DATA7	F19	2.5-V	LCD data bus
4	LCD_D_Cn	B18	2.5-V	LCD data or command select
5	LCD_WEn	C17	2.5-V	LCD write enable
6	LCD_CSn	B17	2.5-V	LCD chip select

Table 2–29 lists the LCD pin definitions, and is an excerpt from Lumex data sheet.

Table 2–29. LCD Pin Definitions and Functions

Pin Number	Symbol	Level	Function	
1	V_{DD}	—	Power supply	5 V
2	V_{SS}	—		GND (0 V)
3	V_0	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)	
6	E	H, H to L	Enable	
7–14	DB0–DB7	H/L	Data bus—software selectable 4-bit or 8-bit mode	

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Table 2–30 lists the LCD component references and the manufacturing information.

Table 2–30. LCD Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J16	2×7 pin, 100 mil, vertical header	Samtec	TSM-107-07-G-D	www.samtec.com
	2×16 character display, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com

Components and Interfaces

This section describes the starter board's communication ports and interface cards relative to the Arria V GX. The development board supports the following communication ports:

- PCI Express
- 10/100/1000 Ethernet
- HSMC
- SDI video output/input
- HDMI video output

PCI Express

The Arria V GX starter board is designed to fit entirely into a PC motherboard with a ×8 PCI Express slot that can accommodate a full height long form factor add-in card. This interface uses the Arria V GX's PCI Express hard IP block, saving logic resources for the user logic application.

For more information on using the PCI Express hard IP block, refer to the *PCI Express Compiler User Guide*.

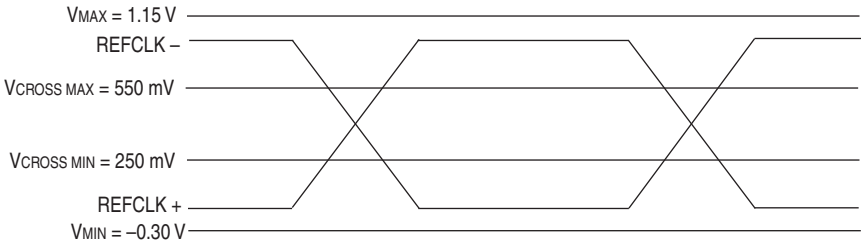
The PCI Express edge connector has a connection speed of 2.5 Gbps/lane for a maximum of 20 Gbps full-duplex (Gen1) or 5.0 Gbps/lane for a maximum of 40 Gbps full-duplex (Gen2).

The power for the board can be sourced entirely from the PCI Express edge connector when installed into a PC motherboard. Although the board can also be powered by a laptop power supply for use on a lab bench, it is not recommended to power from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The `PCIE_REFCLK_P/N` signal is a 100 MHz differential input that is driven from the PC motherboard on to this board through the edge connector. This signal connects directly to a Arria V GX `REFCLK` input pin pair using DC coupling. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

Figure 2–8 shows the PCI Express reference clock levels.

Figure 2–8. PCI Express Reference Clock Levels



The JTAG and SMB are optional signals in the PCI Express specification. Both types of signals are wired to the Arria V GX but are not required for normal operation. The PCI Express control DIP switch allows the presence detect grounding to be altered to enable a ×1, ×4, or ×8 width edge connector. The PCI Express control DIP switch does not support auto-negotiation.

The PCI express edge connector has a presence detect feature to allow the motherboard to determine if a card is installed. A DIP switch provides an option to connect the `PRSNT1n` pin to any of the three `PRSNT2n` pins found within the ×8 connector definition. This is to address issues on some PC systems that would base the link width capability on the presence detect pins versus a query operation.

Table 2–31 summarizes the PCI Express pin assignments. The signal names and directions are relative to the Arria V GX.

Table 2–31. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J1)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
A5	PCIE_JTAG_TCK	—	LVTTL	JTAG chain clock
A6	PCIE_JTAG_TDI	—	LVTTL	JTAG chain data in
A7	PCIE_JTAG_TDO	—	LVTTL	JTAG chain data out
A8	PCIE_JTAG_TMS	—	LVTTL	JTAG chain mode select
A11	PCIE_PERSTN	B2	LVTTL	Reset
A1	PCIE_PRSNT1N	—	LVTTL	Link width DIP switch
B17	PCIE_PRSNT2N_X1	—	LVTTL	Link width DIP switch
B31	PCIE_PRSNT2N_X4	—	LVTTL	Link width DIP switch
B48	PCIE_PRSNT2N_X8	—	LVTTL	Link width DIP switch
A13	PCIE_REFCLK_P	AA27	HCSL	Motherboard reference clock
A14	PCIE_REFCLK_N	AA28	HCSL	Motherboard reference clock
B14	PCIE_RX_P0	AK34	1.5-V PCML	Receive bus
B15	PCIE_RX_N0	AK33	1.5-V PCML	Receive bus
B19	PCIE_RX_P1	AH34	1.5-V PCML	Receive bus
B20	PCIE_RX_N1	AH33	1.5-V PCML	Receive bus
B23	PCIE_RX_P2	AF34	1.5-V PCML	Receive bus
B24	PCIE_RX_N2	AF33	1.5-V PCML	Receive bus
B27	PCIE_RX_P3	AD34	1.5-V PCML	Receive bus
B28	PCIE_RX_N3	AD33	1.5-V PCML	Receive bus
B33	PCIE_RX_P4	Y34	1.5-V PCML	Receive bus
B34	PCIE_RX_N4	Y33	1.5-V PCML	Receive bus
B37	PCIE_RX_P5	V34	1.5-V PCML	Receive bus
B38	PCIE_RX_N5	V33	1.5-V PCML	Receive bus
B41	PCIE_RX_P6	T34	1.5-V PCML	Receive bus
B42	PCIE_RX_N6	T33	1.5-V PCML	Receive bus
B45	PCIE_RX_P7	P34	1.5-V PCML	Receive bus
B46	PCIE_RX_N7	P33	1.5-V PCML	Receive bus
B5	PCIE_SMBCLK	F16	2.5-V	SMB clock
B6	PCIE_SMBDAT	F14	2.5-V	SMB data
A16	PCIE_TX_CP0	AJ32	1.5-V PCML	Transmit bus
A17	PCIE_TX_CN0	AJ31	1.5-V PCML	Transmit bus
A21	PCIE_TX_CP1	AG32	1.5-V PCML	Transmit bus
A22	PCIE_TX_CN1	AG31	1.5-V PCML	Transmit bus
A25	PCIE_TX_CP2	AE32	1.5-V PCML	Transmit bus
A26	PCIE_TX_CN2	AE31	1.5-V PCML	Transmit bus
A29	PCIE_TX_CP3	AC32	1.5-V PCML	Transmit bus

Table 2–31. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J1)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
A30	PCIE_TX_CN3	AC31	1.5-V PCML	Transmit bus
A35	PCIE_TX_CP4	W32	1.5-V PCML	Transmit bus
A36	PCIE_TX_CN4	W31	1.5-V PCML	Transmit bus
A39	PCIE_TX_CP5	U32	1.5-V PCML	Transmit bus
A40	PCIE_TX_CN5	U31	1.5-V PCML	Transmit bus
A43	PCIE_TX_CP6	R32	1.5-V PCML	Transmit bus
A44	PCIE_TX_CN6	R31	1.5-V PCML	Transmit bus
A47	PCIE_TX_CP7	N32	1.5-V PCML	Transmit bus
A48	PCIE_TX_CN7	N31	1.5-V PCML	Transmit bus
B11	PCIE_WAKEN	E14	2.5-V	Wake signal

10/100/1000 Ethernet

The starter board supports 10/100/1000 base-T Ethernet using an external Marvell 88E1111 PHY and Altera Triple-Speed Ethernet MegaCore MAC function. The PHY-to-MAC interface employs a RGMII interface to the Arria V GX. The MAC function must be provided in the FPGA for typical networking applications.

The Marvell 88E1111 PHY uses 2.5-V and 1.0-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. The PHY interfaces to a Wurth Elektronik model RJ45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–9 shows the RGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–9. RGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

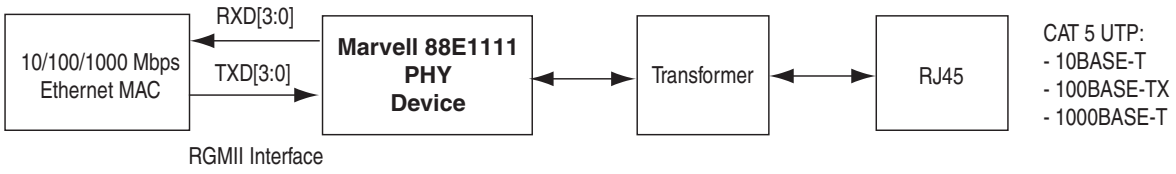


Table 2–32 lists the Ethernet PHY interface pin assignments.

Table 2–32. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference (U20)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
23	ENET_INTN	AG11	2.5-V CMOS	Management bus interrupt
25	ENET_MDC	AJ11	2.5-V CMOS	Management bus data clock
24	ENET_MDIO	AH11	2.5-V CMOS	Management bus data
28	ENET_RESETN	AL11	2.5-V CMOS	Device reset
2	ENET_RX_CLK	AL4	2.5-V CMOS	RGMII receive clock

Table 2–32. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference (U20)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
95	ENET_RX_D0	AF11	2.5-V CMOS	RGMII receive data
92	ENET_RX_D1	AF13	2.5-V CMOS	RGMII receive data
93	ENET_RX_D2	AE12	2.5-V CMOS	RGMII receive data
91	ENET_RX_D3	AE13	2.5-V CMOS	RGMII receive data
94	ENET_RX_DV	AB13	2.5-V CMOS	RGMII receive data valid
77	ENET_RX_P	AP14	LVDS	SGMII receive channel
75	ENET_RX_N	AN14	LVDS	SGMII receive channel
11	ENET_TX_D0	AC11	2.5-V CMOS	RGMII transmit data
12	ENET_TX_D1	AC12	2.5-V CMOS	RGMII transmit data
14	ENET_TX_D2	AC13	2.5-V CMOS	RGMII transmit data
16	ENET_TX_D3	AB11	2.5-V CMOS	RGMII transmit data
9	ENET_TX_EN	AB12	2.5-V CMOS	RGMII transmit enable
8	ENET_GTX_CLK	AD12	2.5-V CMOS	RGMII transmit clock
82	ENET_TX_P	AP13	LVDS	SGMII transmit channel
81	ENET_TX_N	AN12	LVDS	SGMII transmit channel

Table 2–33 lists the Ethernet PHY interface component reference and manufacturing information.

Table 2–33. Ethernet PHY Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U20	Ethernet PHY BASE-T device	Marvell Semiconductor	88E1111-B2-CAA1C000	www.marvell.com
J19	RJ-45 connector,10/100/1000 Mbps	Wurth Elektronik	7499111001A	www.we-online.com

HSMC

The starter board contains a HSMC interface (Port A). This physical interface provides eight channels of 6.5536 Gbps-capable transceivers. The HSMC interface also supports a full SPI4.2 interface (17 LVDS channels), three input and output clocks, as well as JTAG and SMB signals. The LVDS channels can be used for CMOS signaling or LVDS.

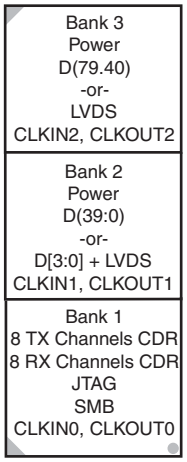
The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of daughtercards (HSMCs).

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

Figure 2–10 shows the bank arrangement of signals with respect to the Samtec connector's three banks.

Figure 2–10. HSMC Signal and Bank Diagram



The HSMC interface has programmable bidirectional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels.

As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–34 lists the HSMC port A interface pin assignments, signal names, and functions.

Table 2–34. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference (J13)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
1	HSMA_TX_P7	AA3	1.5-V PCML	Transceiver TX bit 7
2	HSMA_RX_P7	AB1	1.5-V PCML	Transceiver RX bit 7
3	HSMA_TX_N7	AA4	1.5-V PCML	Transceiver TX bit 7n
4	HSMA_RX_N7	AB2	1.5-V PCML	Transceiver RX bit 7n
5	HSMA_TX_P6	W3	1.5-V PCML	Transceiver TX bit 6
6	HSMA_RX_P6	Y1	1.5-V PCML	Transceiver RX bit 6
7	HSMA_TX_N6	W4	1.5-V PCML	Transceiver TX bit 6n

Table 2–34. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference (J13)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
8	HSMA_RX_N6	Y2	1.5-V PCML	Transceiver RX bit 6n
9	HSMA_TX_P5	U3	1.5-V PCML	Transceiver TX bit 5
10	HSMA_RX_P5	V1	1.5-V PCML	Transceiver RX bit 5
11	HSMA_TX_N5	U4	1.5-V PCML	Transceiver TX bit 5n
12	HSMA_RX_N5	V2	1.5-V PCML	Transceiver RX bit 5n
13	HSMA_TX_P4	R3	1.5-V PCML	Transceiver TX bit 4
14	HSMA_RX_P4	T1	1.5-V PCML	Transceiver RX bit 4
15	HSMA_TX_N4	R4	1.5-V PCML	Transceiver TX bit 4n
16	HSMA_RX_N4	T2	1.5-V PCML	Transceiver RX bit 4n
17	HSMA_TX_P3	N3	1.5-V PCML	Transceiver TX bit 3
18	HSMA_RX_P3	P1	1.5-V PCML	Transceiver RX bit 3
19	HSMA_TX_N3	N4	1.5-V PCML	Transceiver TX bit 3n
20	HSMA_RX_N3	P2	1.5-V PCML	Transceiver RX bit 3n
21	HSMA_TX_P2	L3	1.5-V PCML	Transceiver TX bit 2
22	HSMA_RX_P2	M1	1.5-V PCML	Transceiver RX bit 2
23	HSMA_TX_N2	L4	1.5-V PCML	Transceiver TX bit 2n
24	HSMA_RX_N2	M2	1.5-V PCML	Transceiver RX bit 2n
25	HSMA_TX_P1	J3	1.5-V PCML	Transceiver TX bit 1
26	HSMA_RX_P1	K1	1.5-V PCML	Transceiver RX bit 1
27	HSMA_TX_N1	J4	1.5-V PCML	Transceiver TX bit 1n
28	HSMA_RX_N1	K2	1.5-V PCML	Transceiver RX bit 1n
29	HSMA_TX_P0	G3	1.5-V PCML	Transceiver TX bit 0
30	HSMA_RX_P0	H1	1.5-V PCML	Transceiver RX bit 0
31	HSMA_TX_N0	G4	1.5-V PCML	Transceiver TX bit 0n
32	HSMA_RX_N0	H2	1.5-V PCML	Transceiver RX bit 0n
33	HSMA_SDA	AK8	2.5-V CMOS	Management serial data
34	HSMA_SCL	AJ8	2.5-V CMOS	Management serial clock
35	JTAG_TCK	AN32	2.5-V CMOS	JTAG clock signal
36	HSMA_JTAG_TMS	—	2.5-V CMOS	JTAG mode select signal
37	HSMA_JTAG_TDO	—	2.5-V CMOS	JTAG data output
38	JTAG_FPGA_TDO_RETIMER	—	2.5-V CMOS	JTAG data input
39	HSMA_CLK_OUT0	AL6	2.5-V CMOS	Dedicated CMOS clock out
40	HSMA_CLK_IN0	AL5	2.5-V CMOS	Dedicated CMOS clock in
41	HSMA_D0	AJ10	2.5-V CMOS	Dedicated CMOS I/O bit 0
42	HSMA_D1	AH10	2.5-V CMOS	Dedicated CMOS I/O bit 1
43	HSMA_D2	AH9	2.5-V CMOS	Dedicated CMOS I/O bit 2
44	HSMA_D3	AH8	2.5-V CMOS	Dedicated CMOS I/O bit 3
47	HSMA_TX_D_P0	AM10	LVDS or 2.5-V	LVDS TX bit 0 or CMOS bit 4
48	HSMA_RX_D_P0	AP11	LVDS or 2.5-V	LVDS RX bit 0 or CMOS bit 5

Table 2–34. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference (J13)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
49	HSMA_TX_D_N0	AL10	LVDS or 2.5-V	LVDS TX bit 0n or CMOS bit 6
50	HSMA_RX_D_N0	AP10	LVDS or 2.5-V	LVDS RX bit 0n or CMOS bit 7
53	HSMA_TX_D_P1	AL9	LVDS or 2.5-V	LVDS TX bit 1 or CMOS bit 8
54	HSMA_RX_D_P1	AN8	LVDS or 2.5-V	LVDS RX bit 1 or CMOS bit 9
55	HSMA_TX_D_N1	AK9	LVDS or 2.5-V	LVDS TX bit 1n or CMOS bit 10
56	HSMA_RX_D_N1	AN9	LVDS or 2.5-V	LVDS RX bit 1n or CMOS bit 11
59	HSMA_TX_D_P2	AF10	LVDS or 2.5-V	LVDS TX bit 2 or CMOS bit 12
60	HSMA_RX_D_P2	AM8	LVDS or 2.5-V	LVDS RX bit 2 or CMOS bit 13
61	HSMA_TX_D_N2	AE10	LVDS or 2.5-V	LVDS TX bit 2n or CMOS bit 14
62	HSMA_RX_D_N2	AL8	LVDS or 2.5-V	LVDS RX bit 2n or CMOS bit 15
65	HSMA_TX_D_P3	AE9	LVDS or 2.5-V	LVDS TX bit 3 or CMOS bit 16
66	HSMA_RX_D_P3	AN11	LVDS or 2.5-V	LVDS RX bit 3 or CMOS bit 17
67	HSMA_TX_D_N3	AD9	LVDS or 2.5-V	LVDS TX bit 3n or CMOS bit 18
68	HSMA_RX_D_N3	AM11	LVDS or 2.5-V	LVDS RX bit 3n or CMOS bit 19
71	HSMA_TX_D_P4	AJ6	LVDS or 2.5-V	LVDS TX bit 4 or CMOS bit 20
72	HSMA_RX_D_P4	AL12	LVDS or 2.5-V	LVDS RX bit 4 or CMOS bit 21
73	HSMA_TX_D_N4	AH6	LVDS or 2.5-V	LVDS TX bit 4n or CMOS bit 22
74	HSMA_RX_D_N4	AK12	LVDS or 2.5-V	LVDS RX bit 4n or CMOS bit 23
77	HSMA_TX_D_P5	AC6	LVDS or 2.5-V	LVDS TX bit 5 or CMOS bit 24
78	HSMA_RX_D_P5	AM13	LVDS or 2.5-V	LVDS RX bit 5 or CMOS bit 25
79	HSMA_TX_D_N5	AC7	LVDS or 2.5-V	LVDS TX bit 5n or CMOS bit 26
80	HSMA_RX_D_N5	AL13	LVDS or 2.5-V	LVDS RX bit 5n or CMOS bit 27
83	HSMA_TX_D_P6	AM4	LVDS or 2.5-V	LVDS TX bit 6 or CMOS bit 28
84	HSMA_RX_D_P6	AH12	LVDS or 2.5-V	LVDS RX bit 6 or CMOS bit 29
85	HSMA_TX_D_N6	AM3	LVDS or 2.5-V	LVDS TX bit 6n or CMOS bit 30
86	HSMA_RX_D_N6	AG12	LVDS or 2.5-V	LVDS RX bit 6n or CMOS bit 31
89	HSMA_TX_D_P7	AE6	LVDS or 2.5-V	LVDS TX bit 7 or CMOS bit 32
90	HSMA_RX_D_P7	AJ13	LVDS or 2.5-V	LVDS RX bit 7 or CMOS bit 33
91	HSMA_TX_D_N7	AD6	LVDS or 2.5-V	LVDS TX bit 7n or CMOS bit 34
92	HSMA_RX_D_N7	AH13	LVDS or 2.5-V	LVDS RX bit 7n or CMOS bit 35
95	HSMA_CLK_OUT_P1	AD8	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 36
96	HSMA_CLK_IN_P1	AN3	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 37
97	HSMA_CLK_OUT_N1	AC8	LVDS or 2.5-V	LVDS or CMOS clock out 1 or CMOS bit 38
98	HSMA_CLK_IN_N1	AP2	LVDS or 2.5-V	LVDS or CMOS clock in 1 or CMOS bit 39
101	HSMA_TX_D_P8	G9	LVDS or 2.5-V	LVDS TX bit 8 or CMOS bit 40
102	HSMA_RX_D_P8	A13	LVDS or 2.5-V	LVDS RX bit 8 or CMOS bit 41
103	HSMA_TX_D_N8	H9	LVDS or 2.5-V	LVDS TX bit 8n or CMOS bit 42
104	HSMA_RX_D_N8	B12	LVDS or 2.5-V	LVDS RX bit 8n or CMOS bit 43
107	HSMA_TX_D_P9	J6	LVDS or 2.5-V	LVDS TX bit 9 or CMOS bit 44

Table 2–34. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference (J13)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
108	HSMA_RX_D_P9	A11	LVDS or 2.5-V	LVDS RX bit 9 or CMOS bit 45
109	HSMA_TX_D_N9	K6	LVDS or 2.5-V	LVDS TX bit 9n or CMOS bit 46
110	HSMA_RX_D_N9	B11	LVDS or 2.5-V	LVDS RX bit 9n or CMOS bit 47
113	HSMA_TX_D_P10	G8	LVDS or 2.5-V	LVDS TX bit 10 or CMOS bit 48
114	HSMA_RX_D_P10	E11	LVDS or 2.5-V	LVDS RX bit 10 or CMOS bit 49
115	HSMA_TX_D_N10	G7	LVDS or 2.5-V	LVDS TX bit 10n or CMOS bit 50
116	HSMA_RX_D_N10	F11	LVDS or 2.5-V	LVDS RX bit 10n or CMOS bit 51
119	HSMA_TX_D_P11	G6	LVDS or 2.5-V	LVDS TX bit 11 or CMOS bit 52
120	HSMA_RX_D_P11	F10	LVDS or 2.5-V	LVDS RX bit 11 or CMOS bit 53
121	HSMA_TX_D_N11	H6	LVDS or 2.5-V	LVDS TX bit 11n or CMOS bit 54
122	HSMA_RX_D_N11	G10	LVDS or 2.5-V	LVDS RX bit 11n or CMOS bit 55
125	HSMA_TX_D_P12	E1	LVDS or 2.5-V	LVDS TX bit 12 or CMOS bit 56
126	HSMA_RX_D_P12	C11	LVDS or 2.5-V	LVDS RX bit 12 or CMOS bit 57
127	HSMA_TX_D_N12	F1	LVDS or 2.5-V	LVDS TX bit 12n or CMOS bit 58
128	HSMA_RX_D_N12	D11	LVDS or 2.5-V	LVDS RX bit 12n or CMOS bit 59
131	HSMA_TX_D_P13	E5	LVDS or 2.5-V	LVDS TX bit 13 or CMOS bit 60
132	HSMA_RX_D_P13	A10	LVDS or 2.5-V	LVDS RX bit 13 or CMOS bit 61
133	HSMA_TX_D_N13	F6	LVDS or 2.5-V	LVDS TX bit 13n or CMOS bit 62
134	HSMA_RX_D_N13	B9	LVDS or 2.5-V	LVDS RX bit 13n or CMOS bit 63
137	HSMA_TX_D_P14	E8	LVDS or 2.5-V	LVDS TX bit 14 or CMOS bit 64
138	HSMA_RX_D_P14	C8	LVDS or 2.5-V	LVDS RX bit 14 or CMOS bit 65
139	HSMA_TX_D_N14	F7	LVDS or 2.5-V	LVDS TX bit 14n or CMOS bit 66
140	HSMA_RX_D_N14	D7	LVDS or 2.5-V	LVDS RX bit 14n or CMOS bit 67
143	HSMA_TX_D_P15	E9	LVDS or 2.5-V	LVDS TX bit 15 or CMOS bit 68
144	HSMA_RX_D_P15	A7	LVDS or 2.5-V	LVDS RX bit 15 or CMOS bit 69
145	HSMA_TX_D_N15	F8	LVDS or 2.5-V	LVDS TX bit 15n or CMOS bit 70
146	HSMA_RX_D_N15	A6	LVDS or 2.5-V	LVDS RX bit 15n or CMOS bit 71
149	HSMA_TX_D_P16	A8	LVDS or 2.5-V	LVDS TX bit 16 or CMOS bit 72
150	HSMA_RX_D_P16	B6	LVDS or 2.5-V	LVDS RX bit 16 or CMOS bit 73
151	HSMA_TX_D_N16	B8	LVDS or 2.5-V	LVDS TX bit 16n or CMOS bit 74
152	HSMA_RX_D_N16	C7	LVDS or 2.5-V	LVDS RX bit 16n or CMOS bit 75
155	HSMA_CLK_OUT_P2	L9	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 76
156	HSMA_CLK_IN_P2	C1	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 77
157	HSMA_CLK_OUT_N2	M8	LVDS or 2.5-V	LVDS or CMOS clock out 2 or CMOS bit 78
158	HSMA_CLK_IN_N2	C2	LVDS or 2.5-V	LVDS or CMOS clock in 2 or CMOS bit 79
160	HSMA_PRSNTn	J8	2.5-V CMOS	HSMC port A presence detect

Table 2–35 lists the HSMC connector component reference and manufacturing information.

Table 2–35. HSMC Connector Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J13	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com

SDI Video Output/Input

The SDI video port consists of a LMH0303 cable driver and a LMH0384 cable equalizer. The PHY devices from National Semiconductor interface to single-ended 75-Ω SMB connectors.

The cable driver supports operation at 270 Mbit standard definition (SD), 1.5 Gbit high definition (HD), and 2.97 Gbit dual-link HD modes. Control signals are allowed for SD and HD modes selections, as well as device enable. The device can be clocked by the 148.5 MHz voltage-controlled crystal oscillator (VCXO) and matched to incoming signals within 50 ppm using the UP and DN voltage control lines to the VCXO.

Table 2–36 lists the supported output standards for the SD and HD input.

Table 2–36. Supported Output Standards for SD and HD Input

SD_HD Input	Supported Output Standards	Rise TIme
0	SMPTE 424M, SMPTE 292M	Faster
1	SMPTE 259M	Slower

For more information about the application circuit of the cable driver, refer to the cable driver data sheet in www.national.com.

Table 2–37 summarizes the SDI video output interface pin assignments, signal names, and functions.

Table 2–37. SDI Video Output Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U18)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
1	SDI_TX_P	L32	1.5-V PCML	SDI video output P
2	SDI_TX_N	L31	1.5-V PCML	SDI video output N
6	SDI_TX_EN	AC24	2.5-V	Device enable
7	SDI_SDA	AJ28	2.5-V	Cable driver I²C bus
8	SDI_SCL	AH28	2.5-V	Cable driver I²C bus
10	SDI_TX_SD_HDN	AC25	2.5-V	High-definition select
13	SDI_FAULT	AJ29	2.5-V	Data transmission fault

The cable equalizer supports operation at 270 Mbit SD, 1.5 Gbit HD, and 2.97 Gbit dual-link HD modes. Control signals are allowed for bypassing or disabling the device, as well as a carrier detect or auto-mute signal interface.

Table 2–38 lists the cable equalizer lengths.

Table 2–38. SDI Cable Equalizer Lengths

Data Rate (Mbps)	Cable Type	Maximum Cable Length (m)
270	Belden 1694A	400
1485		140
2970		120

Figure 2–11 is an excerpt from the LMH0384 cable equalizer data sheet that shows the SDI cable equalizer. On this starter board, the output is a single-ended output, with the negative channel driving a load local to the board.

Figure 2–11. SDI Cable Equalizer

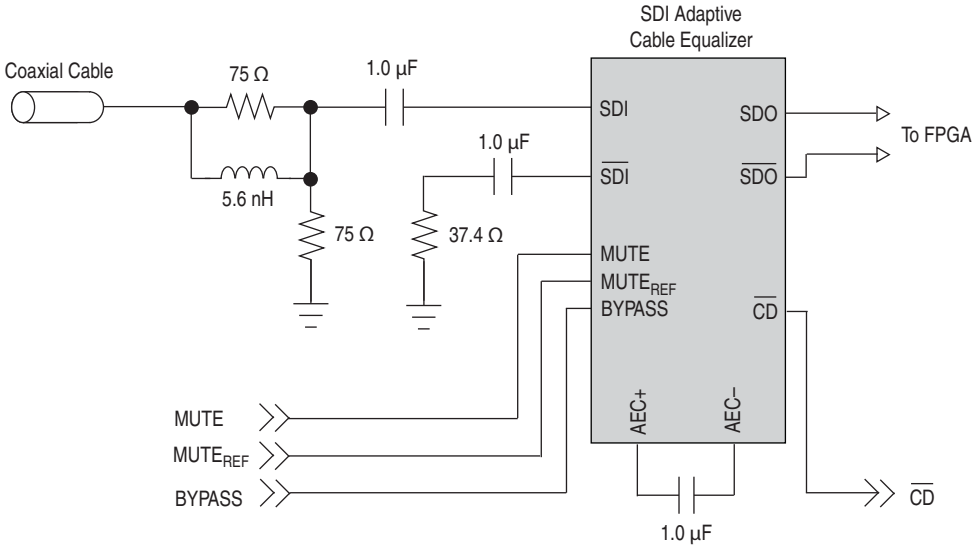


Table 2–39 summarizes the SDI video input interface pin assignments, signal names, and functions.

Table 2–39. SDI Video Input Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U19)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
7	SDI_RX_BYPASS	AD24	2.5-V	Equalizer bypass enable
14	SDI_RX_EN	AD23	2.5-V	Device enable
11	SDI_RX_P	M34	1.5-V PCML	SDI video input P
10	SDI_RX_N	M33	1.5-V PCML	SDI video input N

Table 2–40 lists the SDI connector component reference and manufacturing information.

Table 2–40. SDI Connector Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U18	3-Gbps HD/SD SDI cable driver with cable detect	National Semiconductor	LMH0303SQx	www.national.com
U19	3-Gbps HD/SD SDI adaptive cable equalizer	National Semiconductor	LMH0384SQ	www.national.com

HDMI Video Output

This starter board supports HDMI video (output only) using Arria V transceiver through the TMDS level shifter. This device is compliant with HDMI v1.3. The 2.7 Gbps operation supports television resolutions from 720p up to 1080p at 12-bit color depth and computer graphics outputs at up to UXGA, or 1600x1200.

For more information about the HDMI video IP, visit www.bitec-dsp.com.

Table 2–41 summarizes the HDMI video output TMDS level shifter pin assignments, signal names, and functions.

Table 2–41. HDMI Video Output Interface Pin Assignments, Schematic Signal Names, and Functions

Board Reference (U16)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
30	HDMI_FPGA_HPD	AF8	2.5-V	HDMI connector hot-plug detect
25	HDMI_FPGA_OE_N	AC9	2.5-V	Video output data or clock enable
9	HDMI_FPGA_SCL_DDC	AE11	2.5-V	Management bus clock
8	HDMI_FPGA_SDA_DDC	AD11	2.5-V	Management bus data
39	HDMI_TX_P0	AJ3	1.5-V PCML	Video output data
38	HDMI_TX_N0	AJ4	1.5-V PCML	Video output data
42	HDMI_TX_P1	AG3	1.5-V PCML	Video output data
41	HDMI_TX_N1	AG4	1.5-V PCML	Video output data
45	HDMI_TX_P2	AE3	1.5-V PCML	Video output data
44	HDMI_TX_N2	AE4	1.5-V PCML	Video output data
48	HDMI_TX_CLK_P	AC3	1.5-V PCML	Video output clock
47	HDMI_TX_CLK_N	AC4	1.5-V PCML	Video output clock

Table 2–40 lists the HDMI video output component reference and manufacturing information.

Table 2–42. HDMI Video Output Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J10	19-pin HDMI connector	Samtec	HDMI-19-01-F-SM	www.samtec.com
U16	TMDS level shifter	ST Microelectronics	STHDLS101T	www.st.com

Memory

This section describes the starter board's memory interface support and also their signal names, types, and connectivity relative to the Arria V GX. The starter board has the following memory interfaces:

- DDR3 SDRAM
- Synchronous SRAM
- Synchronous flash

For more information about the memory interfaces, refer to the following documents:

- *Timing Analysis* section in volume 4 of the External Memory Interface Handbook.
- *DDR, DDR2, and DDR3 SDRAM Design Tutorials* section in volume 6 of the External Memory Interface Handbook.

DDR3 SDRAM

The starter board supports a 8Mx32x8 bank DDR3 SDRAM interface for very high-speed sequential memory access. The 32-bit data bus consists of two x16 devices with a single address or command bus. This interface connects to the vertical I/O banks on the top edge of the FPGA.

This DDR3 SDRAM has two interface options. The first option is a x32 interface using a hard memory controller. The second option is a x32 interface using a soft memory controller.

With a hard memory controller, this interface runs at the target frequency of 533 MHz for a maximum theoretical bandwidth of 33.31 Gbps. With a soft memory controller, this interface runs at the target frequency of 667 MHz for a maximum theoretical bandwidth of 41.66 Gbps. Though a soft memory controller runs at higher data rate than a hard memory controller, the hard memory controller operates at a much higher efficiency. The maximum frequency for the Micron device is 667 MHz with a CAS latency of 9.

Table 2–43 lists the DDR3 pin assignments, signal names, and functions. The signal names and types are relative to the Arria V GX in terms of I/O setting and direction.

Table 2–43. DDR3 Device Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
DDR3 x16 (U11)				
N3	DDR3_A0	D26	1.5-V SSTL Class I	Address bus
P7	DDR3_A1	E27	1.5-V SSTL Class I	Address bus
P3	DDR3_A2	A27	1.5-V SSTL Class I	Address bus
N2	DDR3_A3	B27	1.5-V SSTL Class I	Address bus
P8	DDR3_A4	G26	1.5-V SSTL Class I	Address bus
P2	DDR3_A5	H26	1.5-V SSTL Class I	Address bus
R8	DDR3_A6	K27	1.5-V SSTL Class I	Address bus

Table 2–43. DDR3 Device Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
R2	DDR3_A7	L27	1.5-V SSTL Class I	Address bus
T8	DDR3_A8	D27	1.5-V SSTL Class I	Address bus
R3	DDR3_A9	C28	1.5-V SSTL Class I	Address bus
L7	DDR3_A10	C29	1.5-V SSTL Class I	Address bus
R7	DDR3_A11	D28	1.5-V SSTL Class I	Address bus
N7	DDR3_A12	G27	1.5-V SSTL Class I	Address bus
T3	DDR3_A13	G28	1.5-V SSTL Class I	Address bus
M2	DDR3_BA0	A29	1.5-V SSTL Class I	Bank address bus
N8	DDR3_BA1	A28	1.5-V SSTL Class I	Bank address bus
M3	DDR3_BA2	B29	1.5-V SSTL Class I	Bank address bus
K3	DDR3_CASN	F28	1.5-V SSTL Class I	Row address select
K9	DDR3_CKE	K29	1.5-V SSTL Class I	Column address select
J7	DDR3_CLK_P	E26	Differential 1.5-V SSTL Class I	Differential output clock
K7	DDR3_CLK_N	F26	Differential 1.5-V SSTL Class I	Differential output clock
L2	DDR3_CSN	D30	1.5-V SSTL Class I	Chip select
E7	DDR3_DM0	M25	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3_DM1	M23	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3_DQ0	G24	1.5-V SSTL Class I	Data bus byte lane 0
F7	DDR3_DQ1	H24	1.5-V SSTL Class I	Data bus byte lane 0
F2	DDR3_DQ2	M24	1.5-V SSTL Class I	Data bus byte lane 0
F8	DDR3_DQ3	A26	1.5-V SSTL Class I	Data bus byte lane 0
H3	DDR3_DQ4	A25	1.5-V SSTL Class I	Data bus byte lane 0
H8	DDR3_DQ5	C25	1.5-V SSTL Class I	Data bus byte lane 0
G2	DDR3_DQ6	B26	1.5-V SSTL Class I	Data bus byte lane 0
H7	DDR3_DQ7	C26	1.5-V SSTL Class I	Data bus byte lane 0
D7	DDR3_DQ8	H23	1.5-V SSTL Class I	Data bus byte lane 1
C3	DDR3_DQ9	J23	1.5-V SSTL Class I	Data bus byte lane 1
C8	DDR3_DQ10	K24	1.5-V SSTL Class I	Data bus byte lane 1
C2	DDR3_DQ11	B24	1.5-V SSTL Class I	Data bus byte lane 1
A7	DDR3_DQ12	C23	1.5-V SSTL Class I	Data bus byte lane 1
A2	DDR3_DQ13	D23	1.5-V SSTL Class I	Data bus byte lane 1
B8	DDR3_DQ14	D24	1.5-V SSTL Class I	Data bus byte lane 1
A3	DDR3_DQ15	E24	1.5-V SSTL Class I	Data bus byte lane 1
F3	DDR3_DQS_P0	F25	Differential 1.5-V SSTL Class I	Data strobe P byte lane 0
G3	DDR3_DQS_N0	G25	Differential 1.5-V SSTL Class I	Data strobe N byte lane 0

Table 2–43. DDR3 Device Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
C7	DDR3_DQS_P1	F23	Differential 1.5-V SSTL Class I	Data strobe P byte lane 1
B7	DDR3_DQS_N1	G23	Differential 1.5-V SSTL Class I	Data strobe N byte lane 1
K1	DDR3_ODT	H27	1.5-V SSTL Class I	On-die termination enable
J3	DDR3_RASN	B30	1.5-V SSTL Class I	Row address select
T2	DDR3_RESETN	K25	1.5-V SSTL Class I	Reset
L3	DDR3_WEN	F29	1.5-V SSTL Class I	Write enable
L8	DDR3_ZQ01	—	1.5-V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U10)				
N3	DDR3_A0	D26	1.5-V SSTL Class I	Address bus
P7	DDR3_A1	E27	1.5-V SSTL Class I	Address bus
P3	DDR3_A2	A27	1.5-V SSTL Class I	Address bus
N2	DDR3_A3	B27	1.5-V SSTL Class I	Address bus
P8	DDR3_A4	G26	1.5-V SSTL Class I	Address bus
P2	DDR3_A5	H26	1.5-V SSTL Class I	Address bus
R8	DDR3_A6	K27	1.5-V SSTL Class I	Address bus
R2	DDR3_A7	L27	1.5-V SSTL Class I	Address bus
T8	DDR3_A8	D27	1.5-V SSTL Class I	Address bus
R3	DDR3_A9	C28	1.5-V SSTL Class I	Address bus
L7	DDR3_A10	C29	1.5-V SSTL Class I	Address bus
R7	DDR3_A11	D28	1.5-V SSTL Class I	Address bus
N7	DDR3_A12	G27	1.5-V SSTL Class I	Address bus
T3	DDR3_A13	G28	1.5-V SSTL Class I	Address bus
M2	DDR3_BA0	A29	1.5-V SSTL Class I	Bank address bus
N8	DDR3_BA1	A28	1.5-V SSTL Class I	Bank address bus
M3	DDR3_BA2	B29	1.5-V SSTL Class I	Bank address bus
K3	DDR3_CASN	F28	1.5-V SSTL Class I	Row address select
K9	DDR3_CKE	K29	1.5-V SSTL Class I	Column address select
K7	DDR3_CLK_N	F26	1.5-V SSTL Class I	Differential output clock
J7	DDR3_CLK_P	E26	1.5-V SSTL Class I	Differential output clock
L2	DDR3_CSN	D30	1.5-V SSTL Class I	Chip select
E7	DDR3_DM2	M22	1.5-V SSTL Class I	Write mask byte lane
D3	DDR3_DM3	K21	1.5-V SSTL Class I	Write mask byte lane
E3	DDR3_DQ16	D21	1.5-V SSTL Class I	Data bus byte lane 2
F7	DDR3_DQ17	E21	1.5-V SSTL Class I	Data bus byte lane 2
F2	DDR3_DQ18	M21	1.5-V SSTL Class I	Data bus byte lane 2
F8	DDR3_DQ19	C22	1.5-V SSTL Class I	Data bus byte lane 2
H3	DDR3_DQ20	D22	1.5-V SSTL Class I	Data bus byte lane 2

Table 2–43. DDR3 Device Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
H8	DDR3_DQ21	G21	1.5-V SSTL Class I	Data bus byte lane 2
G2	DDR3_DQ22	A23	1.5-V SSTL Class I	Data bus byte lane 2
H7	DDR3_DQ23	B23	1.5-V SSTL Class I	Data bus byte lane 2
D7	DDR3_DQ24	K20	1.5-V SSTL Class I	Data bus byte lane 3
C3	DDR3_DQ25	L20	1.5-V SSTL Class I	Data bus byte lane 3
C8	DDR3_DQ26	M20	1.5-V SSTL Class I	Data bus byte lane 3
C2	DDR3_DQ27	A22	1.5-V SSTL Class I	Data bus byte lane 3
A7	DDR3_DQ28	B21	1.5-V SSTL Class I	Data bus byte lane 3
A2	DDR3_DQ29	B20	1.5-V SSTL Class I	Data bus byte lane 3
B8	DDR3_DQ30	F20	1.5-V SSTL Class I	Data bus byte lane 3
A3	DDR3_DQ31	G20	1.5-V SSTL Class I	Data bus byte lane 3
F3	DDR3_DQS_P2	F22	Differential 1.5-V SSTL Class I	Data strobe P byte lane 2
G3	DDR3_DQS_N2	G22	Differential 1.5-V SSTL Class I	Data strobe N byte lane 2
C7	DDR3_DQS_P3	D20	Differential 1.5-V SSTL Class I	Data strobe P byte lane 3
B7	DDR3_DQS_N3	E20	Differential 1.5-V SSTL Class I	Data strobe N byte lane 3
K1	DDR3_ODT	H27	1.5-V SSTL Class I	On-die termination enable
J3	DDR3_RASN	B30	1.5-V SSTL Class I	Row address select
T2	DDR3_RESETN	K25	1.5-V SSTL Class I	Reset
L3	DDR3_WEN	F29	1.5-V SSTL Class I	Write enable
L8	DDR3_ZQ2	—	1.5-V SSTL Class I	ZQ impedance calibration

Table 2–44 lists the DDR3 component reference and manufacturing information.

Table 2–44. DDR3 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U10, U11	8M×16×8, 1 Gb, DDR3 memory	Micron	MT41J64M16JT-15E	www.micron.com

Synchronous SRAM

The starter board supports a 18-Mb standard synchronous SRAM intended to be used by NIOS II systems for instruction and data storage with low-latency random access capability. The device has a 512K x 36-bits interface (32-bits data and 4-bits parity). This device is part of the shared FSM bus that connects to the flash memory, SRAM, and MAX V CPLD 5M2210 System Controller.

The device speed is 200 MHz single-data-rate. There is no minimum speed for this device. The theoretical bandwidth of this 32-bit interface is 6.4 Gbps for continuous bursts. The read latency for any address is two clocks while the write latency is one clock.

Table 2–45 lists the SSRAM pin assignments, signal names, and functions.

Table 2–45. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference (U14)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
R6	FSM_A2	AN23	2.5-V	Address bus
P6	FSM_A3	AN24	2.5-V	Address bus
A2	FSM_A4	AM23	2.5-V	Address bus
A10	FSM_A5	AL23	2.5-V	Address bus
B2	FSM_A6	AL24	2.5-V	Address bus
B10	FSM_A7	AK24	2.5-V	Address bus
N6	FSM_A8	AK23	2.5-V	Address bus
P3	FSM_A9	AJ23	2.5-V	Address bus
P4	FSM_A10	AJ25	2.5-V	Address bus
P8	FSM_A11	AH23	2.5-V	Address bus
P9	FSM_A12	AH24	2.5-V	Address bus
P10	FSM_A13	AH25	2.5-V	Address bus
P11	FSM_A14	AG23	2.5-V	Address bus
R3	FSM_A15	AG24	2.5-V	Address bus
R4	FSM_A16	AF23	2.5-V	Address bus
R8	FSM_A17	AF25	2.5-V	Address bus
R9	FSM_A18	AE25	2.5-V	Address bus
R10	FSM_A19	AE24	2.5-V	Address bus
R11	FSM_A20	AE23	2.5-V	Address bus
B1	FSM_A21	AP20	2.5-V	Address bus
A1	FSM_A22	AN21	2.5-V	Address bus
B11	FSM_A23	AN20	2.5-V	Address bus
C10	FSM_A24	AM20	2.5-V	Address bus
P2	FSM_A25	AM22	2.5-V	Address bus
J10	FSM_D0	AD27	2.5-V	Data bus
J11	FSM_D1	AD26	2.5-V	Data bus
K10	FSM_D2	AE26	2.5-V	Data bus
K11	FSM_D3	AE28	2.5-V	Data bus
L10	FSM_D4	AF29	2.5-V	Data bus
L11	FSM_D5	AF28	2.5-V	Data bus
M10	FSM_D6	AF26	2.5-V	Data bus
M11	FSM_D7	AG29	2.5-V	Data bus
D10	FSM_D8	AG26	2.5-V	Data bus
D11	FSM_D9	AH29	2.5-V	Data bus
E10	FSM_D10	AG27	2.5-V	Data bus
E11	FSM_D11	AH27	2.5-V	Data bus
F10	FSM_D12	AH26	2.5-V	Data bus

Table 2–45. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference (U14)	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
F11	FSM_D13	AJ26	2.5-V	Data bus
G10	FSM_D14	AK27	2.5-V	Data bus
G11	FSM_D15	AK26	2.5-V	Data bus
D1	FSM_D16	AL27	2.5-V	Data bus
D2	FSM_D17	AL28	2.5-V	Data bus
E1	FSM_D18	AL29	2.5-V	Data bus
E2	FSM_D19	AL31	2.5-V	Data bus
F1	FSM_D20	AM31	2.5-V	Data bus
F2	FSM_D21	AM29	2.5-V	Data bus
G1	FSM_D22	AM28	2.5-V	Data bus
G2	FSM_D23	AL26	2.5-V	Data bus
J1	FSM_D24	AL25	2.5-V	Data bus
J2	FSM_D25	AM26	2.5-V	Data bus
K1	FSM_D26	AM25	2.5-V	Data bus
K2	FSM_D27	AN26	2.5-V	Data bus
L1	FSM_D28	AP28	2.5-V	Data bus
L2	FSM_D29	AP27	2.5-V	Data bus
M1	FSM_D30	AP26	2.5-V	Data bus
M2	FSM_D31	AP25	2.5-V	Data bus
A8	SRAM_ADSCN	AP19	2.5-V	Address status controller
B9	SRAM_ADSPN	AF19	2.5-V	Address status processor
A9	SRAM_ADVN	AE19	2.5-V	Address valid
A7	SRAM_BWEN	AP17	2.5-V	Byte write enable
B5	SRAM_BWN0	AM17	2.5-V	Byte lane 0 write enable
A5	SRAM_BWN1	AM19	2.5-V	Byte lane 1 write enable
A4	SRAM_BWN2	AN17	2.5-V	Byte lane 2 write enable
B4	SRAM_BWN3	AN18	2.5-V	Byte lane 3 write enable
A3	SRAM_CEN	AL19	2.5-V	Chip enable
B6	SRAM_CLK	AL18	2.5-V	Clock
N11	SRAM_DQP0	AF20	2.5-V	Data bus parity byte lane 0
C11	SRAM_DQP1	AE20	2.5-V	Data bus parity byte lane 1
C1	SRAM_DQP2	AE22	2.5-V	Data bus parity byte lane 2
N1	SRAM_DQP3	AE21	2.5-V	Data bus parity byte lane 3
B7	SRAM_GWN	AF22	2.5-V	Global write enable
R1	SRAM_MODE	AG21	2.5-V	Burst sequence selection
B8	SRAM_OEN	AL17	2.5-V	Output enable
H11	SRAM_ZZ	AD21	2.5-V	Power sleep mode

Table 2–44 lists the SRAM component reference and manufacturing information.

Table 2–46. SRAM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U14	Standard synchronous pipelined SCD, 512K × 36 bit, 200 MHz	Integrated Silicon Solution, Inc.	IS61VPS51236A-200B3	www.issi.com

Flash

The starter board supports two 1-Gb CFI-compatible synchronous flash device for non-volatile storage of FPGA configuration data, board information, test application data, and user code space. This device is part of the shared FSM bus that connects to the flash memory, SSRAM, and MAX V CPLD 5M2210 System Controller.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps per device. The write performance is 270 µs for a single word buffer while the erase time is 800 ms for a 128 K array block.

Table 2–47 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Arria V GX in terms of I/O setting and direction.

Table 2–47. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
Flash A (U12)				
F6	FLASH_ADVN	AJ20	2.5-V	Address valid
B4	FLASH_CEN0	AK21	2.5-V	Chip enable
E6	FLASH_CLK	AJ22	2.5-V	Clock
F8	FLASH_OEN	AL22	2.5-V	Output enable
F7	FLASH_RDYBSYN0	AH20	2.5-V	Ready
D4	FLASH_RESETN	AH22	2.5-V	Reset
G8	FLASH_WEN	AH21	2.5-V	Write enable
C6	FLASH_WPN	—	2.5-V	Write protect
A1	FSM_A2	AN23	2.5-V	Address bus
B1	FSM_A3	AN24	2.5-V	Address bus
C1	FSM_A4	AM23	2.5-V	Address bus
D1	FSM_A5	AL23	2.5-V	Address bus
D2	FSM_A6	AL24	2.5-V	Address bus
A2	FSM_A7	AK24	2.5-V	Address bus
C2	FSM_A8	AK23	2.5-V	Address bus
A3	FSM_A9	AJ23	2.5-V	Address bus
B3	FSM_A10	AJ25	2.5-V	Address bus
C3	FSM_A11	AH23	2.5-V	Address bus
D3	FSM_A12	AH24	2.5-V	Address bus

Table 2–47. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
C4	FSM_A13	AH25	2.5-V	Address bus
A5	FSM_A14	AG23	2.5-V	Address bus
B5	FSM_A15	AG24	2.5-V	Address bus
C5	FSM_A16	AF23	2.5-V	Address bus
D7	FSM_A17	AF25	2.5-V	Address bus
D8	FSM_A18	AE25	2.5-V	Address bus
A7	FSM_A19	AE24	2.5-V	Address bus
B7	FSM_A20	AE23	2.5-V	Address bus
C7	FSM_A21	AP20	2.5-V	Address bus
C8	FSM_A22	AN21	2.5-V	Address bus
A8	FSM_A23	AN20	2.5-V	Address bus
G1	FSM_A24	AM20	2.5-V	Address bus
H8	FSM_A25	AM22	2.5-V	Address bus
B6	FSM_A26	AL20	2.5-V	Address bus
B8	FSM_A27	AD20	2.5-V	Address bus
F2	FSM_D0	AD27	2.5-V	Data bus
E2	FSM_D1	AD26	2.5-V	Data bus
G3	FSM_D2	AE26	2.5-V	Data bus
E4	FSM_D3	AE28	2.5-V	Data bus
E5	FSM_D4	AF29	2.5-V	Data bus
G5	FSM_D5	AF28	2.5-V	Data bus
G6	FSM_D6	AF26	2.5-V	Data bus
H7	FSM_D7	AG29	2.5-V	Data bus
E1	FSM_D8	AG26	2.5-V	Data bus
E3	FSM_D9	AH29	2.5-V	Data bus
F3	FSM_D10	AG27	2.5-V	Data bus
F4	FSM_D11	AH27	2.5-V	Data bus
F5	FSM_D12	AH26	2.5-V	Data bus
H5	FSM_D13	AJ26	2.5-V	Data bus
G7	FSM_D14	AK27	2.5-V	Data bus
E7	FSM_D15	AK26	2.5-V	Data bus
Flash B (U13)				
F6	FLASH_ADVN	AJ20	2.5-V	Address valid
B4	FLASH_CEN1	AK20	2.5-V	Chip enable
E6	FLASH_CLK	AJ22	2.5-V	Clock
F8	FLASH_OEN	AL22	2.5-V	Output enable
F7	FLASH_RDYBSYN1	AG20	2.5-V	Ready
D4	FLASH_RESETN	AH22	2.5-V	Reset

Table 2–47. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
G8	FLASH_WEN	AH21	2.5-V	Write enable
C6	FLASH_WPN	—	2.5-V	Write protect
A1	FSM_A2	AN23	2.5-V	Address bus
B1	FSM_A3	AN24	2.5-V	Address bus
C1	FSM_A4	AM23	2.5-V	Address bus
D1	FSM_A5	AL23	2.5-V	Address bus
D2	FSM_A6	AL24	2.5-V	Address bus
A2	FSM_A7	AK24	2.5-V	Address bus
C2	FSM_A8	AK23	2.5-V	Address bus
A3	FSM_A9	AJ23	2.5-V	Address bus
B3	FSM_A10	AJ25	2.5-V	Address bus
C3	FSM_A11	AH23	2.5-V	Address bus
D3	FSM_A12	AH24	2.5-V	Address bus
C4	FSM_A13	AH25	2.5-V	Address bus
A5	FSM_A14	AG23	2.5-V	Address bus
B5	FSM_A15	AG24	2.5-V	Address bus
C5	FSM_A16	AF23	2.5-V	Address bus
D7	FSM_A17	AF25	2.5-V	Address bus
D8	FSM_A18	AE25	2.5-V	Address bus
A7	FSM_A19	AE24	2.5-V	Address bus
B7	FSM_A20	AE23	2.5-V	Address bus
C7	FSM_A21	AP20	2.5-V	Address bus
C8	FSM_A22	AN21	2.5-V	Address bus
A8	FSM_A23	AN20	2.5-V	Address bus
G1	FSM_A24	AM20	2.5-V	Address bus
H8	FSM_A25	AM22	2.5-V	Address bus
B6	FSM_A26	AL20	2.5-V	Address bus
B8	FSM_A27	AD20	2.5-V	Address bus
F2	FSM_D16	AL27	2.5-V	Data bus
E2	FSM_D17	AL28	2.5-V	Data bus
G3	FSM_D18	AL29	2.5-V	Data bus
E4	FSM_D19	AL31	2.5-V	Data bus
E5	FSM_D20	AM31	2.5-V	Data bus
G5	FSM_D21	AM29	2.5-V	Data bus
G6	FSM_D22	AM28	2.5-V	Data bus
H7	FSM_D23	AL26	2.5-V	Data bus
E1	FSM_D24	AL25	2.5-V	Data bus
E3	FSM_D25	AM26	2.5-V	Data bus
F3	FSM_D26	AM25	2.5-V	Data bus

Table 2–47. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Schematic Signal Name	Arria V GX Pin Number	I/O Standard	Description
F4	FSM_D27	AN26	2.5-V	Data bus
F5	FSM_D28	AP28	2.5-V	Data bus
H5	FSM_D29	AP27	2.5-V	Data bus
G7	FSM_D30	AP26	2.5-V	Data bus
E7	FSM_D31	AP25	2.5-V	Data bus

Table 2–48 lists the flash component reference and manufacturing information.

Table 2–48. Flash Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U12, U13	1-Gb synchronous flash	Numonyx	PC28F00AP30BF	www.numonyx.com

Power Supply

You can power up the starter board either from a laptop-style DC power input or from the PCI Express edge connector. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to various power rails used by the board components and installed into the HSMC connectors.

Table 2–49 outlines the allowable power inputs.

Table 2–49. Power Inputs

Power Source	Voltage (V)	Current (A)	Maximum Wattage (W)
Laptop-style DC input	19.0	6.5	120
25-W PCI Express edge connector	3.3	3.0	9
	12.0	2.1	16
75-W PCI Express edge connector	3.3	3.0	9
	12.0	5.5	66

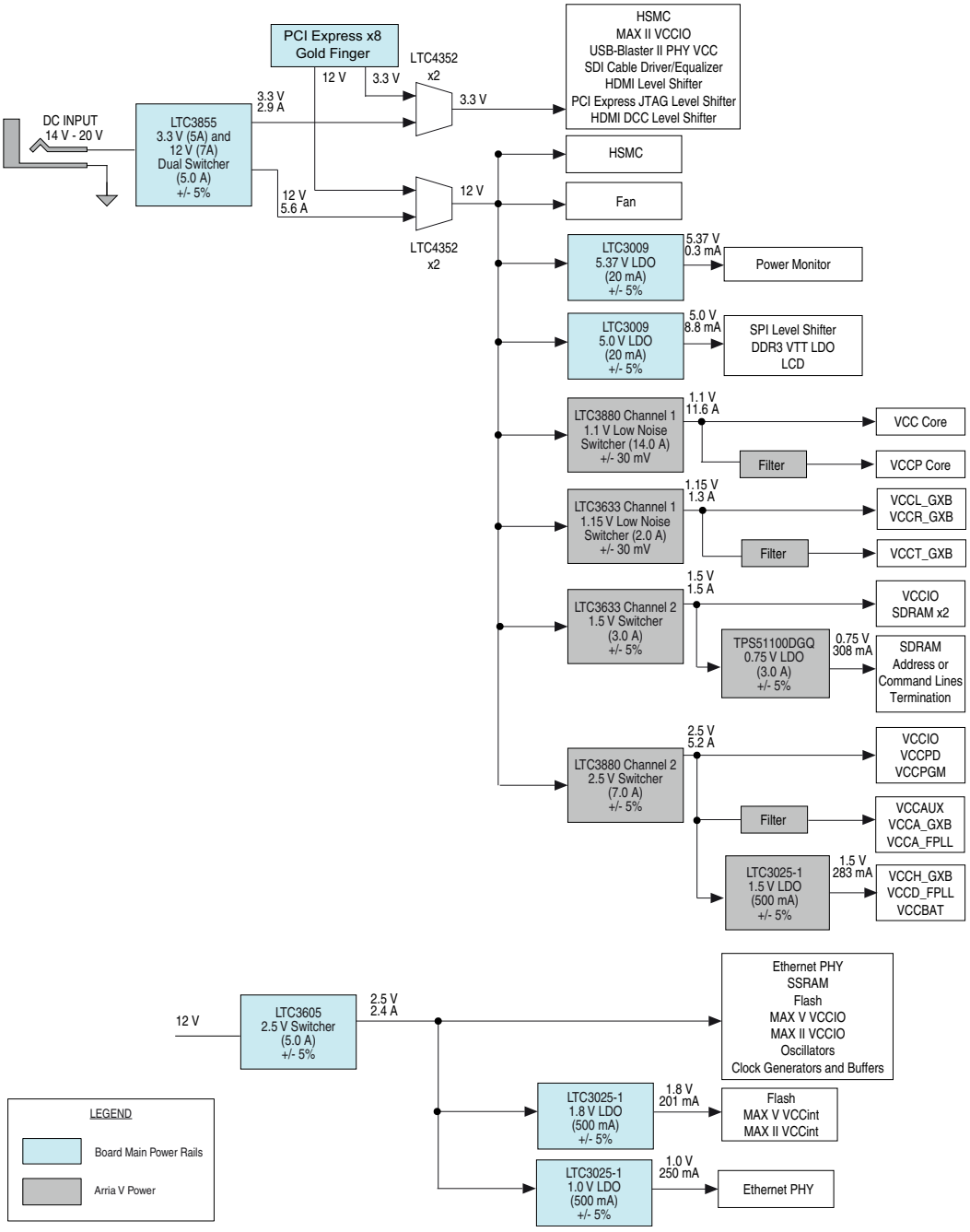
An on-board multi-channel analog-to-digital converter (ADC) measures the current for several specific board rails.

Power Distribution System

Figure 2–12 shows the power distribution system on the development board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

If the sourcing current is higher than the rated current of the switching regulator, refer to www.linear.com for technical support.

Figure 2–12. Power Distribution System



Power Measurement

There are 8 power supply rails that have on-board current sense capabilities using 24-bit differential ADC devices. Precision sense resistors split the ADC devices and rails from the primary supply plane for the ADC to measure current. A SPI bus connects these ADC devices to the MAX V CPLD 5M2210 System Controller.

Figure 2–13 shows the block diagram for the power measurement circuitry.

Figure 2–13. Power Measurement Circuit

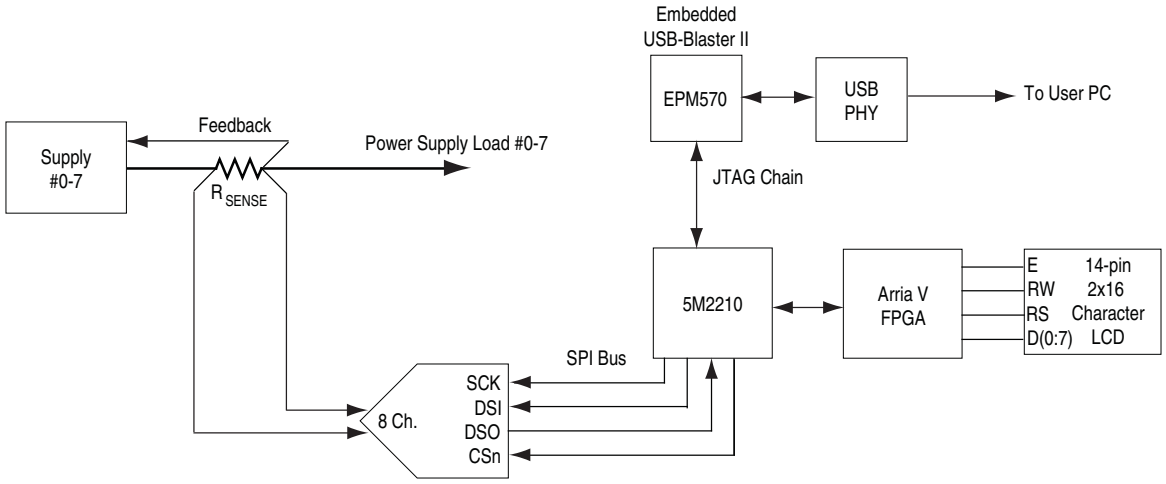


Table 2–50 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured while the device pin column specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2–50. Power Measurement Rails (Part 1 of 2)

Channel	Schematic Signal Name	Voltage (V)	Device Pin	Description
0	A5_VCCINT	1.1	VCC	FPGA core and periphery power
1	A5_VCCL_VCCR_VCCT_GXB	1.1	VCCL_GXB	XCVR analog clock network
		1.1	VCCR_GXB	XCVR analog receive
		1.1	VCCT_GXB	XCVR analog transmit
2	A5_VCCIO_1.5V	1.5	VCCIO_8A, VCCIO_8B, VCCIO_8C	VCCIO bank 8 (DDR3)

Table 2–50. Power Measurement Rails (Part 2 of 2)

Channel	Schematic Signal Name	Voltage (V)	Device Pin	Description
3	A5_VCCIO_VCCPD_VCCPGM	2.5	VCCPD	I/O pre-drivers
		2.5	VCCPGM	Configuration I/O
		2.5	VCCIO_3A, VCCIO_3B, VCCIO_3C, VCCIO_3D, VCCIO_4A, VCCIO_4B, VCCIO_4C, VCCIO_4D, VCCIO_7A, VCCIO_7B, VCCIO_7C, VCCIO_7D, VCCIO_8D	VCC I/O banks 3, 4, 7 and 8D
4	A5_VCCAUX_VCCA_FPLL	2.5	VCCA_FPLL	PLL analog power
		2.5	VCC_AUX	Auxiliary
5	A5_VCCA_GXB	2.5	VCCA_GXB	XCVR transmit driver, receiver, CDR
6	A5_VCCH_GXB	1.5	VCCH_GXB	XCVR block level transmit buffers
7	A5_VCCD_FPLL_VCCBAT	1.5	VCCD_FPLL	PLL digital power
		1.5	VCCBAT	Battery power

Table 2–51 lists the power measurement ADC component reference and manufacturing information.

Table 2–51. Power Measurement ADC Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U40	8-channel differential 24-bit ADC	Linear Technology	LTC2418CGN#PBF	www.linear.com

Statement of China-RoHS Compliance

Table 2–52 lists hazardous substances included with the kit.

Table 2–52. Table of Hazardous Substances' Name and Concentration *Notes* (1), (2)

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Arria V GX starter board	X*	0	0	0	0	0
12 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–52:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

CE EMI Conformity Caution

This development kit is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices it is possible for the user to modify the kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as the result of modifications to the delivered material is the responsibility of the user.

This chapter provides additional information about the document and Altera.

Board Revision History

The following table lists the versions of all releases of the Arria V GX starter board.

Version	Release Date	Description
Production silicon	October 2012	Production device.
Engineering silicon (ES)	July 2012	Initial release.

Document Revision History

The following table lists the revision history for this document.

Date	Version	Changes
September 2015	1.4	■ Correct component positions (SW3), (J6), (PB0, PB1, PB2), (SW5), and (J17) in Figure 2–1 on page 2–2. ■ Correct link to www.bitec-dsp.com in "HDMI Video Output" on page 2–38.
November 2013	1.3	■ Updated the PCI Express link width DIP switch (SW1) default settings in Table 2–13.
February 2013	1.2	■ Updated information for DDR3. ■ Added CE EMI Conformity Caution section.
October 2012	1.1	■ New board revision—changed to production silicon 5AGXFB3H4F35C4N. ■ Added ENET_GTX_CLK pin information in Table 2–32.
July 2012	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.