

P-channel -30 V, 0.01 Ω typ., -12.5 A, STripFET™ H6 Power MOSFET in an SO-8 package

Datasheet - production data

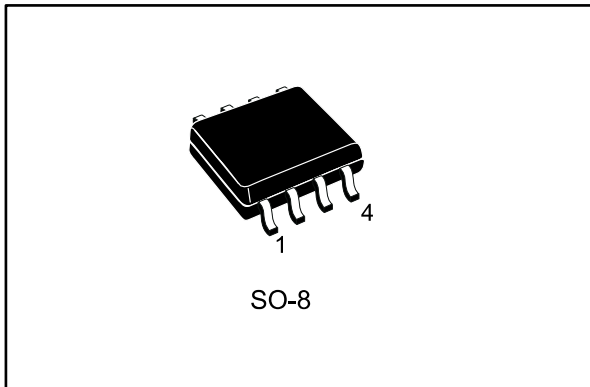
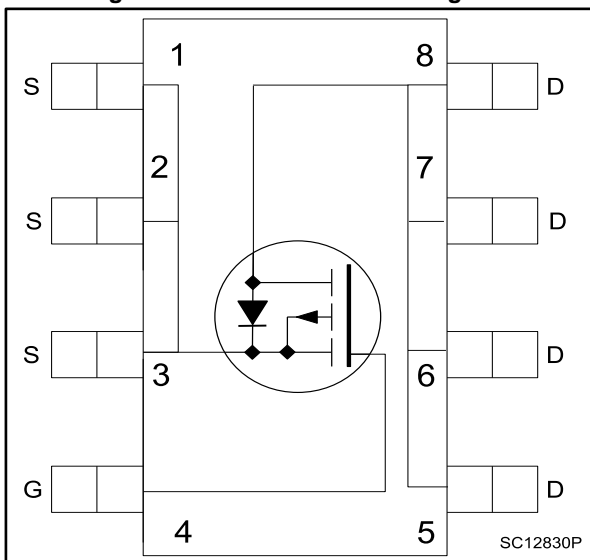


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STS10P3LLH6	-30 V	0.012 Ω	-12.5 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Packages	Packing
STS10P3LLH6	10K3L	SO-8	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	9
4	Package information	10
	4.1 SO-8 package information	10
	4.2 SO-8 packing information.....	12
5	Revision history	13

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_{amb} = 25\text{ }^{\circ}\text{C}$	-12.5	A
	Drain current (continuous) at $T_{amb} = 100\text{ }^{\circ}\text{C}$	-7.8	
$I_{DM}^{(1)}$	Drain current (pulsed)	-50	A
P_{TOT}	Total dissipation at $T_{amb} = 25\text{ }^{\circ}\text{C}$	2.7	W
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = -5\text{A}$)	70	mJ
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	47	$^{\circ}\text{C/W}$

Notes:

⁽¹⁾When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10\text{ s}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = -250 μA	-30			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = -30 V			-1	μA
		V _{DS} = -30 V, T _C = 125 °C ⁽¹⁾			-10	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			-100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = -250 μA	-1	-1.7	-2.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = -10 V, I _D = -5 A		0.01	0.012	Ω
		V _{GS} = -4.5 V, I _D = -5 A		0.014	0.017	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = -25 V, f = 1 MHz, V _{GS} = 0 V	-	3350	-	pF
C _{oss}	Output capacitance		-	414	-	pF
C _{rss}	Reverse transfer capacitance		-	287	-	pF
Q _g	Total gate charge	V _{DD} = -15 V, I _D = -10 A	-	33	-	nC
Q _{gs}	Gate-source charge	V _{GS} = -4.5 V	-	14	-	nC
Q _{gd}	Gate-drain charge	(see Figure 14: "Gate charge test circuit")	-	11	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = -15 V, I _D = -5 A	-	12.8	-	ns
t _r	Rise time	R _G = 4.7 Ω, V _{GS} = -10 V	-	112	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 13: "Switching times test circuit for resistive load")	-	61	-	ns
t _f	Fall time		-	45	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = -5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		-1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = -5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	25.2		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = -24 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	17.4		nC
I_{RRM}	Reverse recovery current	(see <i>Figure 15: "Source-drain diode forward characteristics"</i>)	-	-1.4		A

Notes:

⁽¹⁾Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)



For the P-channel Power MOSFET, current and voltage polarities are reversed

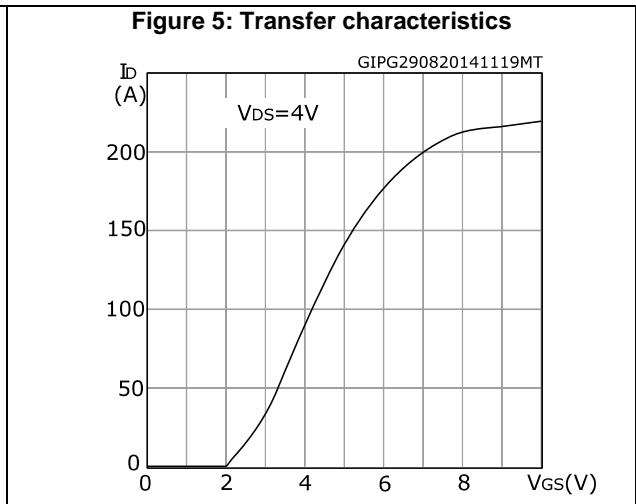
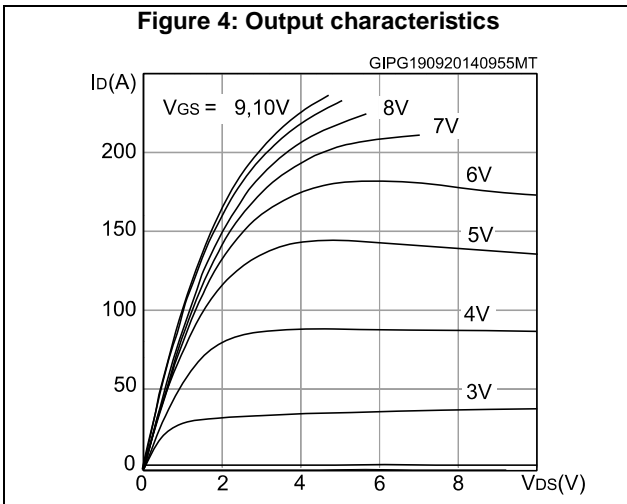
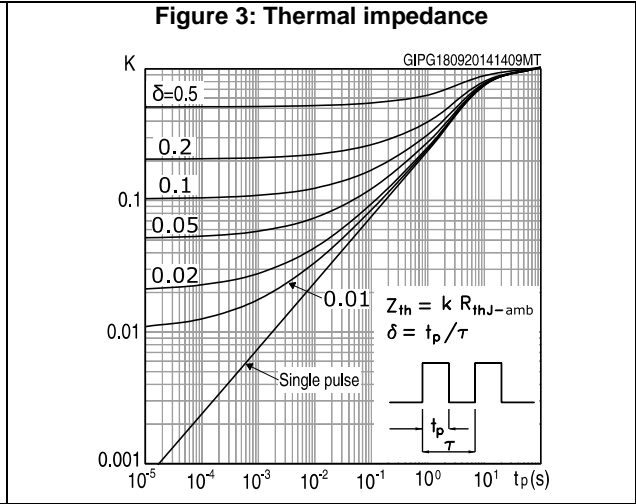
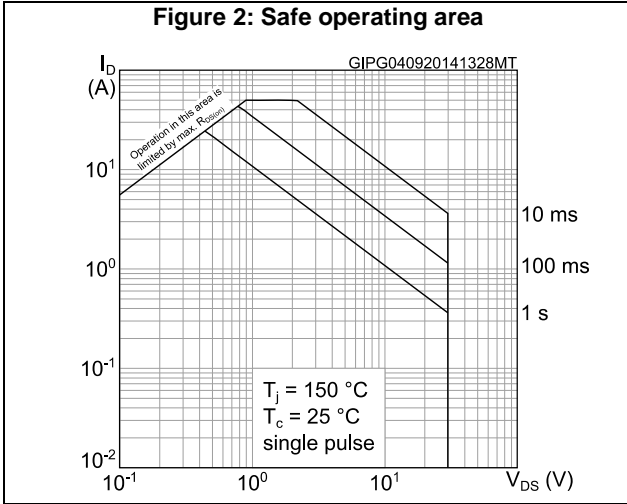


Figure 6: Gate charge vs gate-source voltage

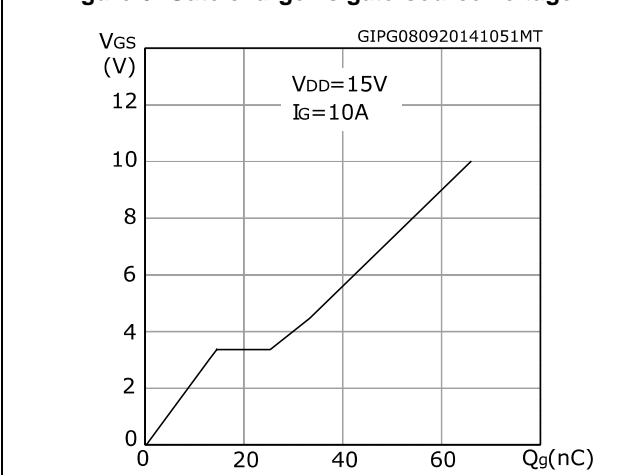


Figure 7: Static drain-source on-resistance

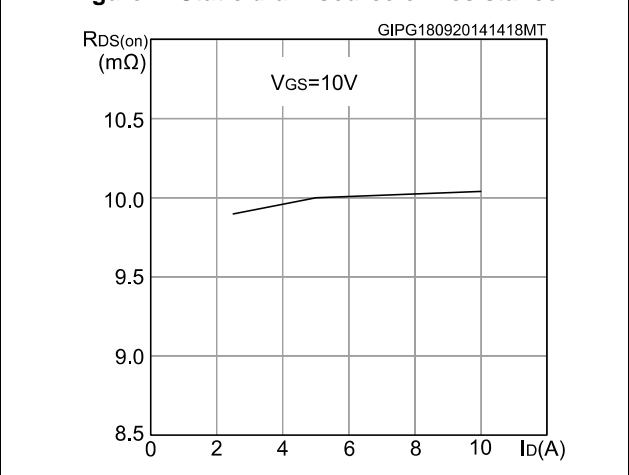


Figure 8: Capacitance variations

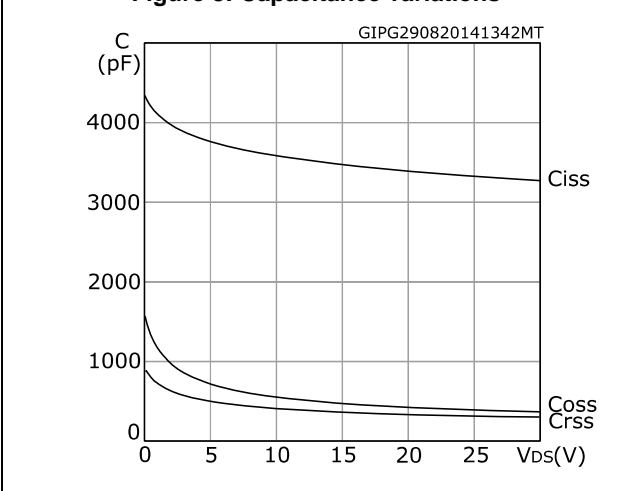


Figure 9: Normalized gate threshold voltage vs temperature

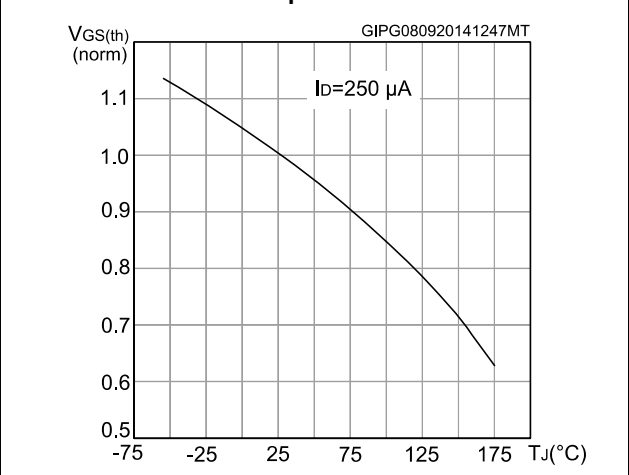


Figure 10: Normalized on-resistance vs temperature

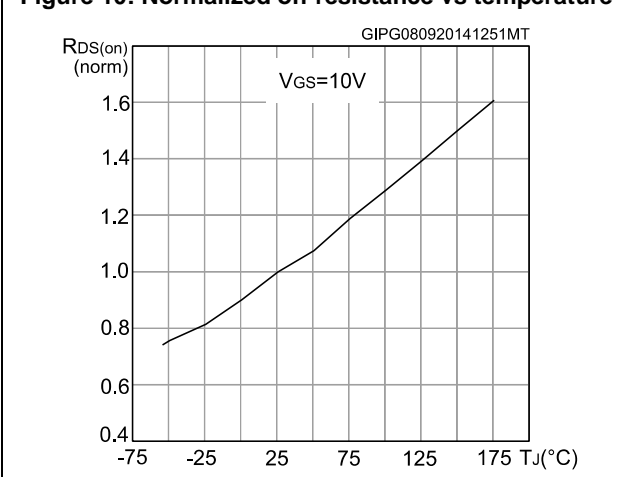


Figure 11: Normalized V(BR)DSS vs temperature

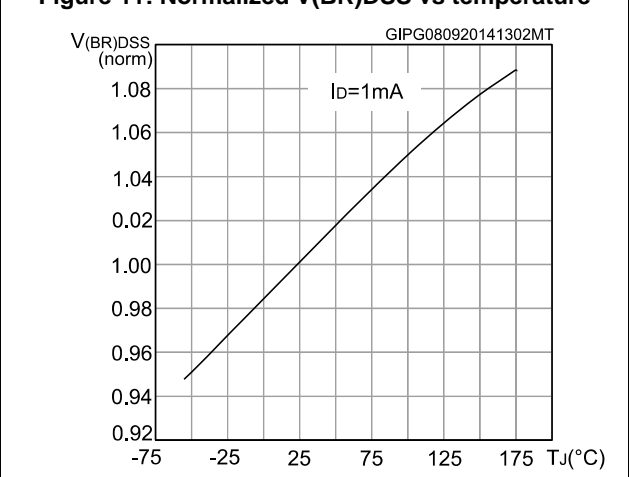
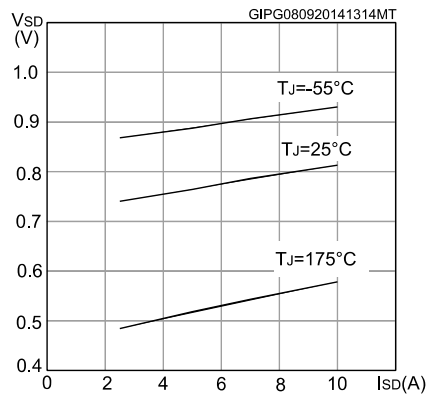


Figure 12: Source-drain diode forward characteristics



For the P-channel Power MOSFET, current and voltage polarities are reversed

3 Test circuits

Figure 13: Switching times test circuit for resistive load

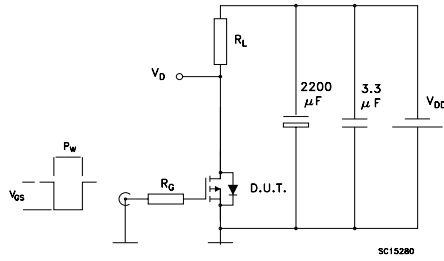


Figure 14: Gate charge test circuit

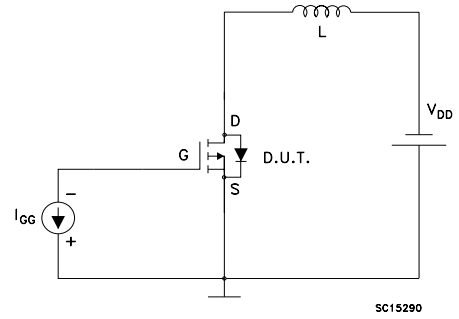
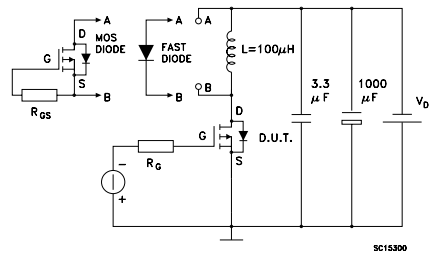


Figure 15: Source-drain diode forward characteristics



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 SO-8 package information

Figure 16: SO-8 package outline

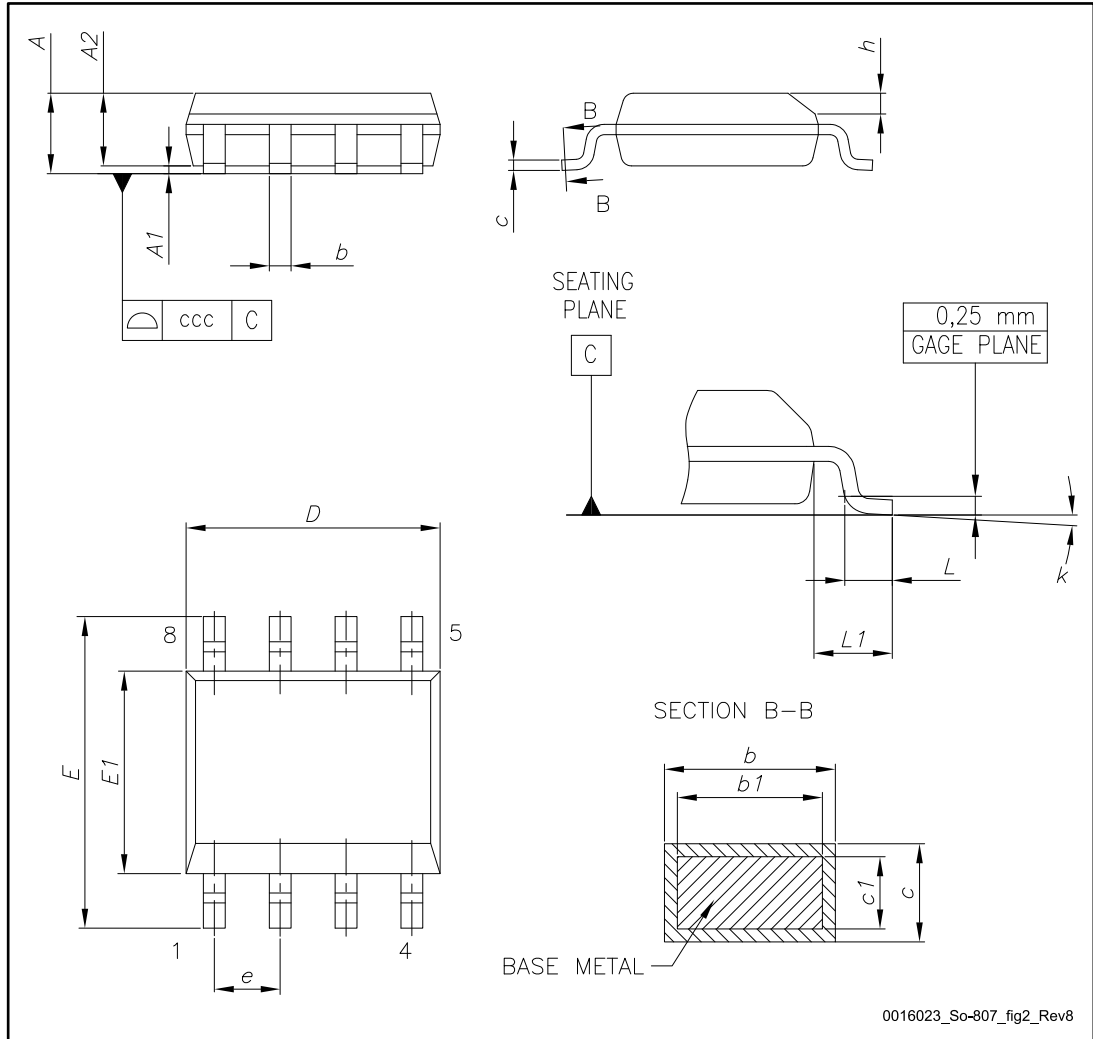
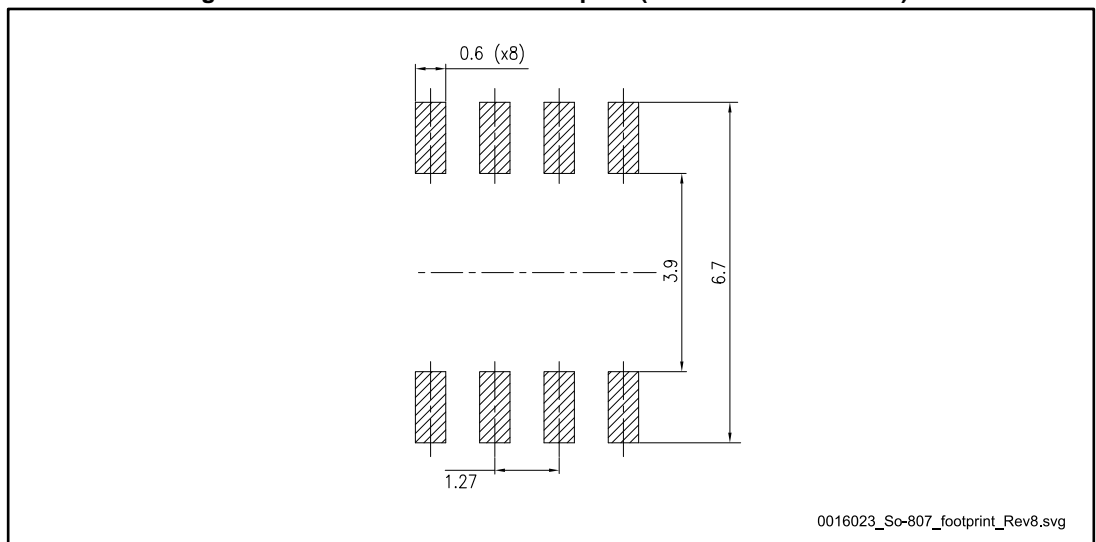


Table 8: SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 17: SO-8 recommended footprint (dimensions are in mm)



4.2 SO-8 packing information

Figure 18: SO-8 tape and reel dimensions

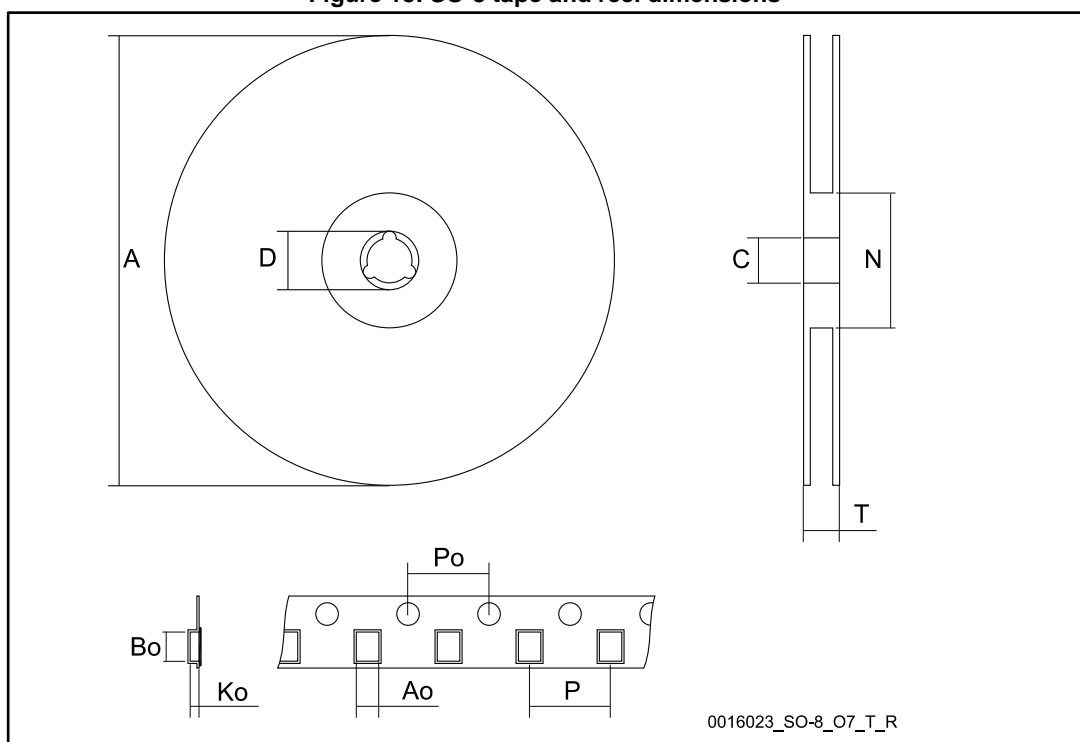


Table 9: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1	-	8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
06-May-2014	1	Initial release.
24-Sep-2014	2	Updated the title, the features and the description in cover page. Updated Section 1: "Electrical ratings", Section 2: "Electrical characteristics". Added Section 2.1: "Electrical characteristics (curves)" Minor text changes.
11-Jun-2015	3	Text and formatting changes throughout document. On cover page: - updated title description and Features table In Section 1 Electrical ratings: - updated Table Absolute maximum ratings In section 2.1 Electrical characteristics (curves) - updated Figure Safe operating area Updated and renamed Section 4.1 SO-8 package information (was SO-8 mechanical data)
24-Aug-2015	4	Updated Table 4: "On/off states".
06-Dec-2016	5	Updated $V_{GS(th)}$ in Table 4: "On/off states". Minor text changes.
03-Apr-2017	6	Added E_{AS} value in Table 2: "Absolute maximum ratings" .

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved