



# RF Power LDMOS Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

This 32 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2496 to 2690 MHz.

### 2600 MHz

- Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQA} = 400$  mA,  $V_{GSB} = 0.7$  Vdc,  $P_{out} = 32$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

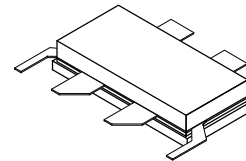
Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	14.7	45.4	7.8	-30.1
2590 MHz	15.0	45.1	8.1	-35.6
2690 MHz	15.0	45.6	7.5	-37.3

### Features

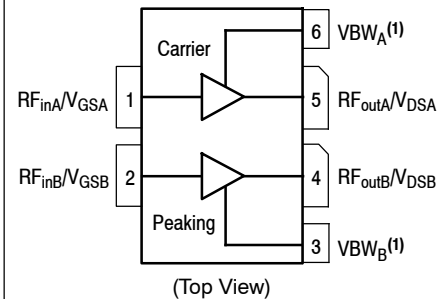
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

**A2T26H165-24SR3**

**2496–2690 MHz, 32 W AVG., 28 V  
 AIRFAST RF POWER LDMOS  
 TRANSISTOR**



**NI-780S-4L2L**



**Figure 1. Pin Connections**

- Device cannot operate with  $V_{DD}$  current supplied through pin 3 and pin 6.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +150	°C
Operating Junction Temperature Range (1,2)	$T_J$	-40 to +225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 73°C, 32 W Avg., W-CDMA, 28 Vdc, $I_{DQA} = 400$ mA, $V_{GSB} = 0.7$ Vdc, 2590 MHz	$R_{\theta JC}$	0.45	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**Off Characteristics (4)**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics - Side A, Carrier**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 70$ $\mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.6	2.2	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_D = 400$ mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.2	2.5	3.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10$ Vdc, $I_D = 700$ mAdc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

**On Characteristics - Side B, Peaking**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 120$ $\mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.6	1.6	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10$ Vdc, $I_D = 1200$ mAdc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
3. Refer to [AN1955](#), *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf> and search for AN1955.
4. Each side of device measured separately.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> <sup>(1,2)</sup> (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQA} = 400\text{ mA}$ , $V_{GSB} = 0.7\text{ Vdc}$ , $P_{out} = 32\text{ W Avg.}$ , $f = 2496\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	14.0	14.7	17.0	dB
Drain Efficiency	$\eta_D$	42.0	45.4	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.2	7.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	-30.1	-27.0	dBc

**Load Mismatch** <sup>(2)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $I_{DQA} = 400\text{ mA}$ ,  $V_{GSB} = 0.7\text{ Vdc}$ ,  $f = 2590\text{ MHz}$ , 10  $\mu\text{sec}$ (on), 10% Duty Cycle

VSWR 10:1 at 32 Vdc, 209 W Pulsed CW Output Power (3 dB Input Overdrive from 155 W Pulsed CW Rated Power)	No Device Degradation
--	-----------------------

**Typical Performance** <sup>(2)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQA} = 400\text{ mA}$ ,  $V_{GSB} = 0.7\text{ Vdc}$ , 2496–2690 MHz Bandwidth

$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	141	—	W
$P_{out}$ @ 3 dB Compression Point <sup>(3)</sup>	P3dB	—	191	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496–2690 MHz frequency range)	$\Phi$	—	-28	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	110	—	MHz
Gain Flatness in 194 MHz Bandwidth @ $P_{out} = 32\text{ W Avg.}$	$G_F$	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.01	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.007	—	dB/°C

**Table 5. Ordering Information**

Device	Tape and Reel Information	Package
A2T26H165-24SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	NI-780S-4L2L

- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- $P3dB = P_{avg} + 7.0\text{ dB}$  where  $P_{avg}$  is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

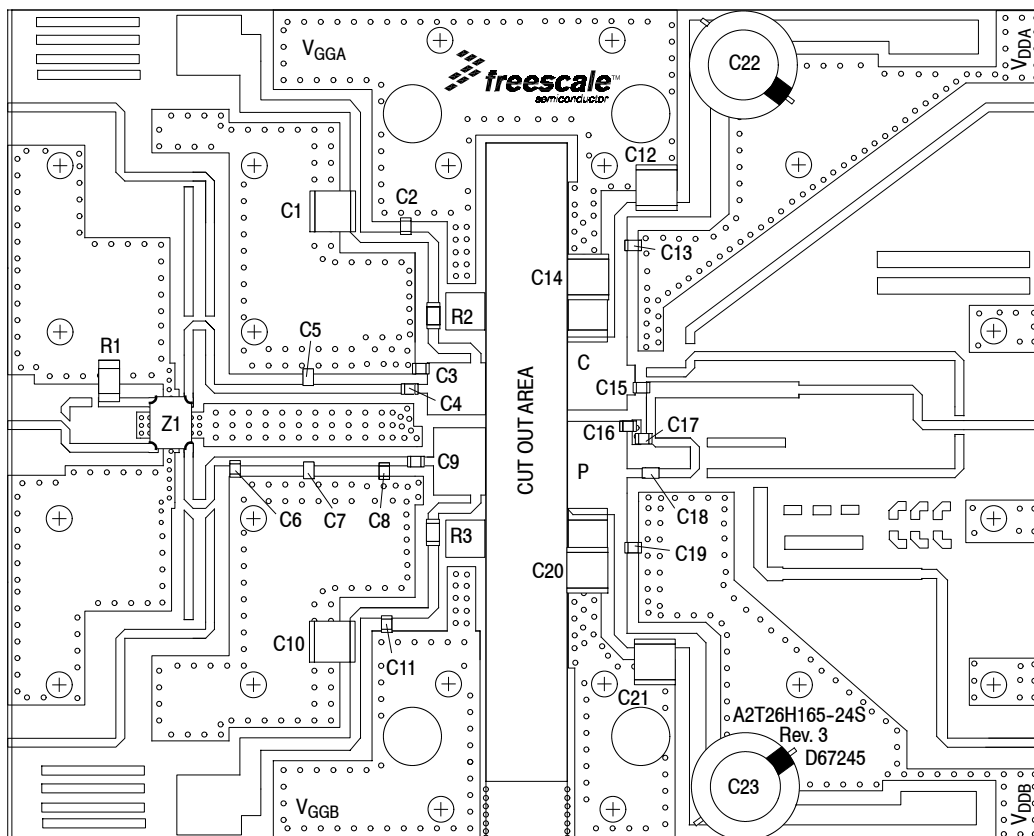


Figure 2. A2T26H165-24SR3 Test Circuit Component Layout

Table 6. A2T26H165-24SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C10, C12, C14, C20, C21	10 $\mu$ F Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C4, C9	7.5 pF Chip Capacitors	ATC600F7R5BT250XT	ATC
C3, C5	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C6	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
C7	0.8 pF Chip Capacitor	ATC600F0R8BT250XT	ATC
C8	0.7 pF Chip Capacitor	ATC600F0R7BT250XT	ATC
C11, C13, C18, C19	8.2 pF Chip Capacitors	ATC600F8R2BT250XT	ATC
C15	5.6 pF Chip Capacitor	ATC600F5R6BT250XT	ATC
C16	0.9 pF Chip Capacitor	ATC600F0R9BT250XT	ATC
C17	0.2 pF Chip Capacitor	ATC600F0R2BT250XT	ATC
C22, C23	470 $\mu$ F, 63 V Electrolytic Capacitors	MCGPR63V470M	Multicomp
R1	50 $\Omega$ , 10 W Termination	CW12010T0050GBK	ATC
R2, R3	6.2 $\Omega$ , 1/4 W Chip Resistors	CRCW12066R20FKEA	Vishay
Z1	2300–2700 MHz Band, 90°, 2 dB Hybrid Coupler	X3C25P1-02S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D67245	MTL

### TYPICAL CHARACTERISTICS

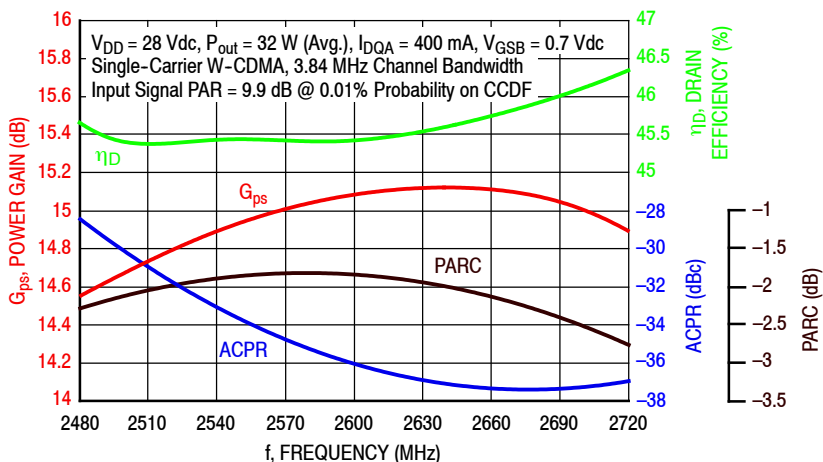


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 32$  Watts Avg.

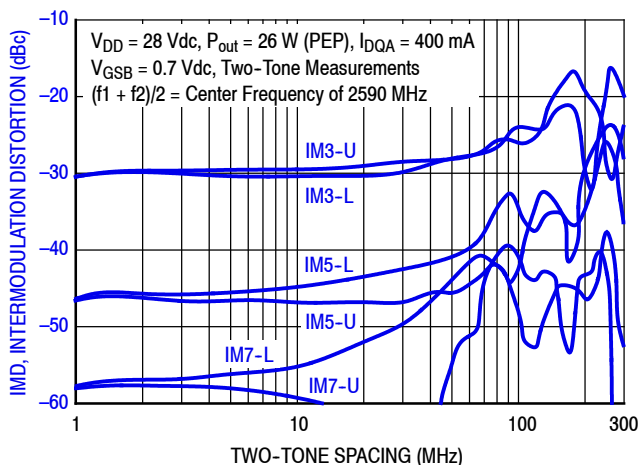


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

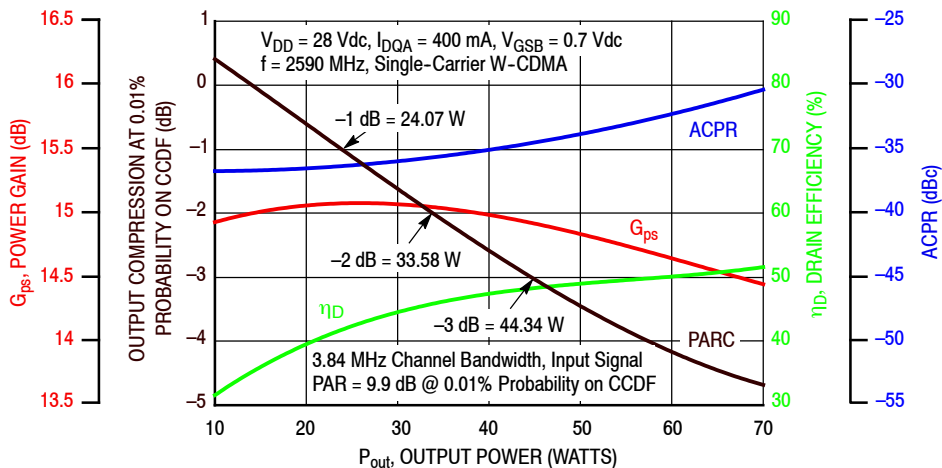
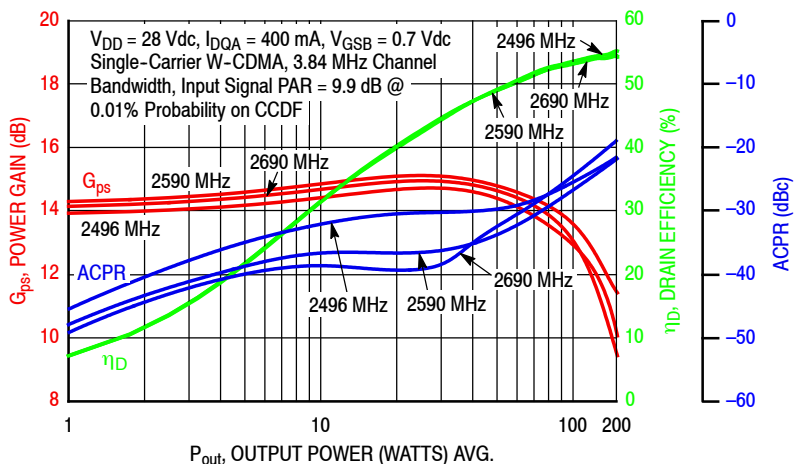
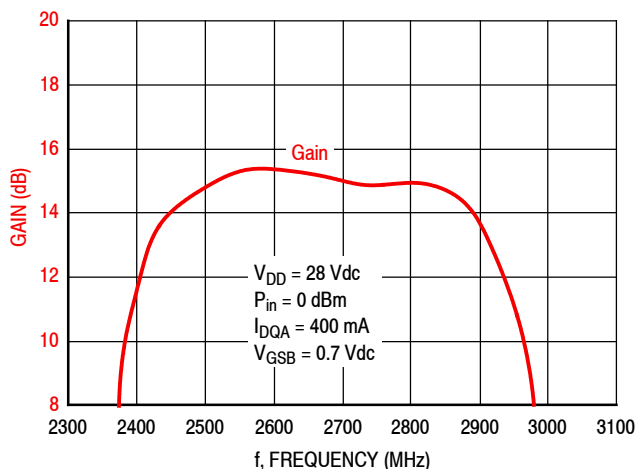


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

### TYPICAL CHARACTERISTICS



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 7. Broadband Frequency Response**

**Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQA} = 441$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	2.52 – j13.3	2.69 + j12.3	4.68 – j10.6	16.8	49.0	80	54.5	–12
2590	3.83 – j13.4	3.80 + j12.5	4.42 – j11.0	17.3	49.0	79	54.0	–12
2690	6.63 – j12.9	6.03 + j11.8	4.49 – j12.1	17.3	49.0	80	54.7	–13

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	2.52 – j13.3	2.62 + j12.6	4.48 – j11.2	14.6	49.7	94	55.5	–15
2590	3.83 – j13.4	3.91 + j12.9	4.33 – j11.7	15.0	49.7	94	55.0	–15
2690	6.63 – j12.9	6.61 + j12.3	4.49 – j12.4	15.1	49.7	94	56.0	–16

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 8. Carrier Load Pull Performance — Maximum Drain Efficiency Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQA} = 441$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	2.52 – j13.3	2.86 + j12.5	11.2 – j8.23	19.9	47.1	51	65.5	–20
2590	3.83 – j13.4	4.00 + j12.5	8.89 – j6.75	20.4	47.1	51	65.7	–21
2690	6.63 – j12.9	6.11 + j11.6	7.24 – j7.37	20.3	47.2	52	65.4	–21

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	2.52 – j13.3	2.75 + j12.7	10.5 – j8.22	17.7	47.9	62	66.7	–26
2590	3.83 – j13.4	4.07 + j12.9	8.73 – j7.25	18.2	47.9	62	66.8	–26
2690	6.63 – j12.9	6.61 + j11.9	7.11 – j7.64	18.2	48.0	62	66.4	–27

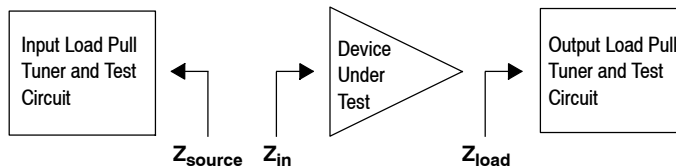
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.



**Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28$  Vdc,  $V_{GSB} = 0.6$  Vdc, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	4.38 – j16.1	4.48 + j16.2	3.21 – j10.5	13.4	51.2	131	54.4	–29
2590	9.10 – j16.7	8.22 + j16.7	2.85 – j10.4	13.4	51.1	129	52.0	–30
2690	14.3 – j9.20	14.6 + j10.3	2.86 – j11.6	13.4	51.2	133	52.9	–30

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	4.38 – j16.1	4.89 + j16.8	3.09 – j10.9	11.3	52.0	158	55.9	–35
2590	9.10 – j16.7	9.59 + j17.1	2.90 – j11.5	11.1	51.9	155	52.4	–35
2690	14.3 – j9.20	15.5 + j8.33	2.81 – j11.9	11.2	52.0	159	53.6	–35

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning**

$V_{DD} = 28$  Vdc,  $V_{GSB} = 0.6$  Vdc, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	4.38 – j16.1	4.03 + j16.3	7.25 – j9.48	14.5	49.7	94	62.3	–37
2590	9.10 – j16.7	7.54 + j17.0	6.65 – j9.17	14.4	49.8	95	61.3	–36
2690	14.3 – j9.20	14.3 + j12.1	5.07 – j8.46	14.5	49.7	94	62.5	–38

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2496	4.38 – j16.1	4.51 + j16.8	6.38 – j9.88	12.4	50.7	119	63.3	–43
2590	9.10 – j16.7	8.95 + j17.5	6.25 – j9.36	12.4	50.6	116	62.4	–43
2690	14.3 – j9.20	15.7 + j9.51	5.31 – j9.68	12.4	50.8	121	62.6	–42

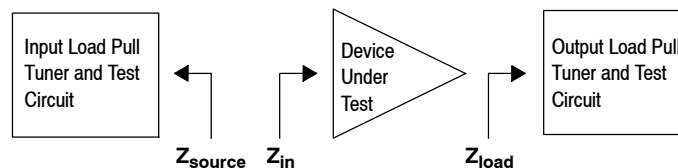
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.





P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2590 MHz

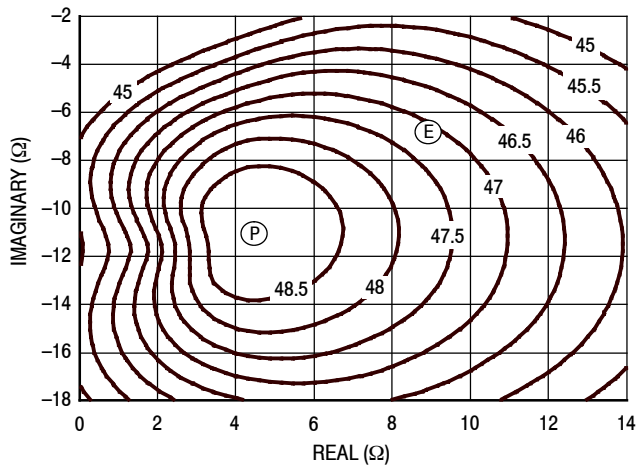


Figure 8. P1dB Load Pull Output Power Contours (dBm)

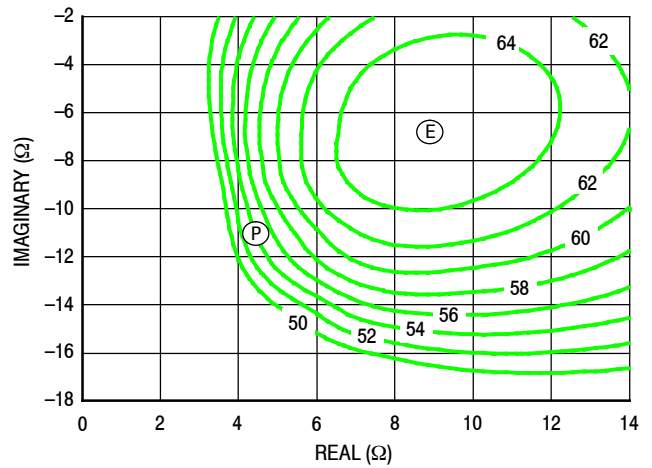


Figure 9. P1dB Load Pull Efficiency Contours (%)

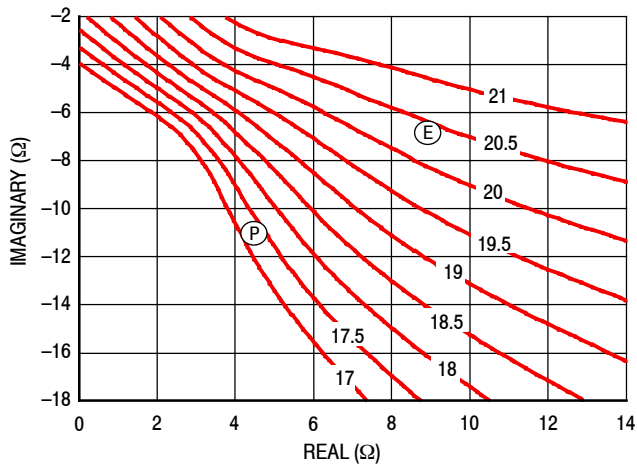


Figure 10. P1dB Load Pull Gain Contours (dB)

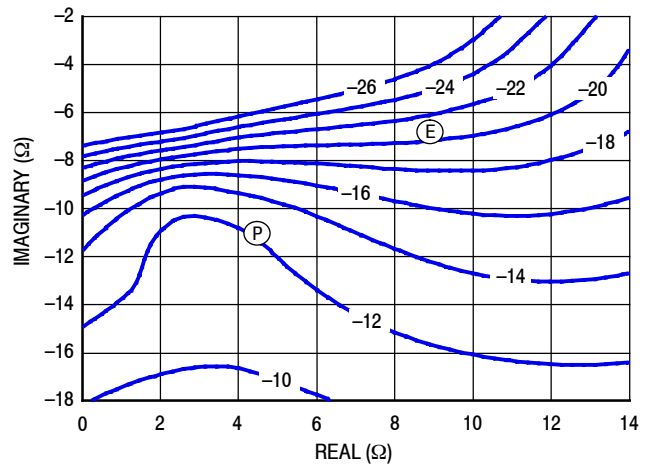


Figure 11. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2590 MHz

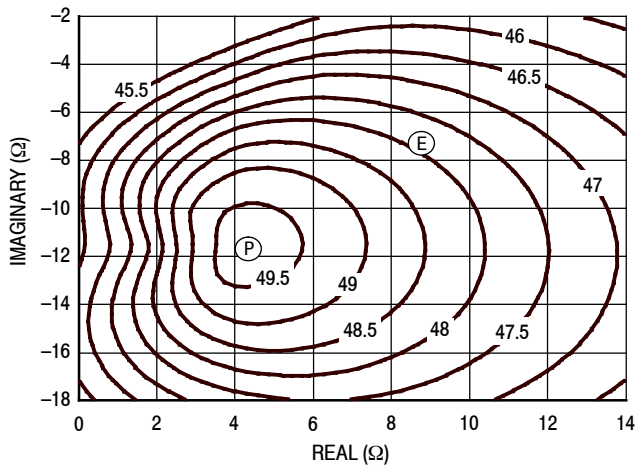


Figure 12. P3dB Load Pull Output Power Contours (dBm)

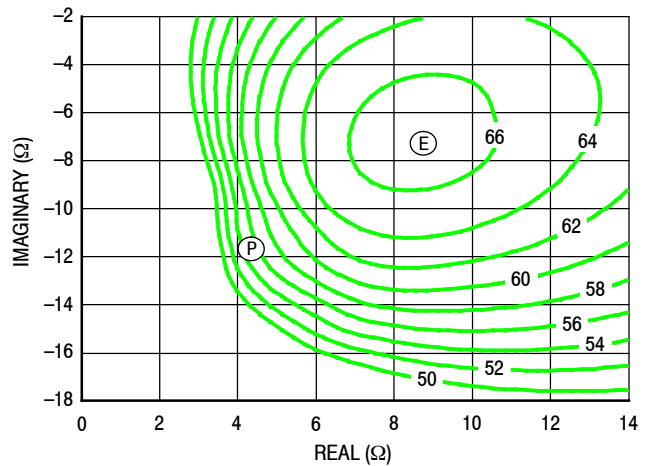


Figure 13. P3dB Load Pull Efficiency Contours (%)

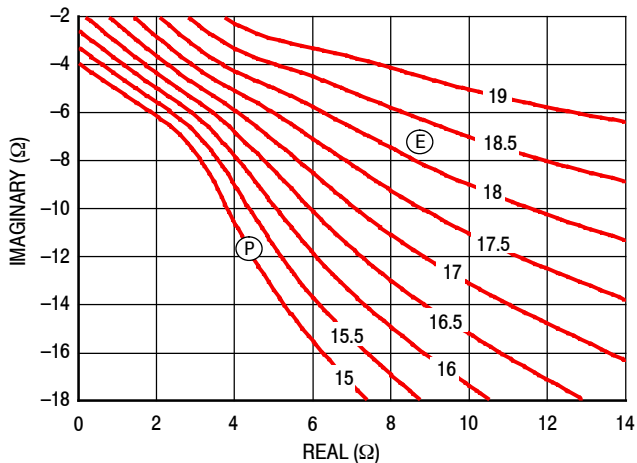


Figure 14. P3dB Load Pull Gain Contours (dB)

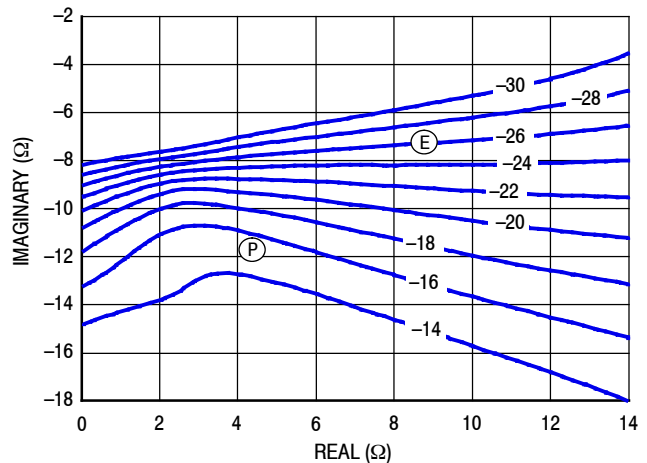


Figure 15. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2590 MHz

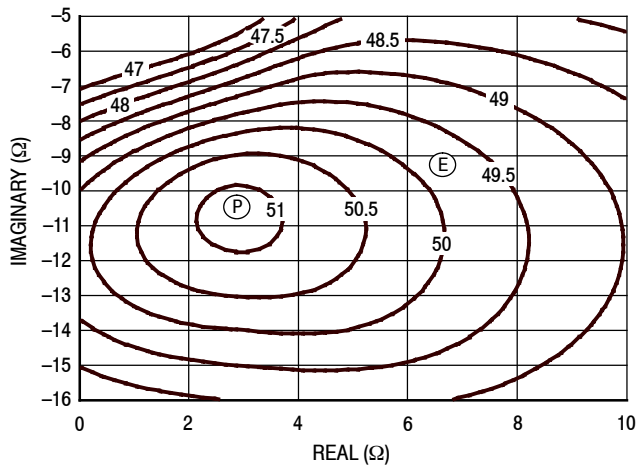


Figure 16. P1dB Load Pull Output Power Contours (dBm)

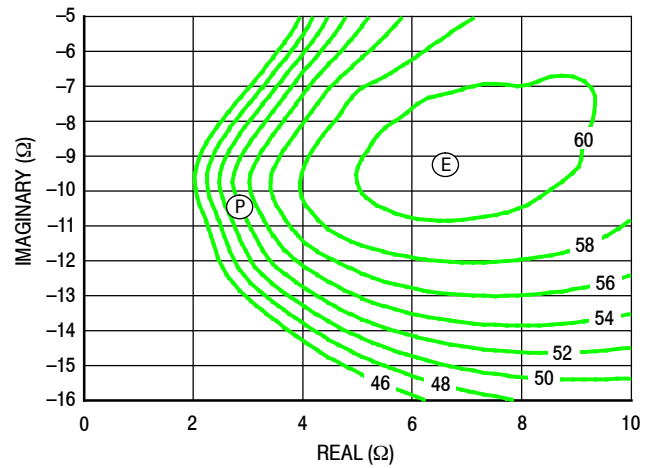


Figure 17. P1dB Load Pull Efficiency Contours (%)

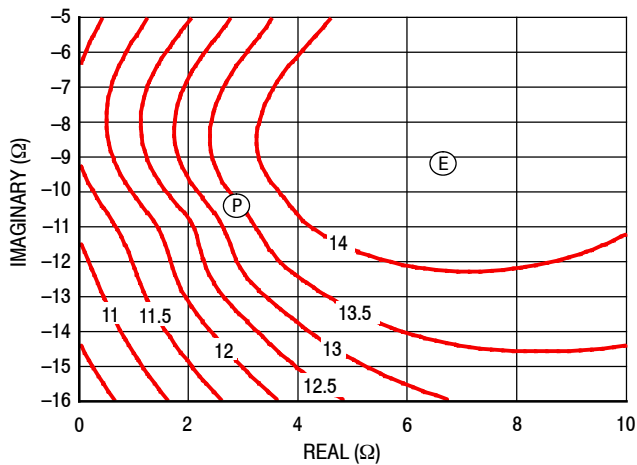


Figure 18. P1dB Load Pull Gain Contours (dB)

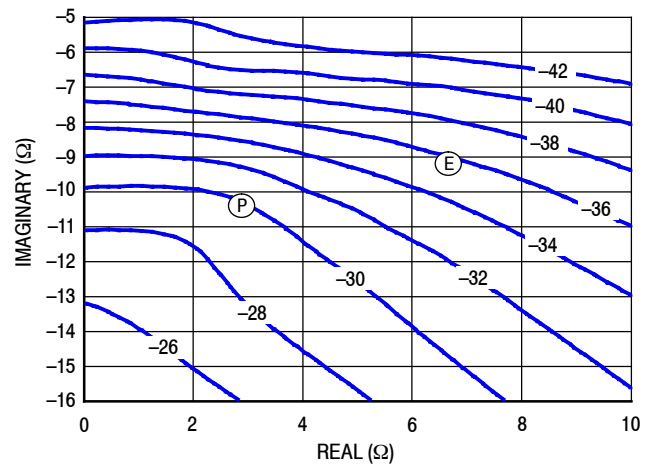


Figure 19. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2590 MHz

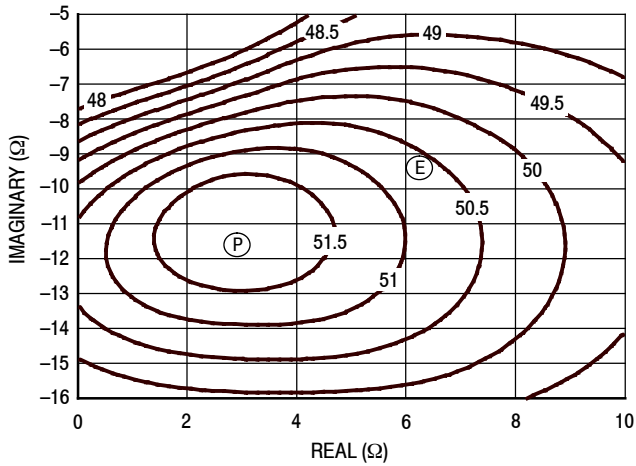


Figure 20. P3dB Load Pull Output Power Contours (dBm)

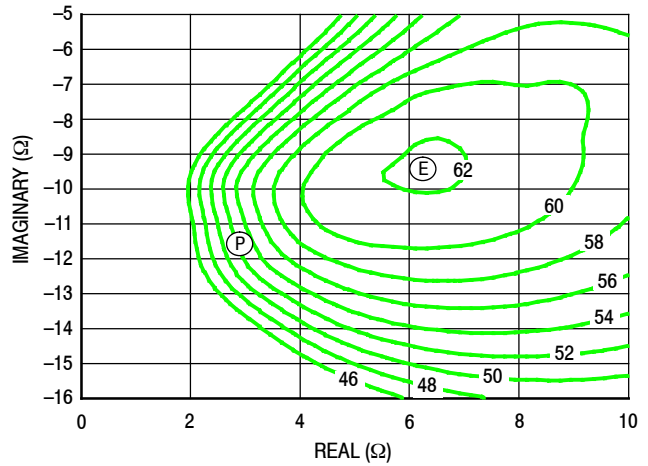


Figure 21. P3dB Load Pull Efficiency Contours (%)

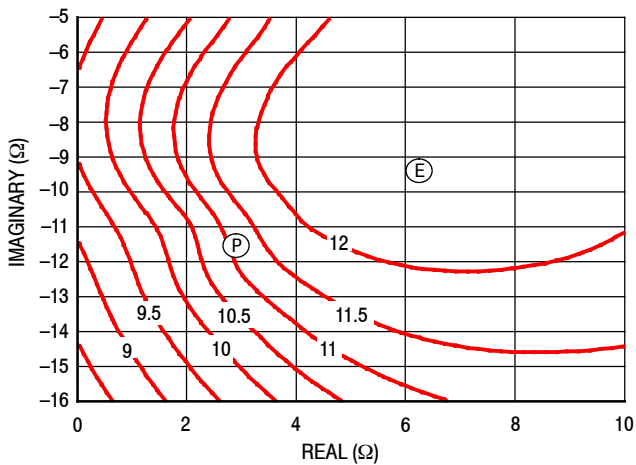


Figure 22. P3dB Load Pull Gain Contours (dB)

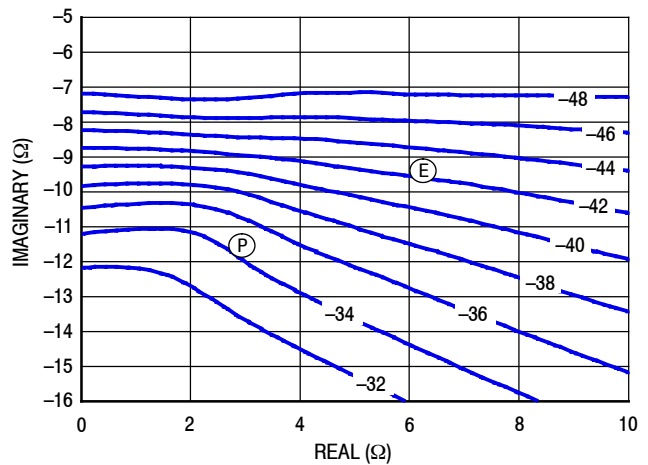
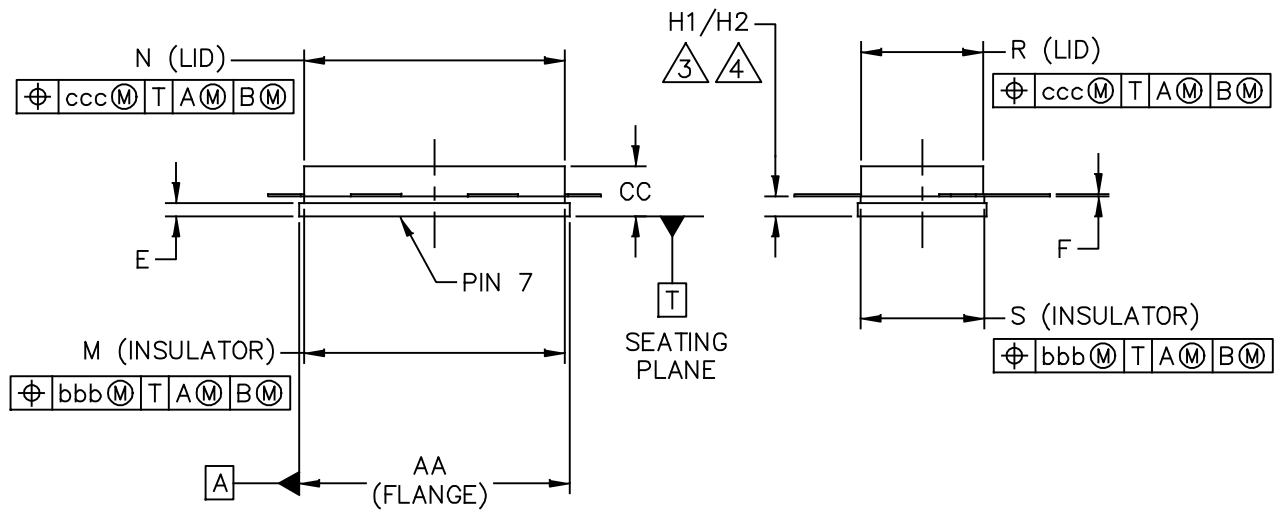
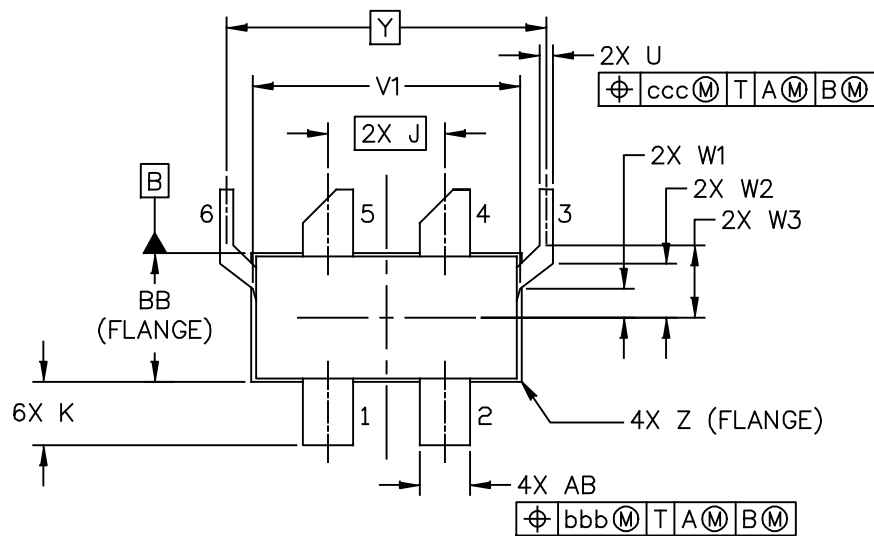


Figure 23. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE:  NI-780S-4L2L	DOCUMENT NO: 98ASA00674D STANDARD: NON-JEDEC	REV: 0  16 JAN 2014

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.080	.090	2.03	2.29
H1	.057	.067	1.45	1.70	W2	.155	.165	3.94	4.19
H2	.054	.070	1.37	1.78	W3	.210	.220	5.33	5.59
J	.350 BSC		8.89 BSC		Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	AB	.145	.155	3.68	3.94
N	.772	.788	19.61	20.02	aaa	.005		0.13	
					bbb	.010		0.25	
					ccc	.015		0.38	
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE:  NI-780S-4L2L					DOCUMENT NO: 98ASA00674D			REV: 0	
					STANDARD: NON-JEDEC				
					16 JAN 2014				

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

### Development Tools

- Printed Circuit Boards

### To Download Resources Specific to a Given Part Number:

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2015	• Initial Release of Data Sheet

## ***How to Reach Us:***

**Home Page:**  
[freescale.com](http://freescale.com)

**Web Support:**  
[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2015 Freescale Semiconductor, Inc.

