MC10H351

Quad TTL/NMOS to PECL* Translator

Description

The MC10H351 is a quad translator for interfacing data between a saturated logic section and the PECL section of digital systems when only a +5.0 Vdc power supply is available. The MC10H351 has TTL/NMOS compatible inputs and PECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2 V) and all inverting outputs to the PECL high logic state (≈ +4.1 V).

The MC10H351 can also be used with the MC10H350 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

Features

- Single +5.0 Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 nsec Typical
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

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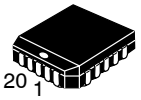
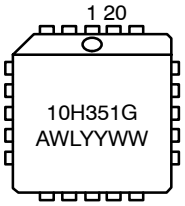


PLCC–20
FN SUFFIX
CASE 775–02

MARKING DIAGRAMS*



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H351FNG	PLCC–20 (Pb-Free)	46 Units/Tube
MC10H351FNR2G	PLCC–20 (Pb-Free)	500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

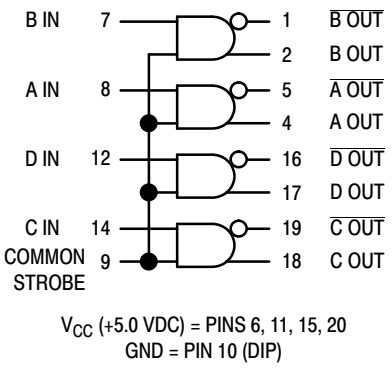


Figure 1. Logic Diagram

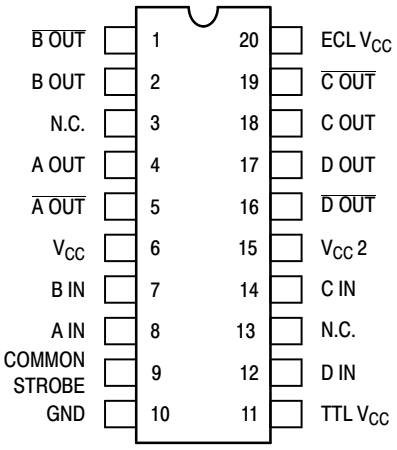


Figure 2. Dip Pin Assignment

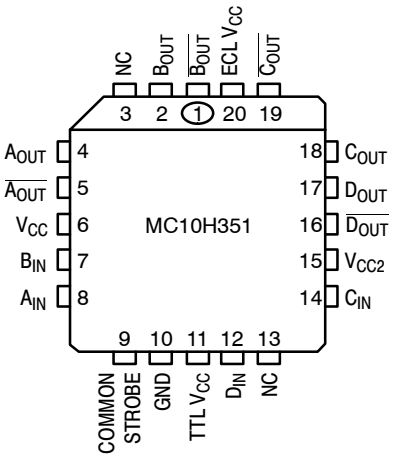


Figure 3. PLCC−20 Pin Assignment

Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit
V_{CC}	Power Supply	0 to +7.0	Vdc
V_I	Input Voltage (V_{CC} = 5.0 V)	0 to V_{CC}	Vdc
I_{out}	Output Current Continuous Surge	 50 100	mA
T_A	Operating Temperature Range	0 to +75	°C
T_{stg}	Storage Temperature Range Plastic	 −55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC1} = V_{CC2} = 5.0 V ± 5.0%)†

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
ECL	Power Supply	–	50	–	45	–	50	mA
TTL	Current	–	20	–	15	–	20	mA
I_R I_{INH}	Reverse Current Pins 7, 8, 12, 14 Pin 9	 – –	 25 100	 – –	 20 80	 – –	 25 100	μA
I_F I_{INL}	Forward Current Pins 7, 8, 12, 14 Pin 9	 – –	 −0.8 −3.2	 – –	 −0.6 −2.4	 – –	 −0.8 −3.2	mA
$V_{(BR)in}$	Input Breakdown Voltage	5.5	–	5.5	–	5.5	–	Vdc
V_I	Input Clamp Voltage (I_{in} = −18 mA)	–	−1.5	–	−1.5	–	−1.5	Vdc
V_{OH}	High Output Voltage (Note 1.)	3.98	4.16	4.02	4.19	4.08	4.27	Vdc
V_{OL}	Low Output Voltage (1)	3.05	3.37	3.05	3.37	3.05	3.37	Vdc
V_{IH}	High Input Voltage	2.0	–	2.0	–	2.0	–	Vdc
V_{IL}	Low Input Voltage	–	0.8	–	0.8	–	0.8	Vdc

†Each MECL 10H™ series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 Ω resistor to V_{CC} −2.0 Vdc.

*Positive Emitter Coupled Logic

1. With V_{CC} at 5.0 V. V_{OH}/V_{OL} change 1:1 with V_{CC}.

Table 3. AC PARAMETERS

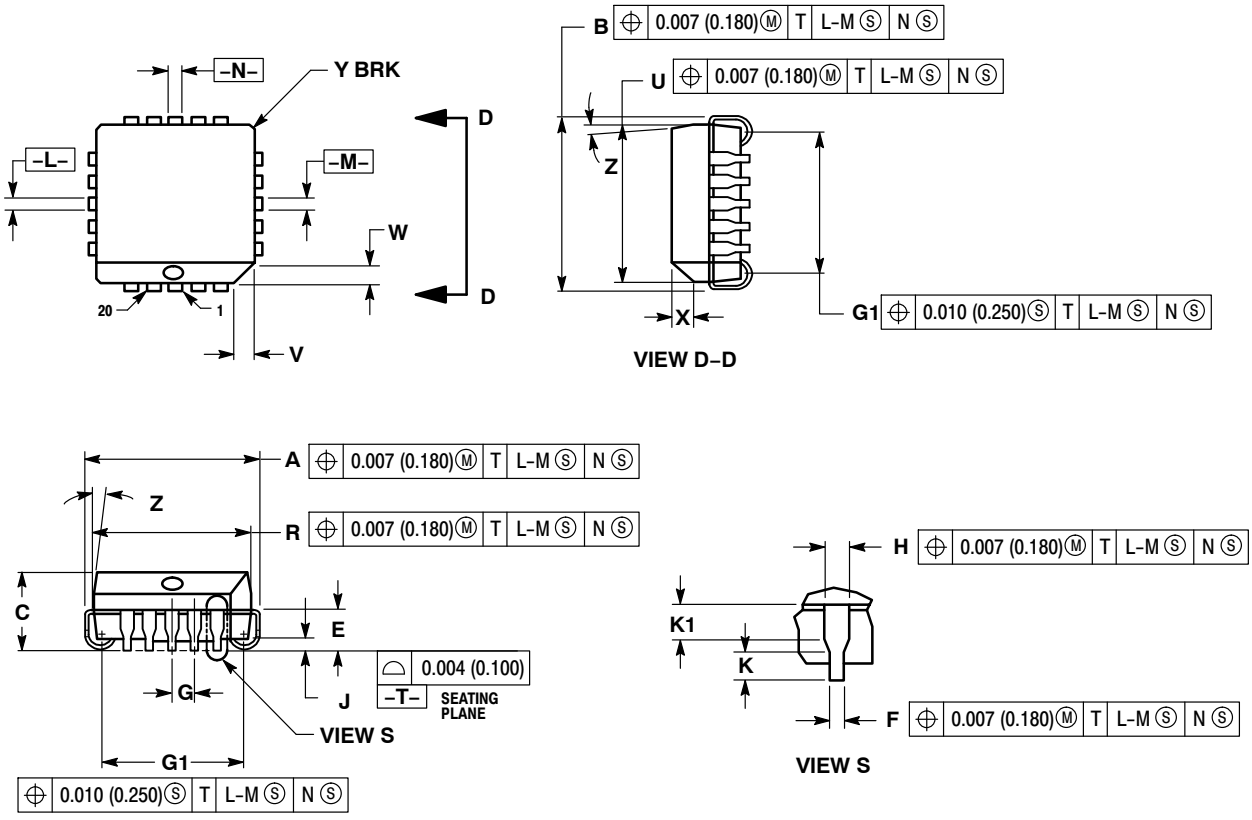
Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
t_{pd}	Propagation Delay (Note 2)	0.4	2.2	0.4	2.2	0.4	2.1	ns
t_r	Rise Time (20% to 80%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
t_f	Fall Time (80% to 20%)	0.4	1.9	0.4	2.0	0.4	2.1	ns
f_{max}	Maximum Operating Frequency	150	–	150	–	150	–	MHz

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Propagation delay is measured on this circuit from +1.5 V on the input waveform to the 50% point on the output waveform.

PACKAGE DIMENSIONS

20 LEAD PLLC
CASE 775−02
ISSUE F



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	−−−	0.51	−−−
K	0.025	−−−	0.64	−−−
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	−−−	0.020	−−−	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	−−−	1.02	−−−

PUBLICATION ORDERING INFORMATION

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