IS31LT3932

HIGH PF LOW THD UNIVERSAL LED DRIVER

December 2013

GENERAL DESCRIPTION

IS31LT3932 is a universal LED driver, which can operate in fly-back, buck-boost and buck convertor. For isolation fly-back, it can achieve high PF, high current accuracy, ±5% load and line regulation and wide voltage input voltage range, without loop compensation. For buck convertor, it also can achieve high PF, high current accuracy, high efficiency, good load and line regulation and wide voltage input voltage range, without loop compensation. With few external components.

IS31LT3932 has special power line sense and output voltage sense circuits, operates in primary feedback mode without Opto-coupler and achieve stable output current control without any loop compensation.

IS31LT3932 has multiple protections to improve the system reliability, including LED open circuit, LED short circuit, UVLO, OVP, current sense resistor short, the primary over current limit and over temperature protections.

FEATURES

- Universal isolation and non-isolation
- Single stage PFC fly-back
- No loop compensation required
- No Opto-coupler required
- ± 3%LED current accuracy
- ± 5% line regulation and load regulation
- Wide input voltage: 85Vac~265Vac
- Low start-up current (15μA)
- Valley turn-on MOSFET to achieve high efficiency for buck application
- Few external components
- UVLO,OCP,OVP and OTP protections
- SOP-8 package

APPLICATION

- LED bulb
- LED tube lamp
- LED PAR

TYPICAL OPERATING CIRCUIT

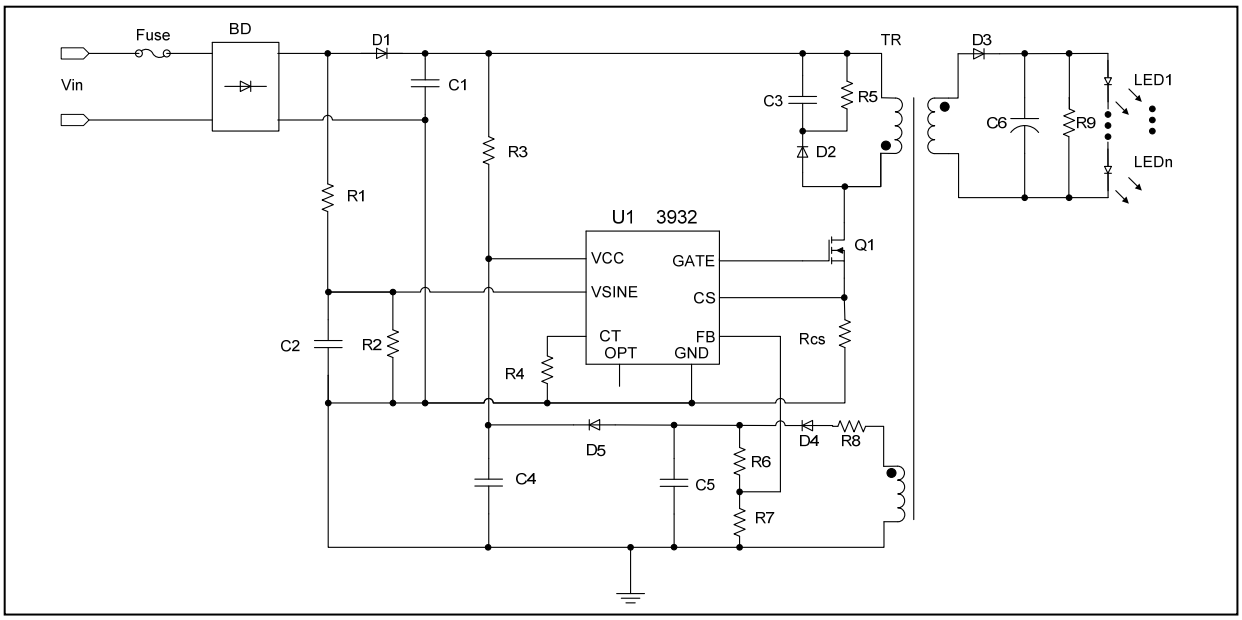
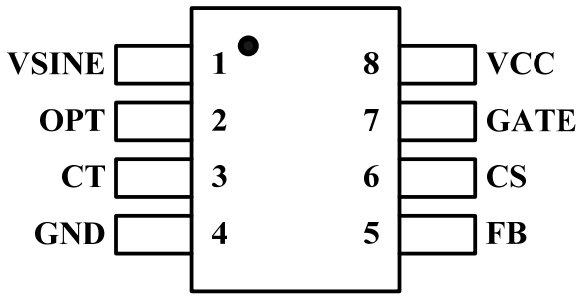


Figure 1 Typical isolated Operating Circuit

PIN CONFIGURATIONS

Package	Top View
SOP-8	

PIN DESCRIPTIONS

Pin	Name	Function
1	VSINE	Power line voltage detection.
2	OPT	Isolation and non-isolation option PIN. -Floating: fly-back and buck-boost -Connect to ground: buck sinusoidal.
3	CT	Time setting through the resistor between PIN and ground. -Isolation: operation cycle time setting $f = 50k \times \frac{V_{FB}}{0.8V} \times \frac{300}{Rct(k\Omega)}$ -Non-isolation: MOSFET turn-off delay time setting when FB detects zero voltage $Tdelay = 15 \times 10^{-6} \times R_{EXT}$
4	GND	Ground.
5	FB	Fly-back and buck-boost: operation frequency is regulated through this PIN to compensate output current Non-isolation: valley turn-on detect PIN, the external MOS turns on after a short delay when FB detects zero voltage
6	CS	MOSFET switching Current sense Pin.
7	GATE	Driver output to the external Power MOSFET.
8	VCC	Power supply input PIN, at a range of 8V~30V.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31LT3932-GRLS2-TR	SOP-8, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

VCC,GATE to GND	-0.3V ~ 36V
VSINE, OPT, CT, ISEN, FB to GND	-0.3V ~ 6.0V
Operating temperature, T_A	-40°C ~ +85°C
Storage temperature, T_{ST}	-60°C ~ +150°C
Junction temperature, T_{JMAX}	150°C
ESD (HBM) ESD (CDM)	2.5kV 750V

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC}=16V, V_{FB}=0V, V_{SINE}=0V, V_{CS}=0V, OPT Floating, R_{SET}=300kΩ, and T_A=25°C.

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{CC}	Power supply range		8		30	V
V_{OVP}	V_{CC} over voltage threshold			33.5		V
t_{OVP}	OVP reset time			160		ms
V_{ST}	Startup voltage	V_{CC} rising	14.5	16.0	17.5	V
V_{UVLO}	Under voltage lockout	V_{CC} falling	6	7	8	V
V_{GATE_CLP}	GATE output clamp voltage	V_{CC}=22V	14	16.5	19	V
I_{IN}	Quiescent current	without switching		750	1000	μA
I_{ST}	Startup current	V_{CC}=<Vth_s		15	20	μA
V_{CSTH}	Peak current voltage threshold		493	500	507	mV
t_{BLANK}	Current sense blanking time	V_{CS}=V_{CSTH}+50mV		550	800	ns
$V_{FB,OVP}$	FB pin over voltage threshold		1.2	1.24	1.28	V
$t_{FB,OVP}$	FB OVP reset time	t_{CYCLE} = 20μs	140	160	180	ms
V_{OCP}	Over current voltage threshold		650	700	750	mV
T_{OCP}	OCP reset time		35	40	45	ms
t_{OFF_MIN}	Minimum TOFF time	OPT=0		1		μs
t_{CYCLE}	Operating cycle	V_{FB}=0.8V, R_{CT}=300kΩ	19.6	20	20.4	μs
		V_{FB}=1.04V, R_{CT}=300kΩ	15.2	15.6	16.0	μs
		V_{FB}=0.56V, R_{CT}=300kΩ	27.7	28.3	28.9	μs
V_{OCP}	Over current voltage threshold			700		mV
t_{OCP}	OCP reset time			40		ms
t_R	Rise time	V_{CC}=16V,C_L=1nF, V_{GATE} from 0 to 7V		75	90	ns
t_F	Fall time	V_{CC}=16V,C_L=1nF		40	50	ns
T_{SD}	Thermal shutdown threshold			150		°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
t_{RE}	CS short protection reset time		35	40	45	ms

TYPICAL PERFORMANCE CHARACTERISTICS

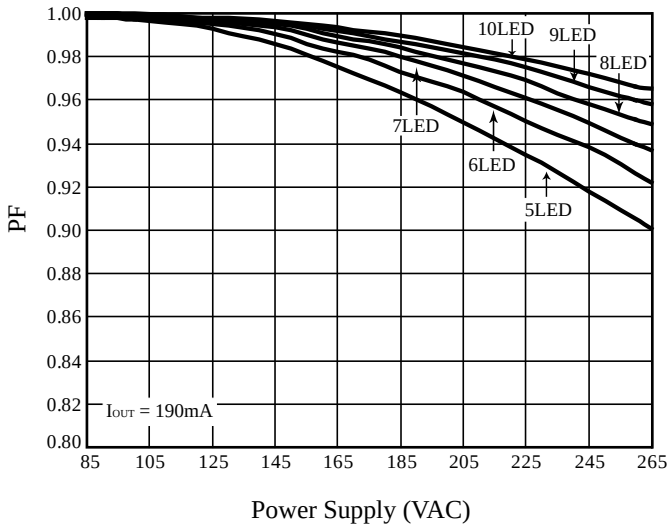


Figure 2 PF vs. Power Supply

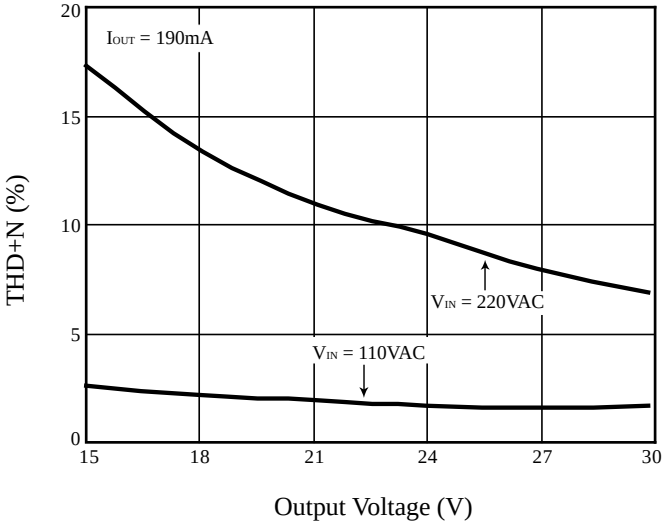


Figure 3 THD+N vs. Output Voltage

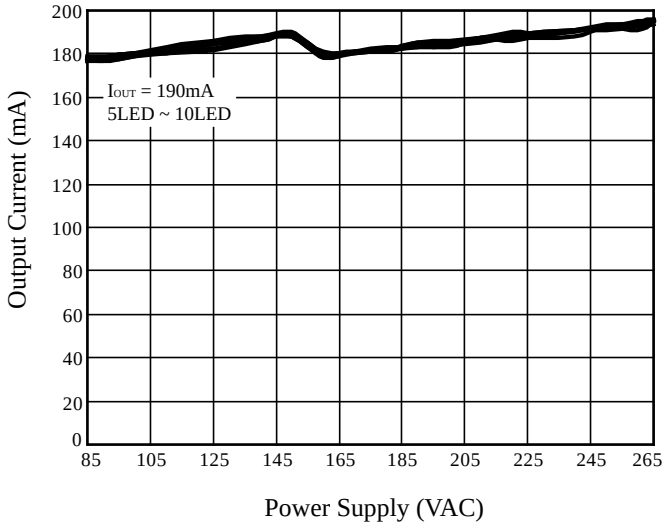


Figure 4 Output Current vs. Power Supply

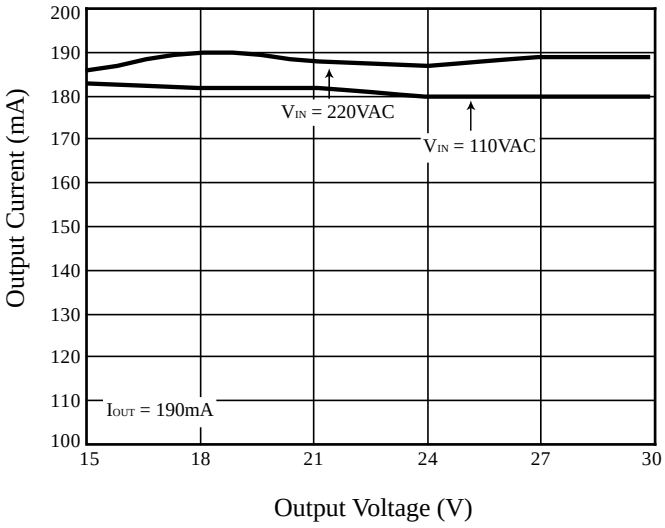


Figure 5 Output Current vs. Output Voltage

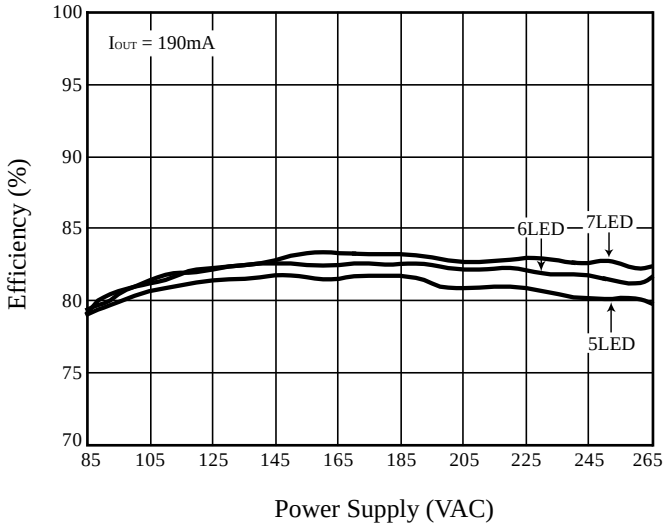


Figure 6 Efficiency vs. Power Supply

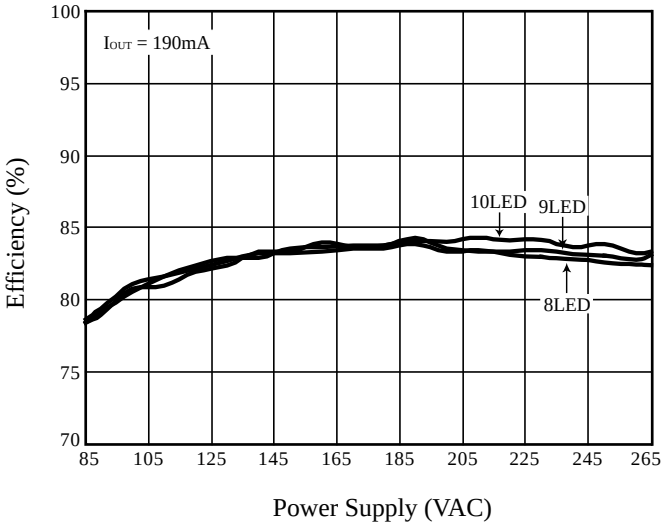
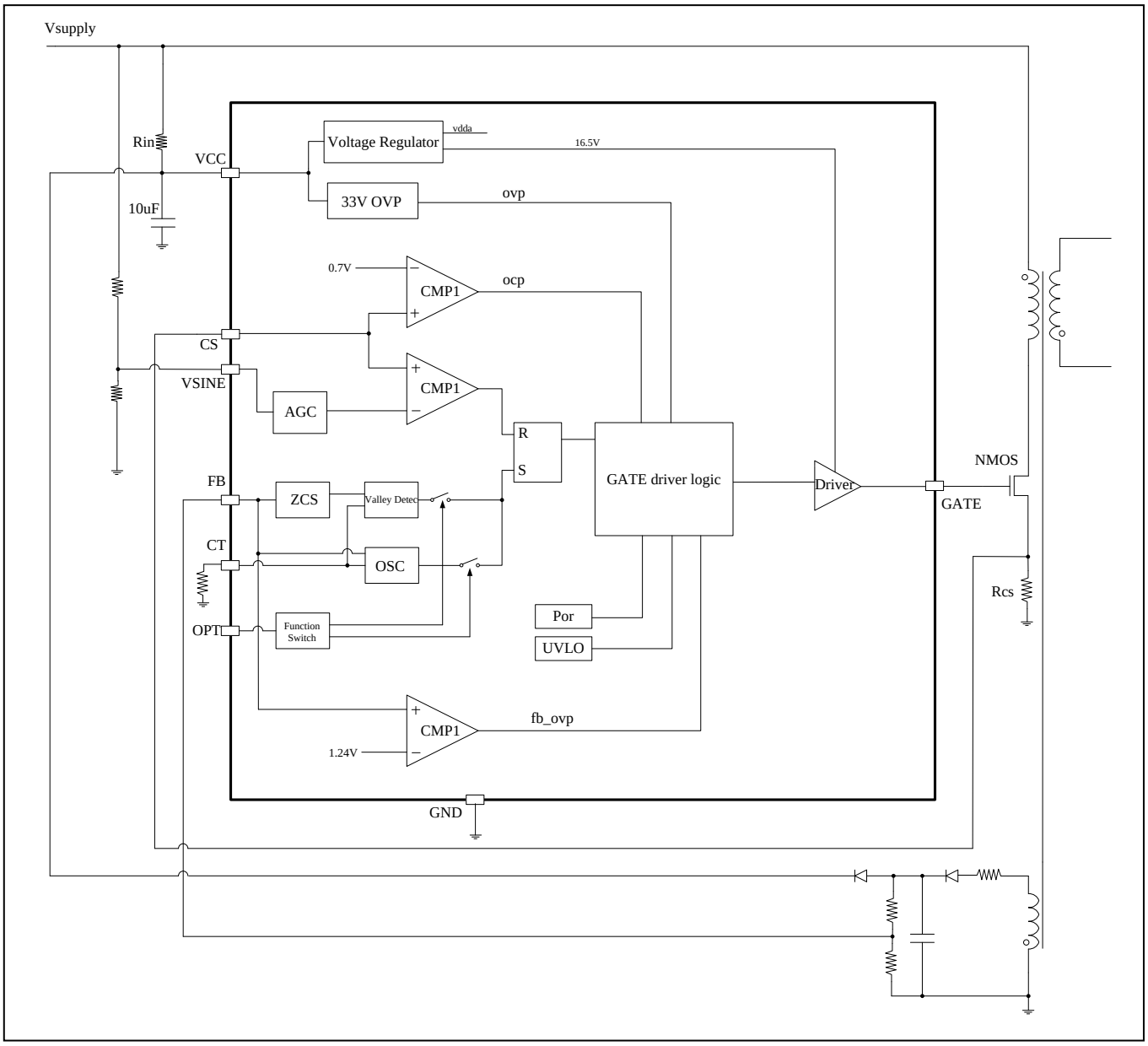


Figure 7 Efficiency vs. Power Supply

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

Base on Figure 17 & Figure 18 Typical Application Circuit

FUNCTION DESCRIPTION

For fly-back or buck-boost when OPT is floating, the operation cycle will be set by the external resistor of CT-PIN through the output clock of OSC block , the GATE will be turned on at the rising edge of clock and turn off when CS voltage hit AGC output. Also, other signal, such as OCP and OVP, can turn off GATE directly.

AGC output is a synchronized half-sinusoid waveform with constant peak, as the input half-sinusoid with variable peak.

For buck when OPT connects to ground, the only difference is that GATE turn on is determined by the Zero-Cross-Switch block with a short delay of Valley Detect, but not the former rising-edge of clock.

STARTUP VOLTAGE

When the rectified AC voltage is applied to the R6, R10 & C9 a startup circuit, this C9 will be started to be charged. The IC will start working when the voltage of C9 reaches 16V of the start threshold for the IC. The value of R6 and R10 & C9 can be determined by the input voltage & start threshold voltage. The bigger values of R6 and R10 used will increase the startup time, but can reduce the loss of power consumption at the whole operation time. R6 & R10 =300kΩ, 1206 size is recommend. A low ESR capacitor of 4.7~10μF, 50V is recommended for C9.

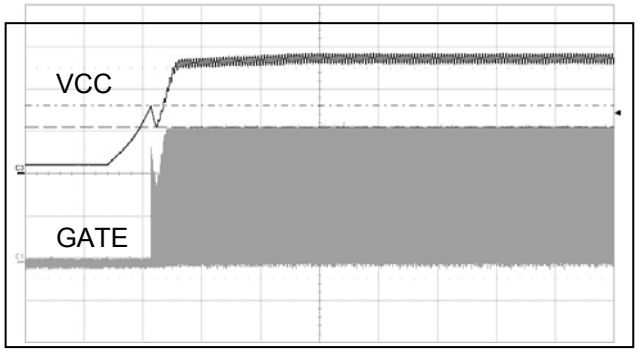


Figure 8 Start-up

SOFT START CONTROL

When Vcc is reached the start the threshold voltage, the CS voltage is forced increasing from low limit level go to 0.5V cycle by cycle. So the switching current will be slow increased to achieve the soft start.

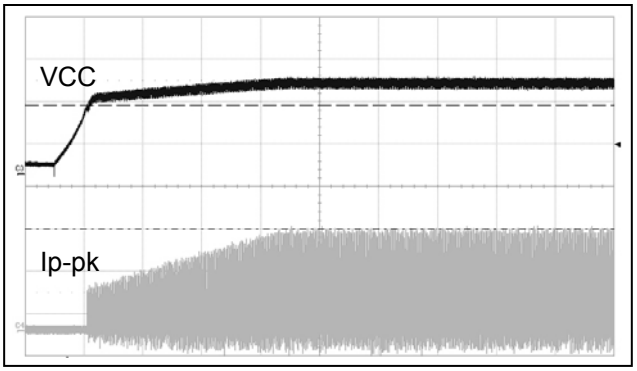


Figure 9 Soft Start

GATE OUTPUT VOLTAGE CLAMP

IS31LT3932 has the voltage clamp function for GATE output. When the voltage of VCC is smaller than the V_{GATE_clp} threshold, the voltage of GATE output is about VCC. When VCC voltage is greater than V_{GATE_clp} threshold, the GATE voltage is clamped same with V_{GATE_clp} threshold voltage.

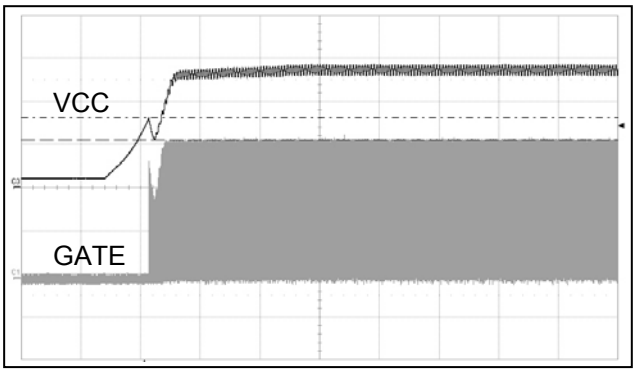


Figure 10 Gate Voltage Clamped

VSINE DETECTION NETWORK AND ACTIVE PFC

The Pin VSINE is used to detect the input voltage which controls the peak current waveform in the inductor to follow Line AC voltage and let inside AGC makes the peak current of inductor constant, so that allows the IS31LT3932 to actively correct the power factor and constant power during operation. The maximum input voltage of the VSINE pin is 2.5V.

This resistor network should be computed such that the peak input voltage condition corresponds to 0.75~2.5VDC. When input AC is 265VAC, the peak voltage is 374.7V and the output of the network should be 2.4V, thus values of R5+R9=2MΩ, its size is 1206 and R18 = 13kΩ are appropriate and recommend to use 1% of tolerance resister. A small1nF capacitor, C7, is used to filter high frequency noise.

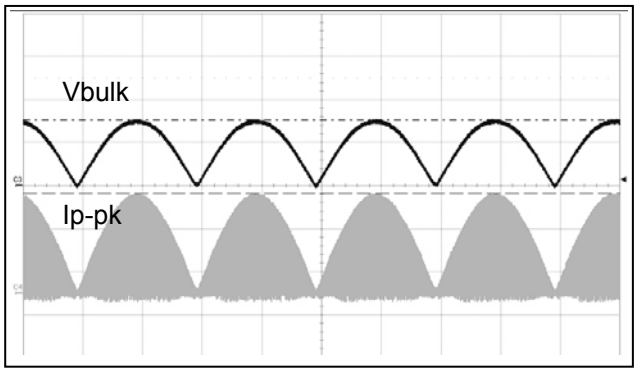


Figure 11 Active PFC

OPERATING FREQUENCY

The working frequency is set by connecting a resistor between the CT pin and ground. The relationship between the frequency and resistance is:

$$f = 50k \times \frac{V_{FB}}{0.8V} \times \frac{300}{R_{CT}(k\Omega)}$$

OUTPUT OPEN CIRCUIT PROTECTION

Open circuit protection is realized by connecting a resistor network to the FB pin. By sensing the voltage of the auxiliary winding, which is proportional to the output voltage, the IS31LT3932 detects when there is an open circuit condition on the secondary and stop the switching action. The threshold voltage for the FB pin is 1.24V. When it is great than 1.24V, the GATE will output the 160ms low level signal to tuned off the MOSFET until the fail is removed.

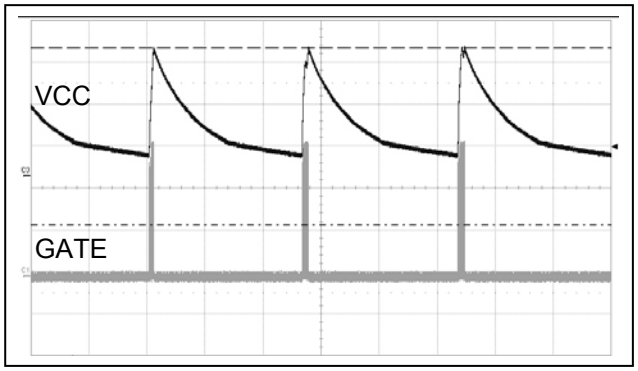


Figure 12 OVP

UVLO PROTECTION

If the output of the circuit is suddenly shorted, then the voltage of the secondary winding is quickly reduced, and also it will be reflected into the auxiliary winding, so VCC of the device will drop rapidly. If the VCC voltage drops below the UVLO' threshold, the device will stop switching, thus indirectly achieving output short circuit protection and UVLO protection.

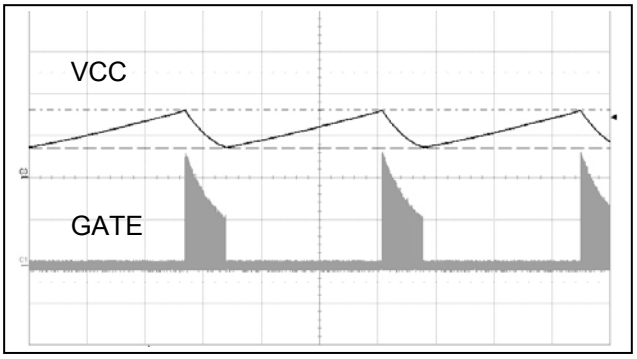


Figure 13 Output Short Circuit Protect

The device will not operate if the VCC voltage is below the under-voltage lockout threshold cycle by cycle, until the VCC voltage is higher than the threshold, and then the device will start working again.

CS OVER CURRENT AND SHORT PROTECTION

If the output LEDs is shorted or some components were failed, Vcs voltage will rise very quickly. If this Vcs voltage is over than 0.7V threshold voltage, the MOSFET gate will be turned off 40ms and then continue keep detecting Vcs voltage cycle by cycle until the fault condition removed.

If the CS pin is shorted, others IC no longer detect the peak switching current, but 3932 IC integrates a maximum duty cycle protection circuit when if a duty cycle occupied up to 100% within one logic stage, the Gate pin will output a low level 40ms to turn off MOSFET until the fault removed.

Please see Figure 13 Output Short Circuit Protection.

LINE & LOAD REGULATION

In order to ensure that at different AC line voltage, the output current is constant, an AGC (Automatic Gain Control) is used, its output signal is as CS threshold voltage and set threshold peak voltage is 0.5V as typical value. The transformer peak current IL is controlled by CS threshold, if the peak current of transformer is constant by mean of changing operation frequency to maintain a constant current & AGC in DCM model, then the input power is constant in all input voltage range and output current is constant in all input voltage range.

As the number of LED lights load changed, the output voltage will change, that caused the transformer auxiliary winding voltage will follow this changes.

This voltage can be determined the number of LED and is feed into the FB pin for proportional adjusting the operation frequency of IC to achieve constant output current when loading changed. Please refer to the specific operating frequency calculation description.

The FB pin voltage is in the range of 0.5~1.25V, the control voltage is proportional to the frequency and FB, when the FB voltage is less than 0.5V, the frequency remained unchanged.

When 3932 works under BUCK application, Pin 2 will be connected to ground. The inductor current works on the CRM model, the Iout current is 0.5IL in the single working cycle. The solid line is the inductor current waveform when the MOS transistor is turned on, the dotted line is the inductor current for the MOS transistor is turned off. The AGC function can maintain a constant IL and work at CRM mode, then the output current Iout will be constant.

To detect the auxiliary winding voltage when the zero current happened and turn on MOSFET as soon, the zero current switching can be achieved; also the CRM model can be achieved. System works in FM mode (Figure 14).

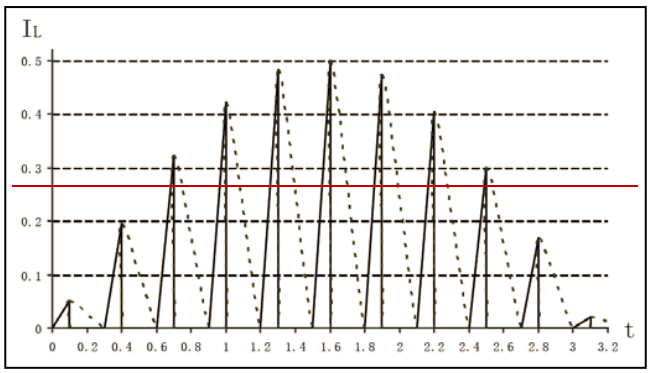


Figure 14 Inductor Switching Current

PCB DESIGN CONSIDERATIONS

(1) As Figure15 and 16 shows, components such as C7, R17, R18, R20, R21, R22, R23, C9 etc. which are connected to the IC should be mounted as close to the IC as possible.

(2) Bypass capacitors should always be mounted as close to the IC as possible.

(3) Switching signal traces should be kept as short as possible and not be routed parallel to one another so as to prevent coupling.

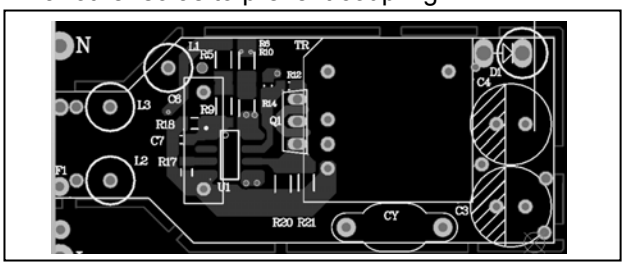


Figure 15 Typical PCB Top Layer

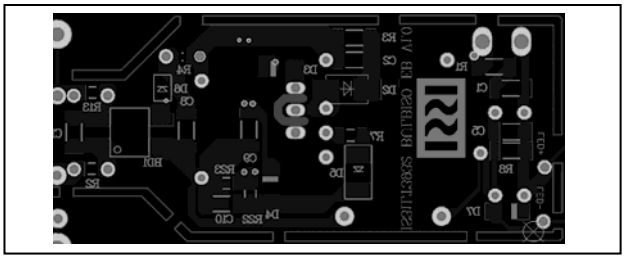


Figure 16 Typical PCB Bottom Layer

TYPICAL APPLICATION CIRCUIT

It is suited to full input voltage 15~30V-0.2A output applications

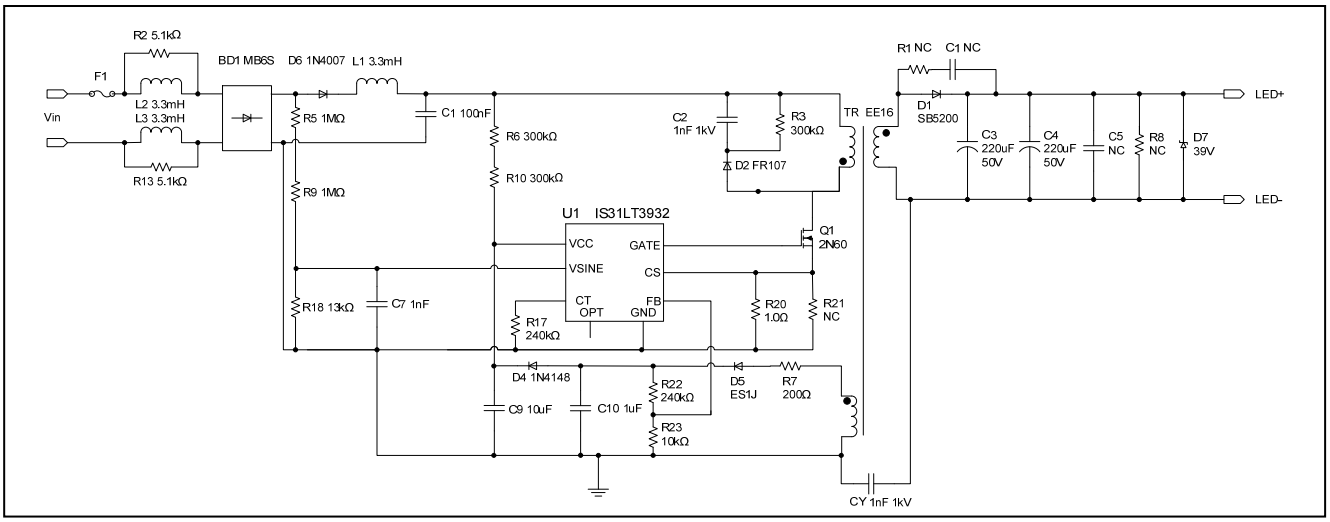


Figure 17 Typical Isolated Application Schematic

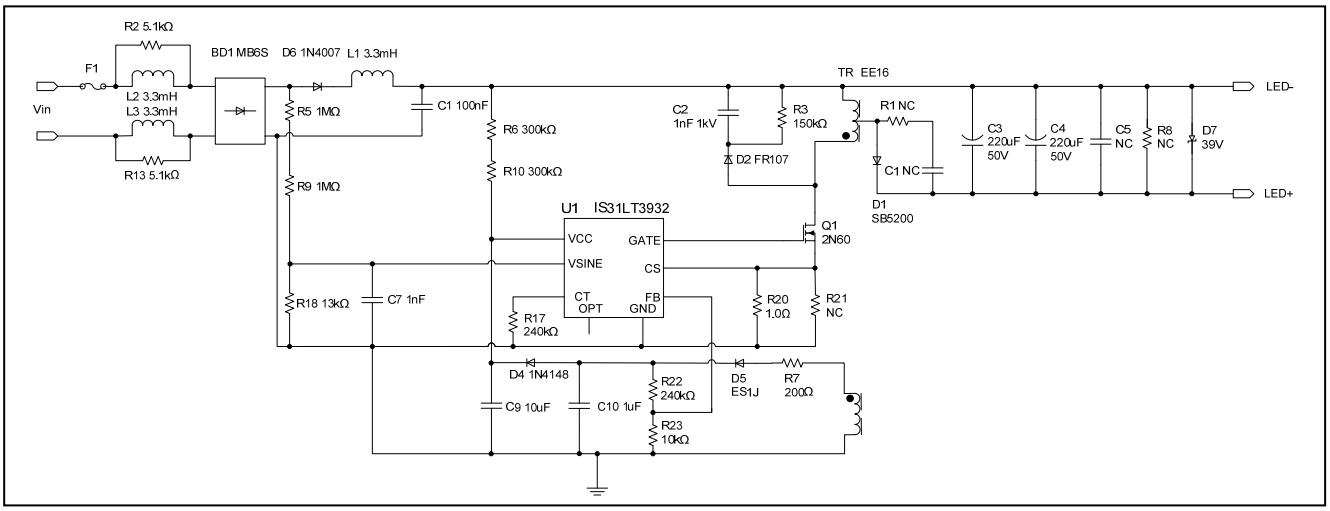


Figure 18 Typical Non-Isolated Application Schematic

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

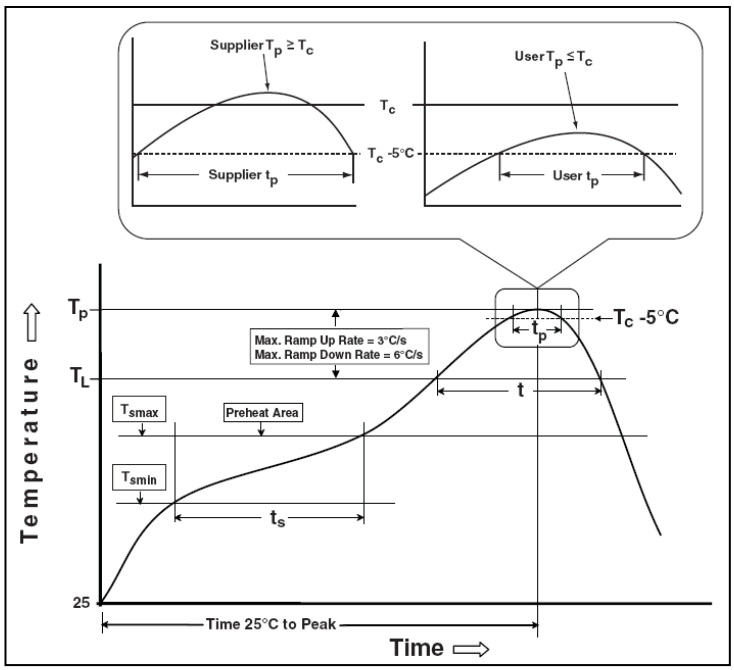
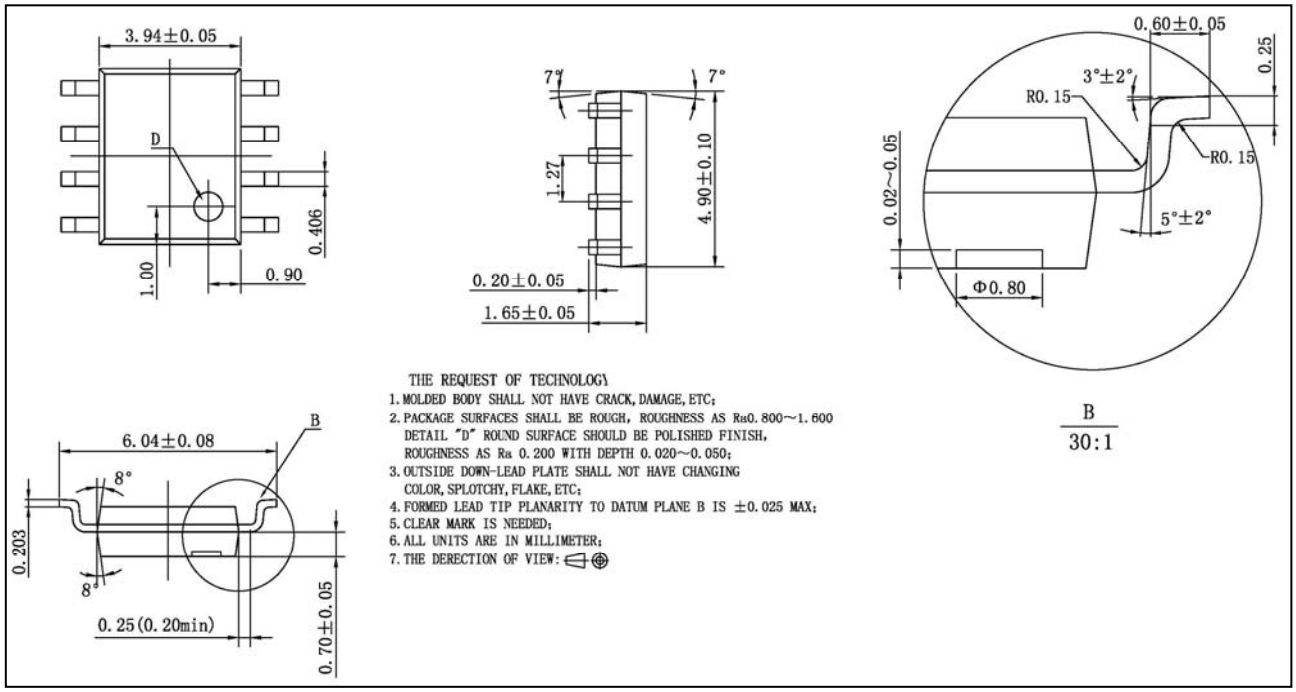


Figure 19 Classification Profile

PACKAGE INFORMATION

SOP-8



Note: All dimensions in millimeters unless otherwise stated.