

# AN8017SA

## 1.8-volt 2-channel step-up DC-DC converter control IC

### ■ Overview

The AN8017SA is a two-channel PWM DC-DC converter control IC that features low-voltage operation.

This IC can obtain the step-up voltage with a small number of external components.

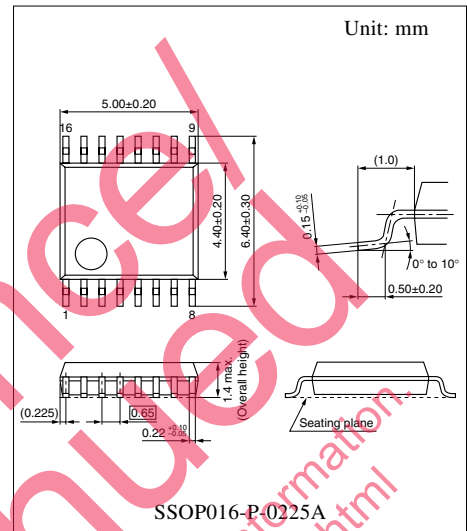
The minimum operating voltage is as low as 1.8 V so that it can operate with two dry batteries. In addition, since it uses the 16-pin surface mounting type package with 0.65 mm pitch, it is suitable for a miniaturized highly efficient portable power supply.

### ■ Features

- Wide operating supply voltage range (1.8 V to 14 V)
- Incorporating a high precision reference voltage circuit (allowance:  $\pm 2\%$ )
- Control in a wide output frequency range is possible (20 kHz to 1 MHz)
- Built-in wideband error amplifier (single gain bandwidth: 10 MHz typical)
- A built-in timer latch short-circuit protection circuit (charge current: 1.1  $\mu\text{A}$  typical)
- Incorporating an under-voltage lock-out circuit (U.V.L.O.) (circuit operation-starting voltage: 1.67 V typical)
- Dead-time is variable
- Flatness of switching current can be obtained by staggering the turn-on timing of each channel
- Built-in unlatch function
  - When DT1 pin is low level or DT2 pin is high level, independent turn-off is possible.
- Incorporating an on/off control function (active-high control input, standby mode current: 1  $\mu\text{A}$  maximum)
- Parallel operation is possible
- Totem pole output
  - Output source-current:  $-50$  mA maximum (Constant current output with a less supply voltage fluctuation is possible by connecting an external resistor to pin 6 and pin 11)
  - Output sink-current:  $+80$  mA maximum

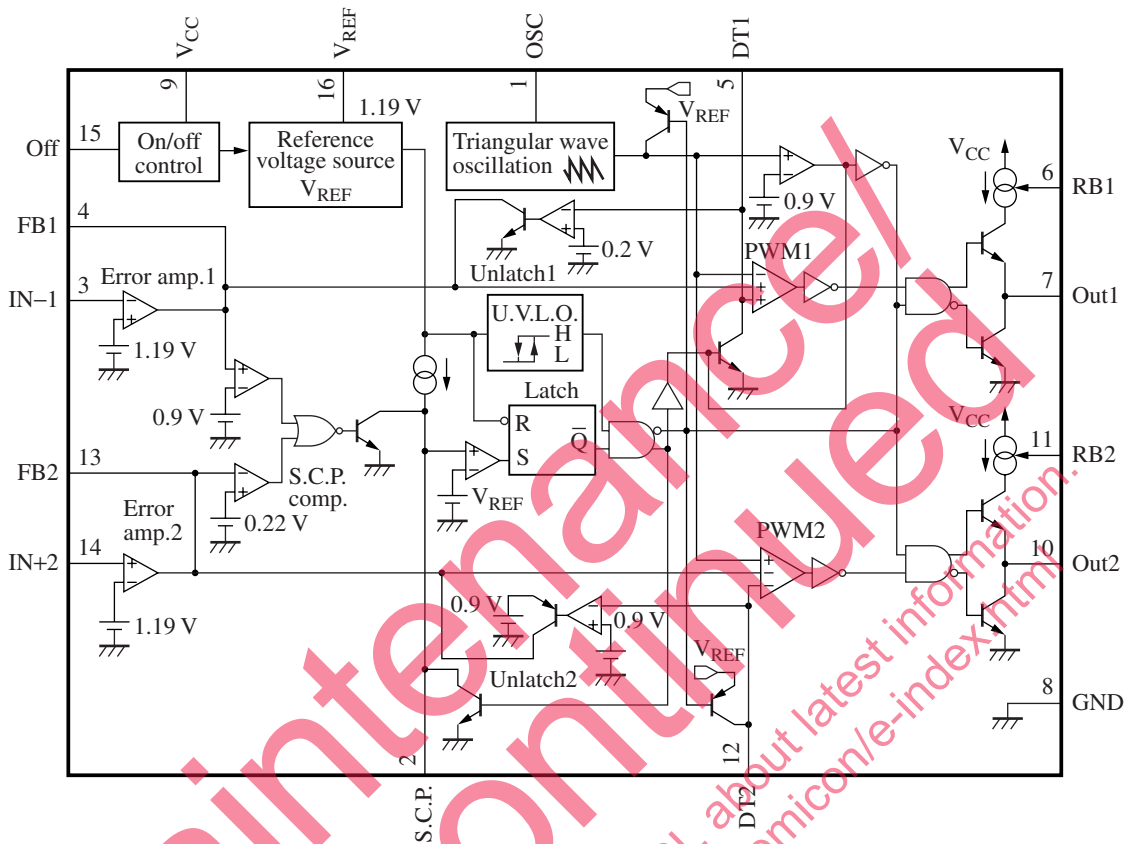
### ■ Applications

- LCD displays, digital still cameras, and PDAs



Note) The package of this product will be changed to lead-free type (SSOP016-P-0225E). See the package dimensions section later of this datasheet.

### ■ Block Diagram



### ■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	OSC	Pin for connecting a oscillation timing resistor and capacitor	8	GND	Grounding pin
2	S.C.P.	Pin for connecting the time constant setting capacitor for short-circuit protection	9	V <sub>CC</sub>	Power supply voltage application pin
3	IN-1	Inverting input pin to error amplifier 1 block	10	Out2	Out2 block push-pull type output pin
4	FB1	Output pin of error amplifier 1 block	11	RB2	Out2 block output source current setting resistor connection pin
5	DT1	PWM1 block dead-time setting pin	12	DT2	PWM2 block dead-time setting pin
6	RB1	Out1 block output source current setting resistor connection pin	13	FB2	Output pin of error amplifier 2 block
7	Out1	Out1 block push-pull type output pin	14	IN+2	Error amplifier 2 block noninverting input pin
			15	Off	On/off control pin
			16	V <sub>REF</sub>	Reference voltage output pin

### ■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	15	V
Off terminal allowable application voltage	$V_{OFF}$	15	V
IN-1 terminal allowable application voltage *2	$V_{IN-1}$	6	V
IN+2 terminal allowable application voltage *2	$V_{IN+2}$	6	V
Supply current	$I_{CC}$	—	mA
Output source current	$I_{SO(OUT)}$	-50	mA
Output sink current	$I_{SI(OUT)}$	+80	mA
Power dissipation *1	$P_D$	135	mW
Operating ambient temperature	$T_{opr}$	-30 to +85	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Note) 1. Do not apply external currents or voltages to any pins not specifically mentioned.

For the circuit currents, '+' denotes current flowing into the IC, and '-' denotes current flowing out of the IC.

2. Except for the power dissipation, operating ambient temperature and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

3. \*1:  $T_a = 85^\circ\text{C}$ . For the independent IC without a heat sink. Note that applications must observe the derating curve for the relationship between the IC power consumption and the ambient temperature.

\*2:  $V_{IN-1}, V_{IN+2} = V_{CC}$  when  $V_{CC} < 6\text{ V}$ .

### ■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	$V_{CC}$	1.8 to 14	V
Off control terminal application voltage	$V_{OFF}$	0 to 14	V
Output source current	$I_{SO(OUT)}$	-40 (minimum)	mA
Output sink current	$I_{SI(OUT)}$	70 (maximum)	mA
Timing resistance	$R_T$	1 to 51	k $\Omega$
Timing capacitance	$C_T$	100 to 10000	pF
Oscillation frequency	$f_{OUT}$	20 to 1000	kHz
Short-circuit protection time constant setting capacitance	$C_{SCP}$	1000 (minimum)	pF
Output current setting resistance	$R_B$	180 to 15000	$\Omega$

### ■ Electrical Characteristics at $V_{CC} = 2.4\text{ V}$ , $C_{REF} = 0.1\ \mu\text{F}$ , $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
Reference voltage	$V_{REF}$	$I_{REF} = -0.1\text{ mA}$	1.166	1.19	1.214	V
Input regulation with input fluctuation	Line	$V_{CC} = 1.8\text{ V to }14\text{ V}$	—	15	30	mV
Load regulation	Load	$I_{REF} = -0.1\text{ mA to }-1\text{ mA}$	-20	-5	—	mV
U.V.L.O. block						
Circuit operation start voltage	$V_{UON}$		1.59	1.67	1.75	V

**■ Electrical Characteristics at  $V_{CC} = 2.4\text{ V}$ ,  $C_{REF} = 0.1\ \mu\text{F}$ ,  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Error amplifier 1 block</b>						
Input threshold voltage 1	$V_{TH1}$		1.16	1.19	1.22	V
Input bias current 1	$I_{B1}$		—	0.2	0.8	$\mu\text{A}$
High-level output voltage 1	$V_{EH1}$		0.83	0.93	1.03	V
Low-level output voltage 1	$V_{EL1}$		—	—	0.2	V
Output source current 1	$I_{SO(FB)1}$		-61	-47	-33	$\mu\text{A}$
Output sink current 1	$I_{SI(FB)1}$		33	47	61	$\mu\text{A}$
<b>Error amplifier 2 block</b>						
Input threshold voltage 2	$V_{TH2}$		1.16	1.19	1.22	V
Input bias current 2	$I_{B2}$		—	0.2	0.8	$\mu\text{A}$
High-level output voltage 2	$V_{EH2}$		0.83	0.93	1.03	V
Low-level output voltage 2	$V_{EL2}$		—	—	0.2	V
Output source current 2	$I_{SO(FB)2}$		-61	-47	-33	$\mu\text{A}$
Output sink current 2	$I_{SI(FB)2}$		33	47	61	$\mu\text{A}$
<b>Oscillator block</b>						
Output off threshold voltage	$V_{TH(OSC)}$		0.8	0.9	1.0	V
<b>Output 1 block</b>						
Oscillation frequency 1	$f_{OUT1}$	$R_T = 12\ \text{k}\Omega$ , $C_T = 330\ \text{pF}$	185	205	225	kHz
Output duty ratio 1	$Du_1$		73	78	83	%
High-level output voltage 1	$V_{OH1}$	$I_O = -10\ \text{mA}$ , $R_B = 820\ \Omega$	1.4	—	—	V
Low-level output voltage 1	$V_{OL1}$	$I_O = 10\ \text{mA}$ , $R_B = 820\ \Omega$	—	—	0.2	V
Output source current 1	$I_{SO(OUT)1}$	$V_O = 0.7\ \text{V}$ , $R_B = 820\ \Omega$	-40	-30	-20	mA
Output sink current 1	$I_{SI(OUT)1}$	$V_O = 0.7\ \text{V}$ , $R_B = 820\ \Omega$	20	—	—	mA
Pull-down resistance 1	$R_{O1}$		20	30	40	k $\Omega$
<b>Output 2 block</b>						
Oscillation frequency 2	$f_{OUT2}$	$R_T = 12\ \text{k}\Omega$ , $C_T = 330\ \text{pF}$	185	205	225	kHz
Output duty ratio 2	$Du_2$		72	77	82	%
High-level output voltage 2	$V_{OH2}$	$I_O = -10\ \text{mA}$ , $R_B = 820\ \Omega$	1.4	—	—	V
Low-level output voltage 2	$V_{OL2}$	$I_O = 10\ \text{mA}$ , $R_B = 820\ \Omega$	—	—	0.2	V
Output source current 2	$I_{SO(OUT)2}$	$V_O = 0.7\ \text{V}$ , $R_B = 820\ \Omega$	-40	-30	-20	mA
Output sink current 2	$I_{SI(OUT)2}$	$V_O = 0.7\ \text{V}$ , $R_B = 820\ \Omega$	20	—	—	mA
Pull-down resistance 2	$R_{O2}$		20	30	40	k $\Omega$
<b>PWM1 block</b>						
Output full-off input threshold voltage 1	$V_{T0-1}$	Duty = 0%	—	0.28	0.30	V
Output full-on input threshold voltage 1	$V_{T100-1}$	Duty = 100%	0.65	0.72	—	V
Input current 1	$I_{DT1}$	$V_{DT1} = 0.5\ \text{V}$	-1.1	-0.5	—	$\mu\text{A}$

**■ Electrical Characteristics at  $V_{CC} = 2.4\text{ V}$ ,  $C_{REF} = 0.1\ \mu\text{F}$ ,  $T_a = 25\ ^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>PWM2 block</b>						
Output full-off input threshold voltage 2	$V_{T0-2}$	Duty = 0%	0.65	0.72	—	V
Output full-on input threshold voltage 2	$V_{T100-2}$	Duty = 100%	—	0.28	0.30	V
Input current 2	$I_{DT2}$	$V_{DT2} = 0.2\text{ V}$	-1.1	-0.5	—	$\mu\text{A}$
<b>Unlatch circuit 1 block</b>						
Input threshold voltage 1	$V_{THUL1}$		0.15	0.20	0.25	V
<b>Unlatch circuit 2 block</b>						
Input threshold voltage 2	$V_{THUL2}$		0.8	0.9	1.0	V
<b>Short-circuit protection circuit block</b>						
Input standby voltage	$V_{STBY}$		—	60	120	mV
Input threshold voltage 1	$V_{THPC1}$		0.8	0.9	1.0	V
Input threshold voltage 2	$V_{THPC2}$		0.17	0.22	0.27	V
Input latch voltage	$V_{IN}$		—	60	120	mV
Charge current	$I_{CHG}$	$V_{SCP} = 0\text{ V}$	-1.43	-1.1	-0.77	$\mu\text{A}$
<b>On/off control block</b>						
Input threshold voltage	$V_{ON(TH)}$		0.8	1.0	1.3	V
<b>Whole device</b>						
Output off consumption current	$I_{CC(OFF)}$	$R_B = 820\ \Omega$ , duty = 0%	—	7.0	9.8	mA
Latch mode consumption current	$I_{CC(LA)}$	$R_B = 820\ \Omega$	—	5.6	7.8	mA
Standby current	$I_{CC(SB)}$		—	—	1	$\mu\text{A}$

**• Design reference data**

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Reference voltage block</b>						
$V_{REF}$ temperature characteristics	$V_{REFdT}$	$T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$	-1	—	+1	%
Over-current protection drive current	$I_{OC}$		—	-11	—	mA
<b>U.V.L.O. block</b>						
Reset voltage	$V_R$		—	0.8	—	V
<b>Error amplifier 1/2 blocks</b>						
$V_{TH}$ temperature characteristics	$V_{THdT}$	$T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$	-0.3	—	+0.3	mV/ $^\circ\text{C}$
Open-loop gain	$A_V$		—	57	—	dB
Single gain bandwidth	$f_{BW}$		—	10	—	MHz
<b>Output 1/2 blocks</b>						
RB terminal voltage	$V_B$		—	0.36	—	V
Frequency supply voltage characteristics	$f_{dV}$		-1	—	+1	%
Frequency temperature characteristics	$f_{dT}$		-3	—	+3	%

### ■ Electrical Characteristics at $V_{CC} = 2.4\text{ V}$ , $C_{REF} = 0.1\ \mu\text{F}$ , $T_a = 25^\circ\text{C}$ (continued)

#### • Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Short-circuit protection block						
Comparator threshold voltage	$V_{THL}$		—	1.19	—	V
On/off control block						
Off terminal current	$I_{OFF}$		—	23	—	$\mu\text{A}$

### ■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		<p>OSC:</p> <p>The terminal used for connecting a timing capacitor/resistor to set oscillation frequency. Use a capacitance value within the range of 100 pF to 10000 pF and a resistance value within the range of 1 k<math>\Omega</math> to 51 k<math>\Omega</math>. Use an oscillation frequency in the range of 20 kHz to 1 MHz. In a parallel synchronous operation, the channel 2 output stops when this pin becomes 0.9 V or more. (Refer to the "Application Notes, [7]" section.)</p>	O
2		<p>S.C.P.:</p> <p>The terminal for connecting a capacitor to set the time constant of the timer latch short-circuit protection circuit. Use a capacitance value in the range of 1000 pF or more. The charge current <math>I_{CHG}</math> is 1.1 <math>\mu\text{A}</math> typical.</p>	O
3		<p>IN-1:</p> <p>The inverting input pin for error amplifier 1 block.</p>	I

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
4		<p><b>FB1:</b> The output pin for error amplifier 1 block. The source current is <math>-47 \mu\text{A}</math> and the sink current is <math>47 \mu\text{A}</math>. Correct the frequency characteristics of the gain and the phase by connecting a resistor and a capacitor between this terminal and GND.</p>	O
5		<p><b>DT1:</b> The pin for setting channel 1 output maximum duty ratio. If this terminal is set at a voltage of <math>0.20 \text{ V}</math> or less, FB1 terminal becomes low-level voltage and the protective function for channel 1 output short-circuit will stop (Unlatch function).</p>	I
6		<p><b>RB1:</b> The pin for connecting a resistor for setting channel 1 output current. Use a resistance value in the range of <math>180 \Omega</math> to <math>15 \text{ k}\Omega</math>. The terminal voltage is <math>0.36 \text{ V}</math> (at <math>R_{B1} = 820 \Omega</math>). Please refer to the "Usage Notes [2]", if you intend to directly drive a n-channel MOSFET from this pin.</p>	I
7		<p><b>Out1:</b> The pin is push-pull type output terminal. The absolute maximum ratings of output current are <math>-50 \text{ mA}</math> for the source current and <math>+80 \text{ mA}</math> for the sink current. A constant current output with less fluctuation with power supply voltage and dispersion can be obtained by the resistor externally attached to RB1 pin.</p> $I_{SO(OUT)1} = 68 \times \frac{V_{RB1}}{R_{B1}} \text{ [A]}$	O
8		<p><b>GND:</b> Grounding terminal</p>	—
9		<p><b>Vcc:</b> The supply voltage application terminal Use the operating supply voltage in the range of <math>1.8 \text{ V}</math> to <math>14 \text{ V}</math>.</p>	—

### ■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
10		<p><b>Out2:</b> The pin is push-pull type output terminal. The absolute maximum ratings of output current are -50 mA for the source current and +80 mA for the sink current. A constant current output with less fluctuation with power supply voltage and dispersion can be obtained by the resistor externally attached to RB2 pin.</p> $I_{SO(OUT)2} = 68 \times \frac{V_{RB2}}{R_{B2}} \text{ [A]}$	O
11		<p><b>RB2:</b> The pin for connecting a resistor for setting channel 2 output current. Use a resistance value in the range of 180 Ω to 15 kΩ. The terminal voltage is 0.36 V (at <math>R_{B2} = 820 \Omega</math>). Please refer to the "Usage Notes [2]" if you intend to directly drive a n-channel MOSFET from this pin.</p>	I
12		<p><b>DT2:</b> The pin for setting channel 2 output maximum duty ratio. If this terminal is set at a voltage of 0.9 V or more, FB2 terminal becomes high-level voltage and the protective function for channel 2 output short-circuit will stop (Unlatch function).</p>	I
13		<p><b>FB2:</b> The output pin for error amplifier. The source current is -47 μA and the sink current is 47 μA. Correct the frequency characteristics of the gain and the phase by connecting a resistor and a capacitor between this terminal and GND.</p>	O
14		<p><b>IN+2:</b> The noninverting input pin for error amplifier 2 block.</p>	I



■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
15		<p>Off:</p> <p>The terminal for on/off control.</p> <p>High-level input: Normal operation (<math>V_{OFF} &gt; 1.3 \text{ V}</math>)</p> <p>Low-level input: Standby state (<math>V_{OFF} &lt; 0.8 \text{ V}</math>)</p> <p>The total current consumption in the standby state can be suppressed to a value of <math>1 \mu\text{A}</math> or less.</p>	I
16		<p><math>V_{REF}</math>:</p> <p>The output terminal for the internal reference voltage.</p> <p>The reference voltage is <math>1.19 \text{ V}</math> (allowance: <math>\pm 2\%</math>) at <math>V_{CC} = 2.4 \text{ V}</math> and <math>I_{REF} = -0.1 \text{ mA}</math>.</p> <p>Connect a capacitor of <math>0.01 \mu\text{F}</math> or more between <math>V_{REF}</math> and GND for phase compensation.</p>	O

■ Usage Notes

[1] The loss, P of this IC increases in proportion to the supply voltage. Use the IC so as not to exceed the allowable power dissipation of package,  $P_D$ .

Reference formula:

$$P = (V_{CC} - V_{BEQ1}) \times I_{SO(OUT)1} \times Du_1 + (V_{CC} - V_{BEQ2}) \times I_{SO(OUT)2} \times Du_2 + V_{CC} \times I_{CC} < P_D$$

$V_{BEQ1}$  : Base-emitter voltage of npn transistor Q1

$I_{SO(OUT)1}$  : Out1 terminal output source current  
(set by  $R_{B1}$ ,  $I_{SO(OUT)1} = 40 \text{ mA}$  maximum at  $R_{B1} = 820 \Omega$ )

$Du_1$  : Output1 duty ratio

$V_{BEQ2}$  : Base-emitter voltage of npn transistor Q2

$I_{SO(OUT)2}$  : Out2 terminal output source current  
(set by  $R_{B2}$ ,  $I_{SO(OUT)2} = 40 \text{ mA}$  maximum at  $R_{B2} = 820 \Omega$ )

$Du_2$  : Output2 duty ratio

$I_{CC}$  :  $V_{CC}$  terminal current ( $8.0 \text{ mA}$  maximum where  $V_{CC} = 2.4 \text{ V}$ )

[2] Since the output of the AN8017SA is assuming the bipolar transistor driving, it is necessary to pay attention to the following points when an n-channel MOSFET is driven directly.

1. Select an n-channel MOSFET having a low input capacitance

The AN8017SA is of the constant current ( $50 \text{ mA}$  maximum) output source current type circuit assuming the bipolar transistor driving. Also, its sink current capability is around  $80 \text{ mA}$  maximum. For those reason, it is necessary to pay attention to the increase of loss due to the extension of the output rise time and the output fall time.

If any problem arises, there is a method to solve it by amplifying with inverters as shown in figure 1.

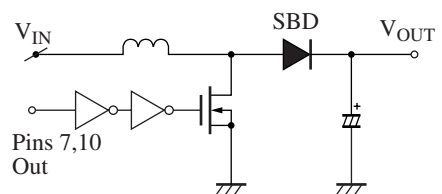


Figure 1. Output bootstrap circuit example

## ■ Usage Notes (continued)

2. Select an n-channel MOSFET having a low gate threshold value

The high-level output voltage of out pin of the AN8017SA is  $V_{CC} - 1.0$  V minimum, so that it is necessary to select a low  $V_T$  MOSFET having a sufficiently low on-state resistance in accordance with the using operating supply voltage.

If a larger  $V_{GS}$  is desired, there is a method to apply the double-voltage of the input to the IC's  $V_{CC}$  pin by using the transformer as shown in figure 2.

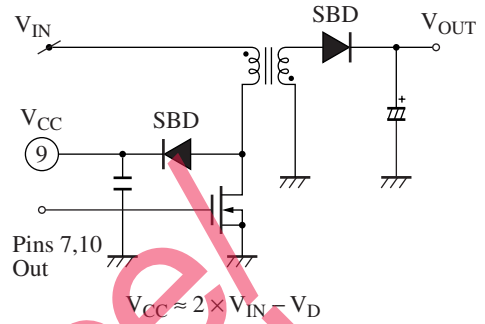
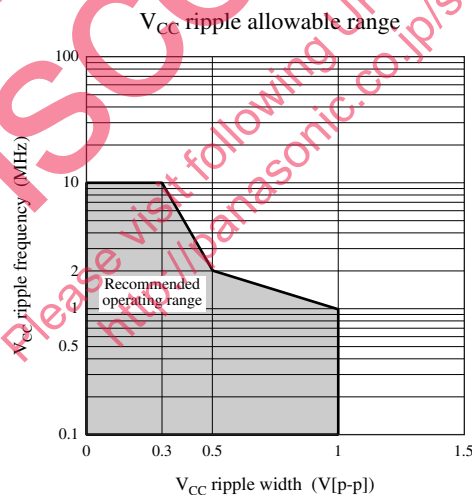


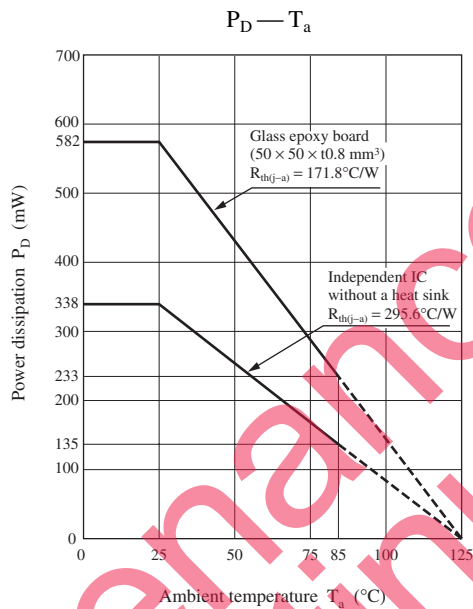
Figure 2. Gate drive voltage increasing method

- [3] In order to realize a low noise and high efficiency, care should be taken in the following points in designing the board layout.
1. The wiring for ground line should be taken as wide as possible and grounded separately from the power system.
  2. The input filter capacitor should be arranged in a place as close to  $V_{CC}$  and GND pin as possible so as not to allow switching noise to enter into the IC inside.
  3. The wiring between the Out terminal and switching device (transistor or MOSFET) should be as short as possible to obtain a clean switching waveform.
  4. In wiring the detection resistor of the output voltage, the wiring for the low impedance side should be longer.
- [4] There is a case in which this IC does not start charging to the S.C.P. capacitor when the output is short-circuited due to the malfunction of U.V.L.O. circuit biased by  $V_{CC}$  that has ripples generated by turning on and off of the switching transistor. The allowable range of the  $V_{CC}$  ripple is as shown in the following figure. Reduce the  $V_{CC}$  ripple by inserting a capacitor near the  $V_{CC}$  terminal and GND terminal of this IC so that the  $V_{CC}$  ripple is in this allowable range. However, this allowable range is design reference value and not the guaranteed value.



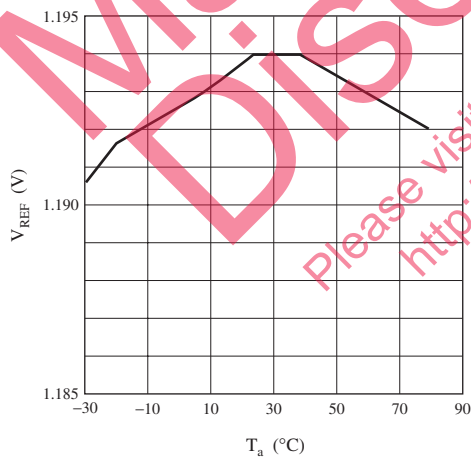
Application Notes

[1]  $P_D - T_a$  curves of SSOP016-P-0225A

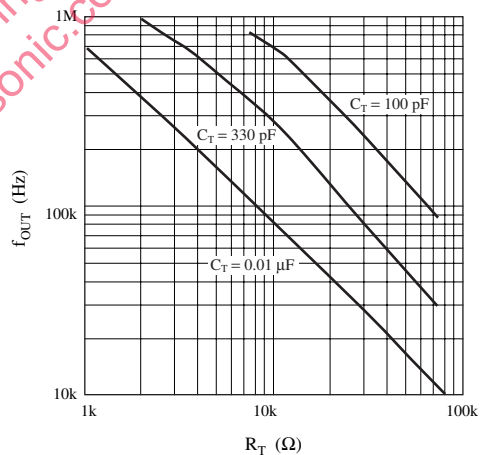


[2] Main characteristics

$V_{REF}$  temperature characteristics



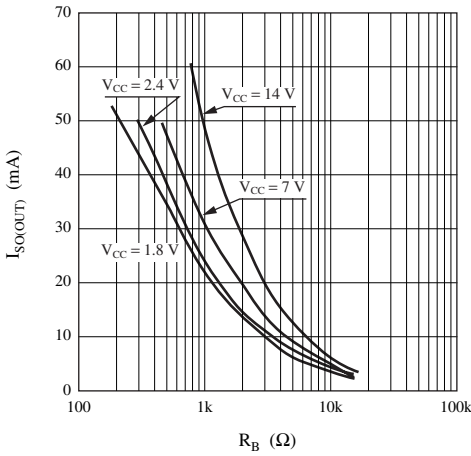
Frequency characteristics



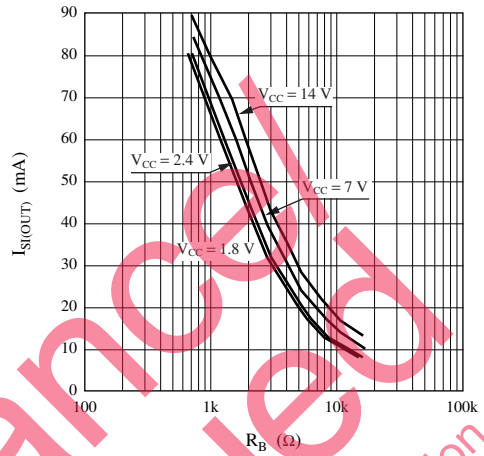
■ Application Notes (continued)

[2] Main characteristics (continued)

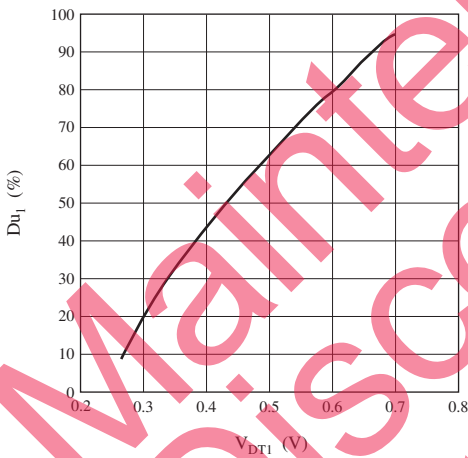
$I_{SO(OUT)} - R_B$



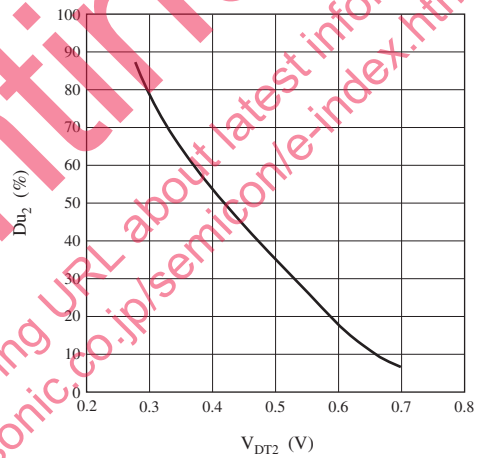
$I_{SI(OUT)} - R_B$



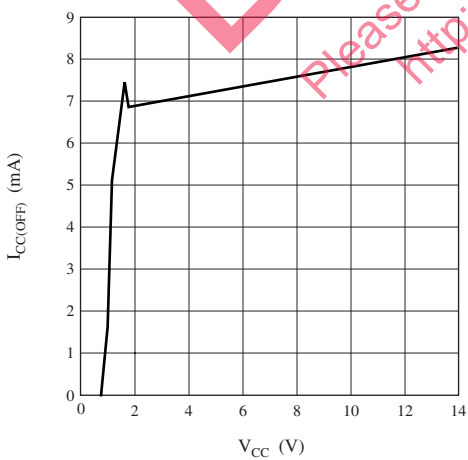
$Du_1 - V_{DT1}$



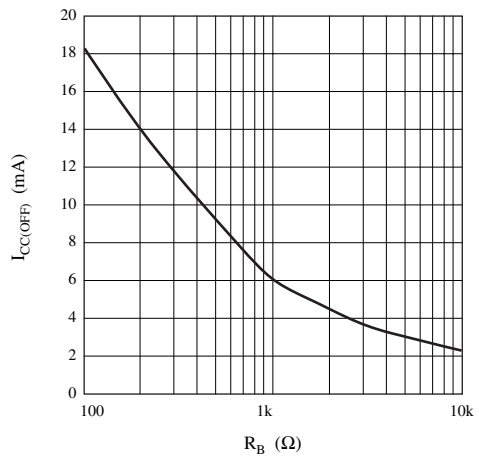
$Du_2 - V_{DT2}$



$I_{CC(OFF)} - V_{CC}$

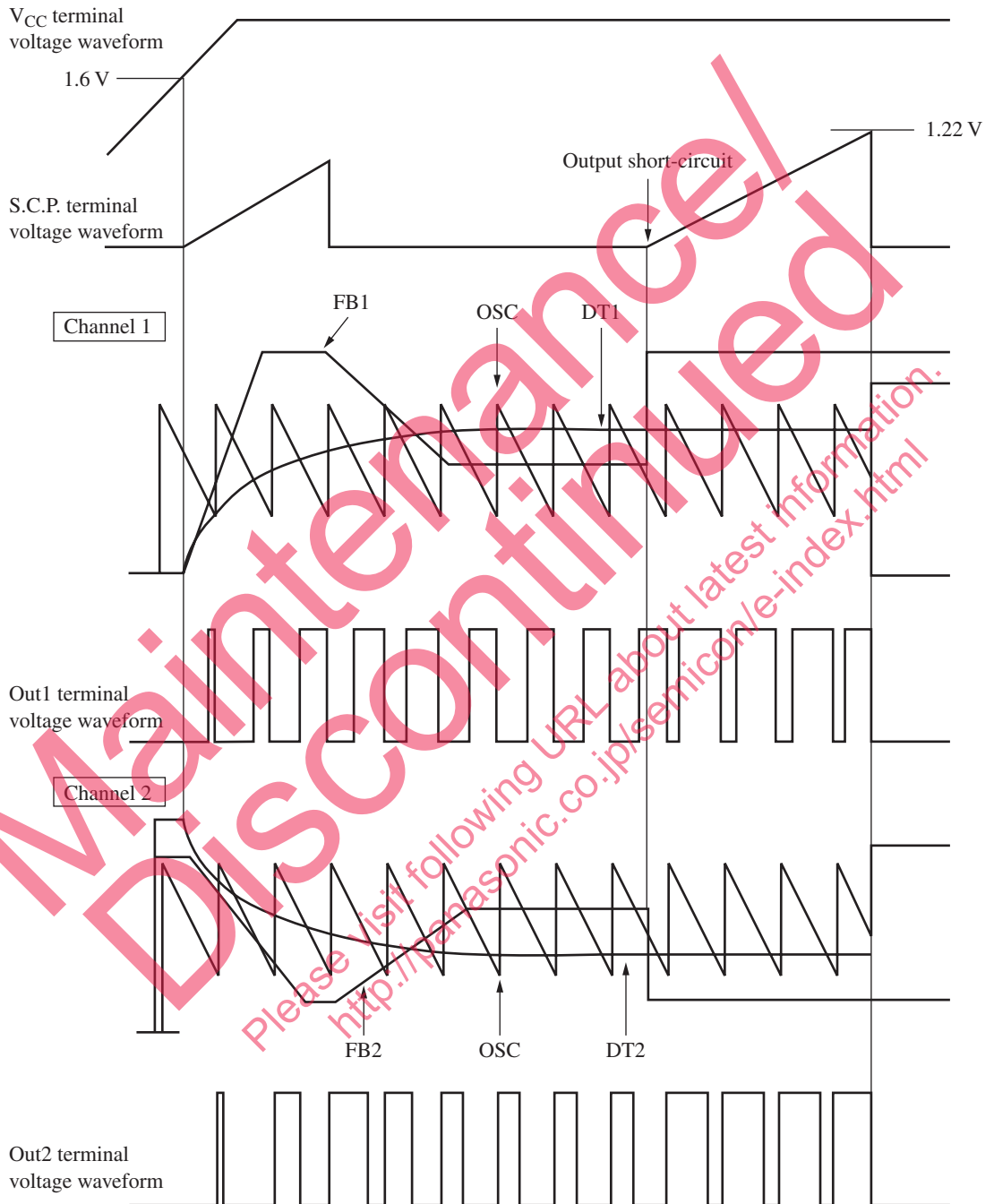


$I_{CC(OFF)} - R_B$



■ Application Notes (continued)

[3] Timing chart



## ■ Application Notes (continued)

### [4] Function descriptions

#### 1. Reference voltage block

This block is composed of the band gap circuit, and outputs the temperature compensated 1.19 V reference voltage. The reference voltage is stabilized when the supply voltage is 1.8 V or more. The reference voltage is also used as the reference voltage for the error amplifier 1 block and the error amplifier 2 block.

#### 2. Triangular wave oscillation block

The sawtooth-waveform-like triangular wave having a peak of approximately 0.7 V and a trough of approximately 0.2 V can be generated by connecting the timing capacitor and resistor to the OSC terminal (pin 1). The oscillation frequency can be freely set by the value of  $C_T$  and  $R_T$  to be connected externally. The usable oscillation frequency is from 20 kHz to the maximum 1 MHz. The triangular wave is connected with the inverting input of PWM comparator for channel 1 side and the noninverting input of PWM comparator for channel 2 side within the IC. And refer to the experimentally determined graph of the frequency characteristics provided in the main characteristics section.

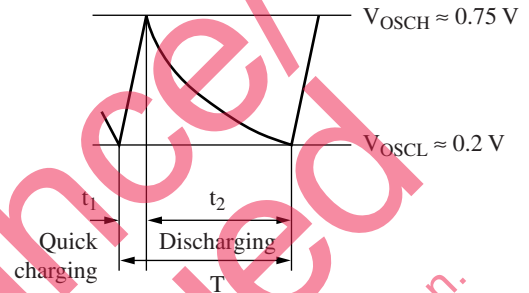


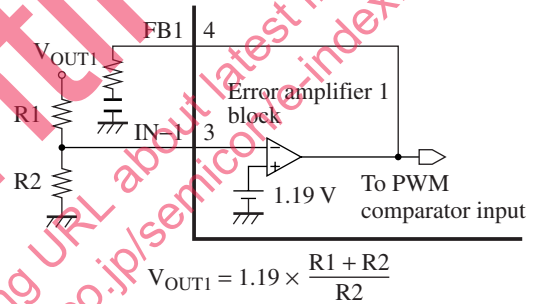
Figure 1. Triangular wave oscillation waveform

#### 3. Error amplifier 1 block

The output voltage of DC-DC converter is detected by the npn-transistor-input type error amplifier and the amplified signal is input to the PWM comparator. The internal reference voltage 1.19 V is given to the noninverting input.

Also, it is possible to perform the gain setting and the phase compensation arbitrarily by connecting a resistor and a capacitor from the FB1 terminal (pin 4) to GND in series.

The output voltage  $V_{OUT1}$  can be set by making connection as shown in figure 2.



$$V_{OUT1} = 1.19 \times \frac{R1 + R2}{R2}$$

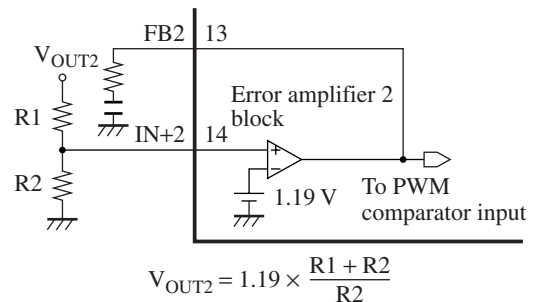
Figure 2. Connection method of error amplifier 1 block (Step-up output)

#### 4. Error amplifier 2 block

The output voltage of DC-DC converter is detected by the npn-transistor-input type error amplifier and the amplified signal is input to the PWM comparator. The internal reference voltage 1.19 V is given to the noninverting input.

Also, it is possible to perform the gain setting and the phase compensation arbitrarily by connecting a resistor and a capacitor from the FB2 terminal (pin 13) to GND in series.

The output voltage  $V_{OUT2}$  can be set by making connection as shown in figure 3.



$$V_{OUT2} = 1.19 \times \frac{R1 + R2}{R2}$$

Figure 3. Connection method of error amplifier 2 block (Step-up output)

## ■ Application Notes (continued)

### [4] Function descriptions (continued)

#### 5. Timer latch short-circuit protection circuit

This circuit protects the external main switching devices, flywheel diodes, and choke coils, etc. from destruction or deterioration if overload or short-circuit condition of power supply output lasts for a certain time.

The timer latch short-circuit protection circuit detects the output level of the error amplifier. When the output voltage of DC-DC converter drops and the output level of error amplifier 1 block exceeds 0.9 V or the output level of error amplifier 2 block exceeds 0.22 V, the low-level output is given and the timer circuit is actuated to start the charge of the external protection-enable capacitor.

If the output of the error amplifier does not return to a normal voltage range by the time when the voltage of this capacitor reaches 1.22 V, it sets the latch circuit, and cuts off the output drive transistor, and sets the dead-time to 100%.

#### 6. Low input voltage malfunction prevention circuit (U.V.L.O.)

This circuit protects the system from destruction or deterioration due to control malfunction when the supply voltage is low in the transient state of power on/off.

The low input voltage malfunction prevention circuit detects the internal reference voltage which changes according to the supply voltage level. Until the supply voltage reaches 1.67 V during its rise time, it cuts off the output drive transistor, and sets the dead-time to 100%. At the same time, it holds the S.C.P. terminal (pin 2) and DT1 terminal (pin 5) to low-level and the OSC terminal (pin 1) and DT2 terminal (pin 12) to high-level.

#### 7. PWM comparator block

The PWM comparator controls the on-period of the output pulse according to the input voltage. The PWM1 and PWM2 block are reverse logic relation.

The PWM1 block turns on the output transistor during the period when the triangular wave of OSC terminal (pin 1) is lower than any lower one of the FB1 (pin 4) terminal voltage and the DT1 (pin 5) terminal voltage.

The PWM2 block turns on the output transistor during the period when the triangular wave of OSC terminal (pin 1) is higher than any higher one of the FB2 (pin 13) terminal voltage and the DT2 (pin 12) terminal voltage.

The maximum duty ratio is variable from the outside.

Also, the soft start which gradually extends on-period of the output pulse is activated by connecting a capacitor in parallel with the resistor-dividing for the maximum duty ratio setting.

#### 8. Unlatch block

The unlatch circuit 1 block fixes the FB1 terminal (pin 4) at low-level at the DT1 terminal (pin 5) is 0.20 V or less. The unlatch circuit 2 block fixes the FB2 terminal (pin 13) at high-level at the DT2 terminal (pin 12) is 0.9 V or less. Consequently, by controlling the DT terminal voltage, it is possible to operate only one channel or to start and stop each channel in any required sequence.

#### 9. Output 1 block

This block uses a totem pole type output circuit. By connecting the current setting resistor to the RB1 terminal, it is possible to arbitrarily set a constant-current source-output having a small fluctuation with the supply voltage.

The available constant-current source-output is up to 50 mA. The breakdown voltage of output terminal is 15 V.

#### 10. Output 2 block

This block uses a totem pole type output circuit. By connecting the current setting resistor to the RB2 terminal, it is possible to arbitrarily set a constant-current source-output having a small fluctuation with the supply voltage.

The available constant-current source-output is up to 50 mA. The breakdown voltage of output terminal is 15 V.

## ■ Application Notes (continued)

### [5] About logic of PWM block

The logic for channel 1 and channel 2 of this IC is reversed. Thereby an input current flatness is realized. At the same time, noise can be suppressed to a lower level by staggering the turn on timing.

The PWM1 block turns on the output transistor during the period when the triangular wave of the OSC terminal (pin 1) is lower than both of the FB1 (pin 4) terminal voltage and the DT1 (pin 5) terminal voltage.

The PWM2 block turns on the output transistor during the period when the triangular wave of the OSC terminal (pin 1) is higher than both of the FB2 (pin 13) terminal voltage and the DT2 (pin 12) terminal voltage.

(Refer to figure 4.)

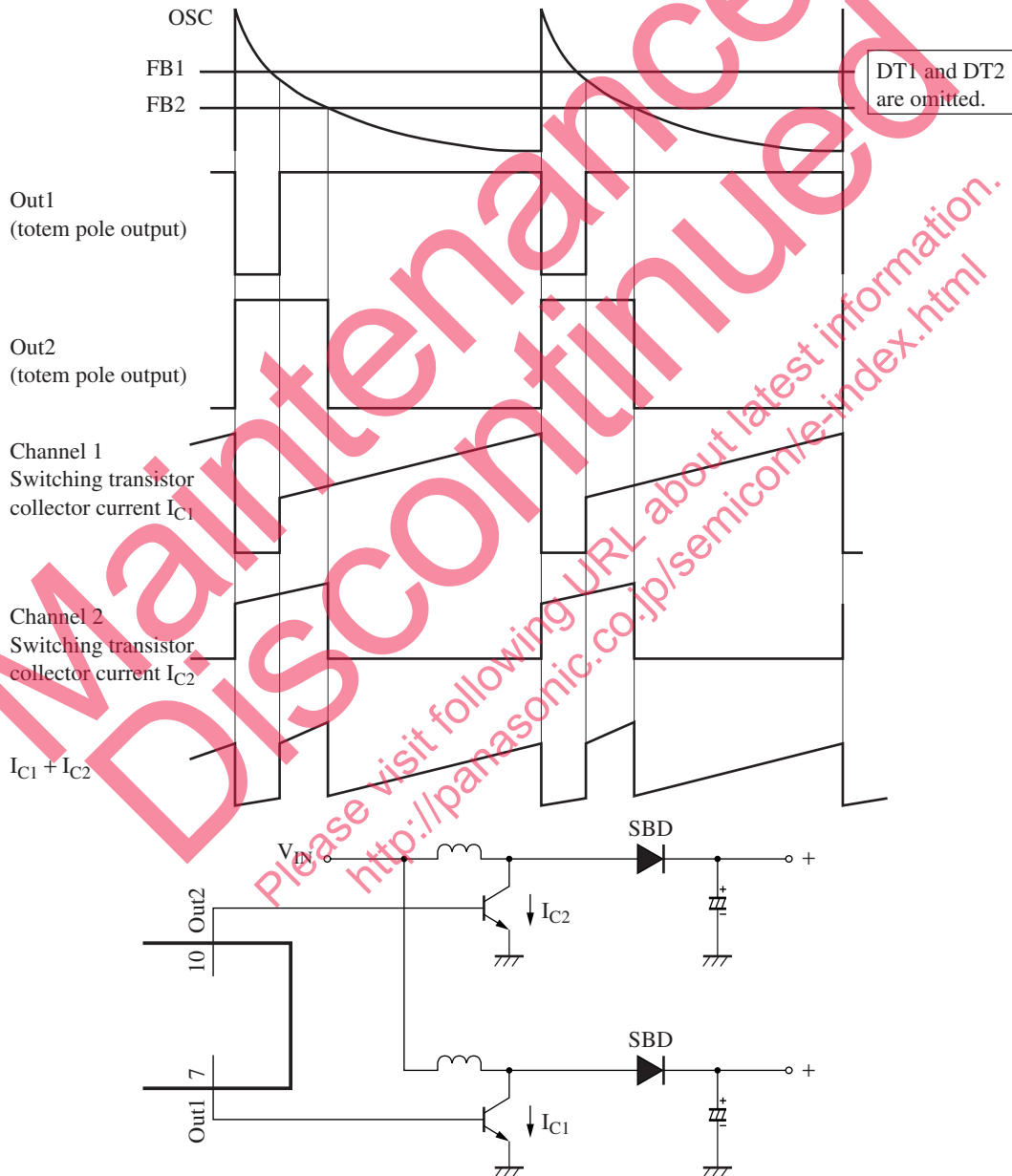


Figure 4. PWM logic explanation chart



■ Application Notes (continued)

[6] Time constant setting method for timer latch short-circuit protection circuit

The constructional block diagram of protection latch circuit is shown in figure 6. The comparator for short-circuit protection compares the error amplifier 1 output FB1 with the reference voltage of 0.9 V for channel 1 side, and the error amplifier 2 output FB2 with the reference voltage of 0.18 V for channel 2 side at all the time.

When the load conditions of DC-DC converter output is stabilized, there is no fluctuation of error amplifier output and the short-circuit protection comparator also keeps the balance. At this moment, the output transistor Q1 is in the conductive state and the S.C.P. terminal is held to approximately 60 mV.

When the load conditions for channel 1 side suddenly change and high-level signal (0.9 V or more) is input from the error amplifier 1 block to the short-circuit protection comparator, the short-circuit protection comparator outputs the low-level signal to cut off the output transistor Q1. Also, when the load conditions for channel 2 side suddenly change and low-level signal (0.22 V or less) is inputted from the error amplifier 2 block to the short-circuit protection comparator, the short-circuit protection comparator outputs the low-level signal to cut off the output transistor Q1. The capacitor C<sub>SCP</sub> connected to the S.C.P. terminal starts charging. When the external capacitor C<sub>SCP</sub> has been charged to approximately 1.19 V with the constant current of approximately 1.1 μA, the latch circuit is set, the output terminal is fixed to low-level, and the dead-time is set to 100%. Once the latch circuit is set, the S.C.P. terminal is discharged to approximately 40 mV. However, the latch circuit is not reset unless the power for the latch circuit is turned off or restarted by the on/off control.

$$1.19 \text{ V} = I_{\text{CHG}} \times \frac{t_{\text{PE}}}{C_{\text{SCP}}}$$

$$\therefore t_{\text{PE}} [\text{s}] = 1.08 \times C_{\text{SCP}}$$

When the power supply is turned on, the output is considered to be short-circuited state so that the S.C.P. terminal voltage starts charging. It is necessary to set the external capacitor so as to start up the DC-DC converter output voltage before setting the latch circuit in the later stage. Especially, pay attention to the delay of the start-up time when applying the soft-start.

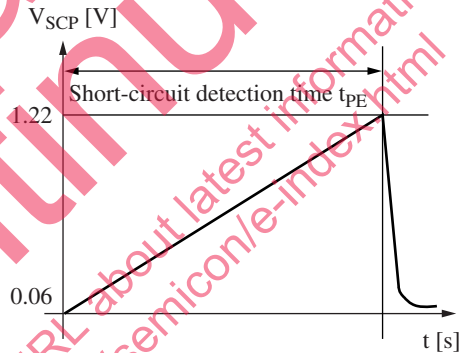


Figure 5. S.C.P. terminal charging waveform

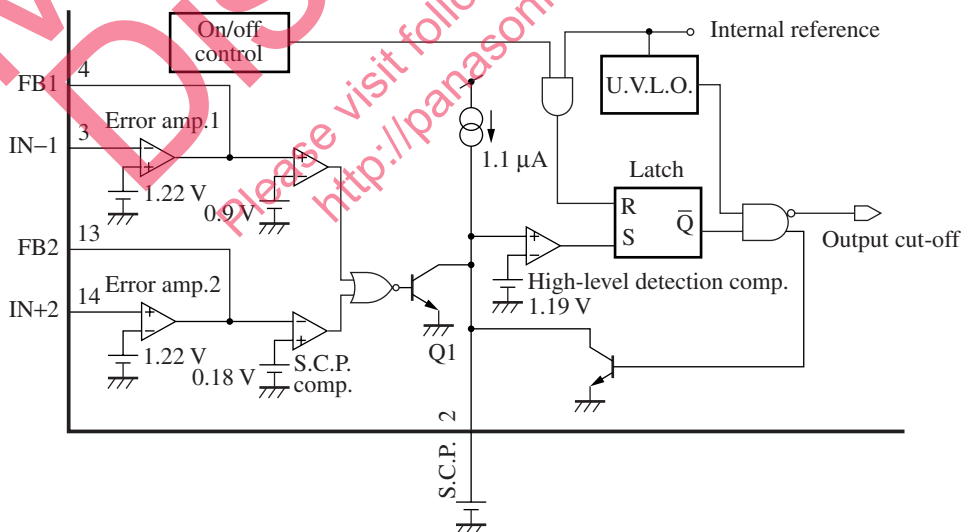


Figure 6. Short-circuit protection circuit



■ Application Notes (continued)

[7] Parallel synchronous operation of multiple ICs (continued)

2. About the operation of short-circuit protection at parallel synchronous operation

In the case of the operation in parallel, if the single output (or multiple outputs) of them is short-circuited and the timer latch is applied to the IC which has that output, the output of other ICs will be also shut down.

In figure 8, if the timer latch is applied to IC-2, Q1 turns on and the OSC terminal (pin 1) is raised to approximately 1.1 V. Then channel 1 of IC-1 logically turns off, and then for channel 2, the output of comparator whose reference voltage is 0.9 V becomes high-voltage and Out2 is forced to go off. The same goes with the case when the timer latch is applied to IC-1.

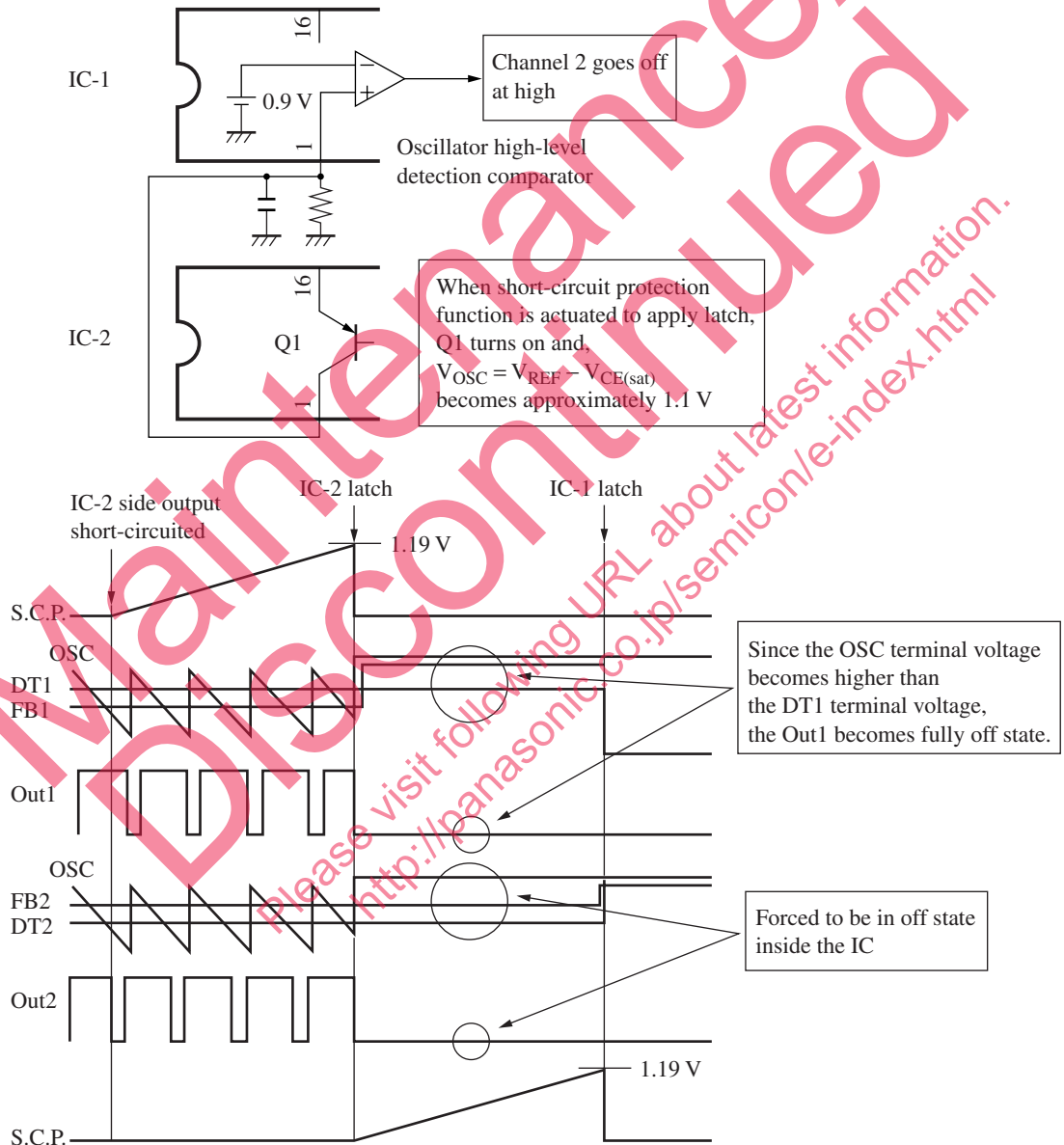


Figure 8. Operation of short-circuit protection at parallel synchronous operation

■ Application Notes (continued)

[8] Setting of Off-terminal connection resistor

The start circuit starts its operation when Q1 is turned on. In an organization in which Q1 turns off/on when Q2 turns on/off in figure 9, the input voltage  $V_{IN}$  at which the start circuit operates is obtained by the equation:

$$V_{IN} = V_{BEQ1} \times (R_{OFF} + R1 + R2) / R2$$

Therefore,  $R_{OFF}$  can be set by:

$$R_{OFF} = R2 \cdot V_{IN} / V_{BEQ1} - R1 - R2$$

Also, in case of limiting the Off terminal current by  $R_{OFF}$ , set it by the above equation. However, take the values as:

$$V_{BEQ1} = 0.7 \text{ V (T = 25}^\circ\text{C)}$$

$$V_{BEQ1} \text{ fluctuation with temperature: } -2 \text{ mV/}^\circ\text{C}$$

$$\text{Temperature coefficient of R1 and R2: } +6000 \text{ PPM/}^\circ\text{C}$$

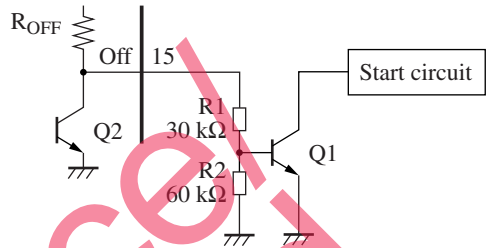


Figure 9. Off terminal peripheral circuit

[9] Sequential operation

It is possible to turn on/off the output of DC-DC converter individually by turning on/off Q1 and Q2 as shown in figure 10. However, pay particular attention to the current flowing into the  $V_{REF}$  terminal when Q2 is turned off since sink capability of  $V_{REF}$  terminal is approximately 100  $\mu$ A.

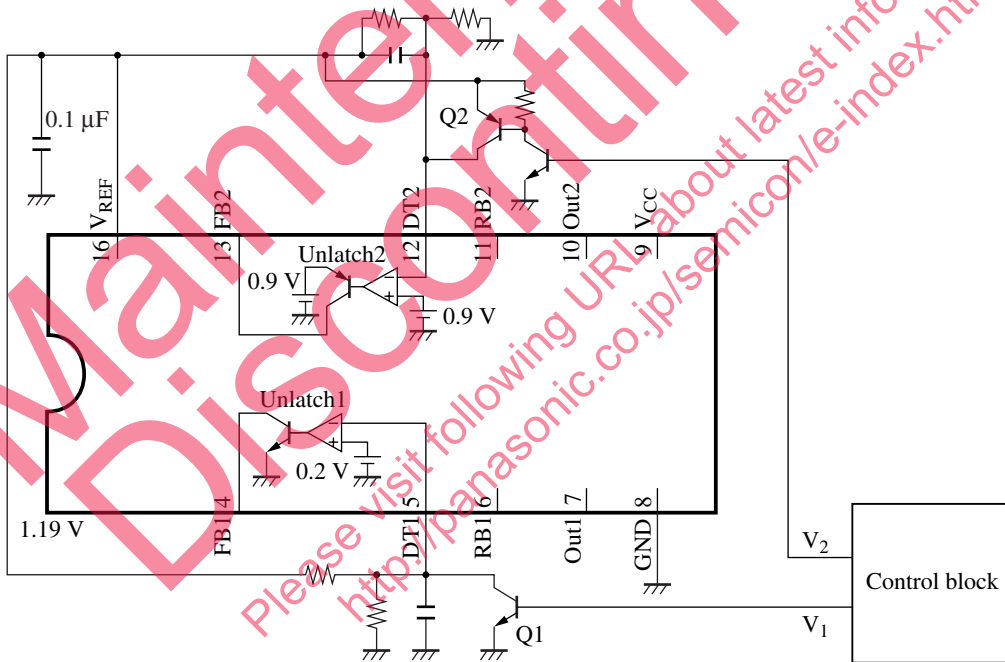
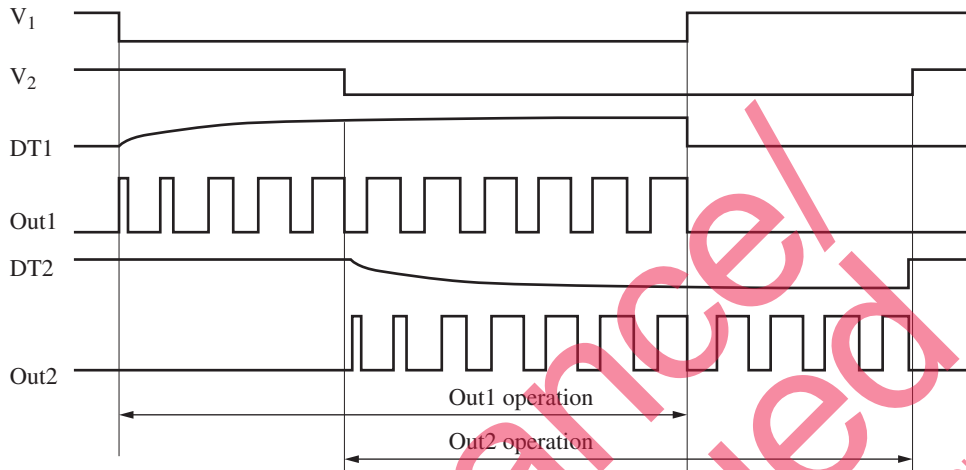


Figure 10

■ Application Notes (continued)

[9] Sequence operation (continued)



Out1: Off at DT1 < 0.2 V      Out2: Off at DT2 > 0.9 V

Operation when each channel is turned on/off independently

[10] Error amplifier phase-compensation setting method

The equivalent circuit of error amplifier is shown in figure 11.

The transfer function is:

$$H = \frac{1 / \{S (C_{E1} + C_{O1})\}}{R_{E1} + 1 / \{S (C_{E1} + C_{O1})\}} = \frac{1}{SC_{O1} \cdot R_{E1} + 1} \quad (\text{from } C_{E1} \ll C_{O1})$$

The cut-off frequency is variable by changing the externally attached phase compensation capacitor  $C_{O1}$ .

Adjust by inserting a resistor  $R_{O1}$  between the FB1 terminal and  $C_{O1}$  in series as shown in figure 12 when it is required to have a gain on the high frequency side or desired to lead a phase.

The transfer function is:

$$H = \frac{SC_{O1} \cdot R_{O1} + 1}{SC_{O1} (R_{O1} + R_{E1}) + 1} \quad (\text{from } C_{E1} \ll C_{O1})$$

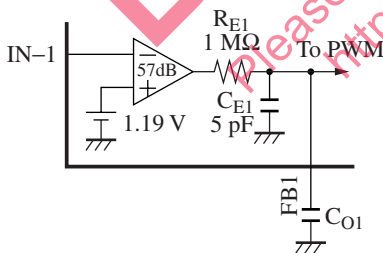


Figure 11. Error amplifier equivalent circuit

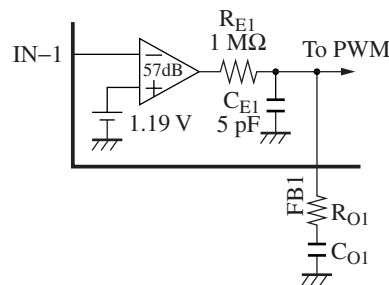
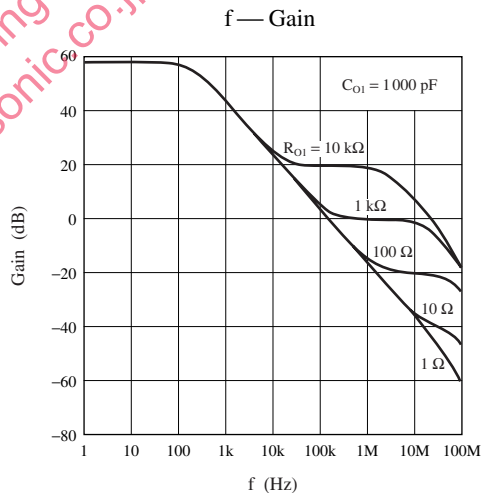
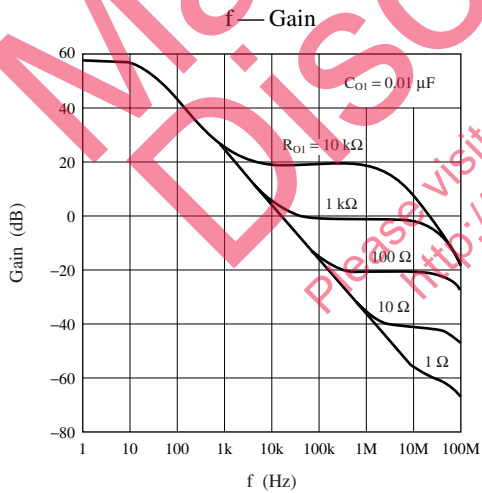
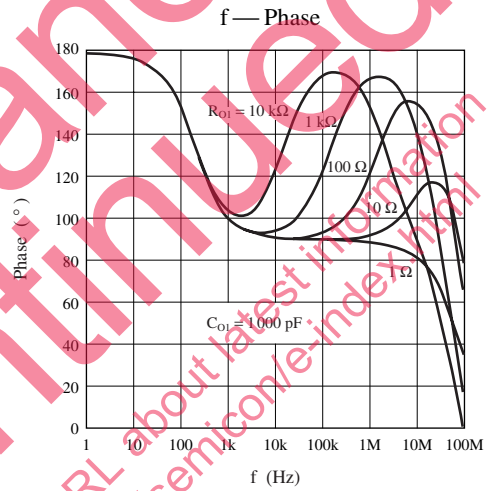
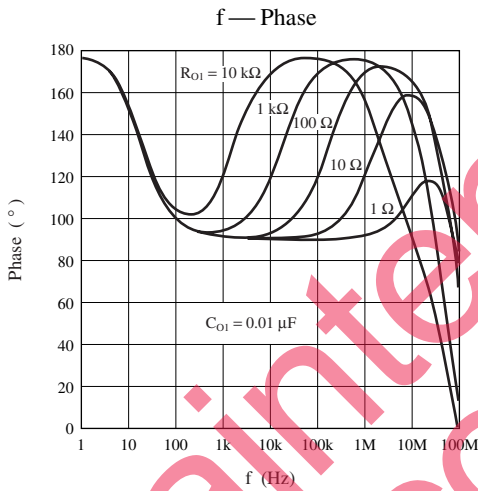
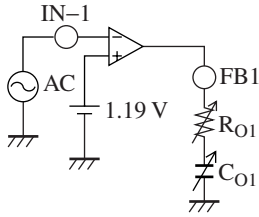


Figure 12. Error amplifier equivalent circuit ( $R_{O1}$  inserted)

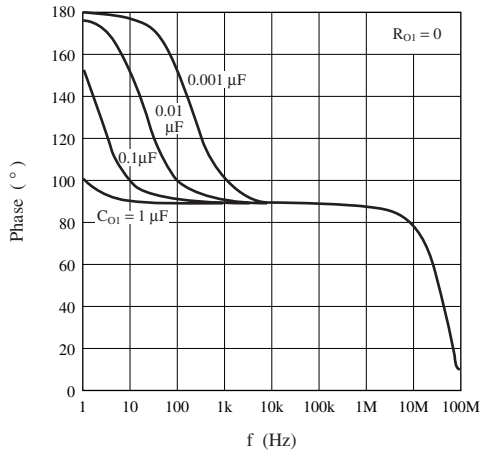
■ AC Analysis Result

- Simulation circuit

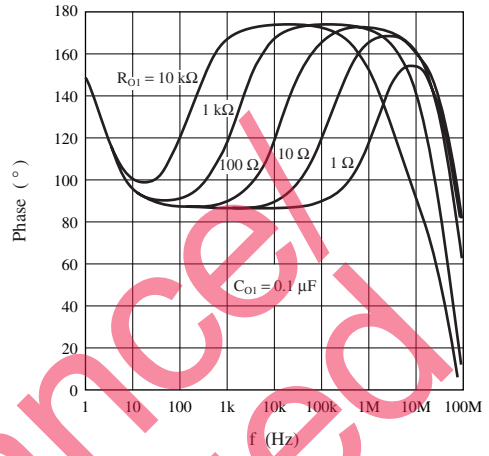


■ AC Analysis Result (continued)

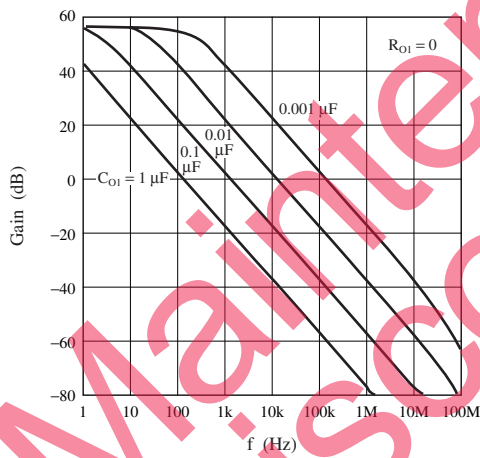
f — Phase



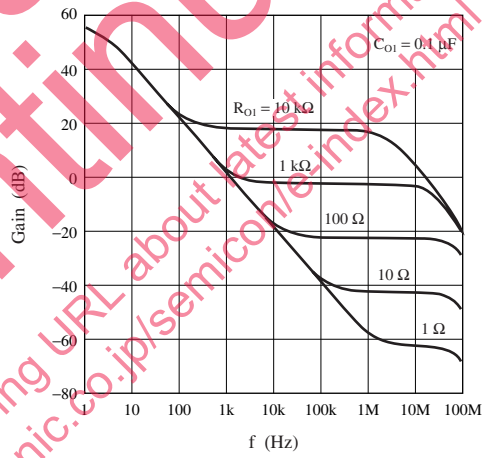
f — Phase



f — Gain



f — Gain

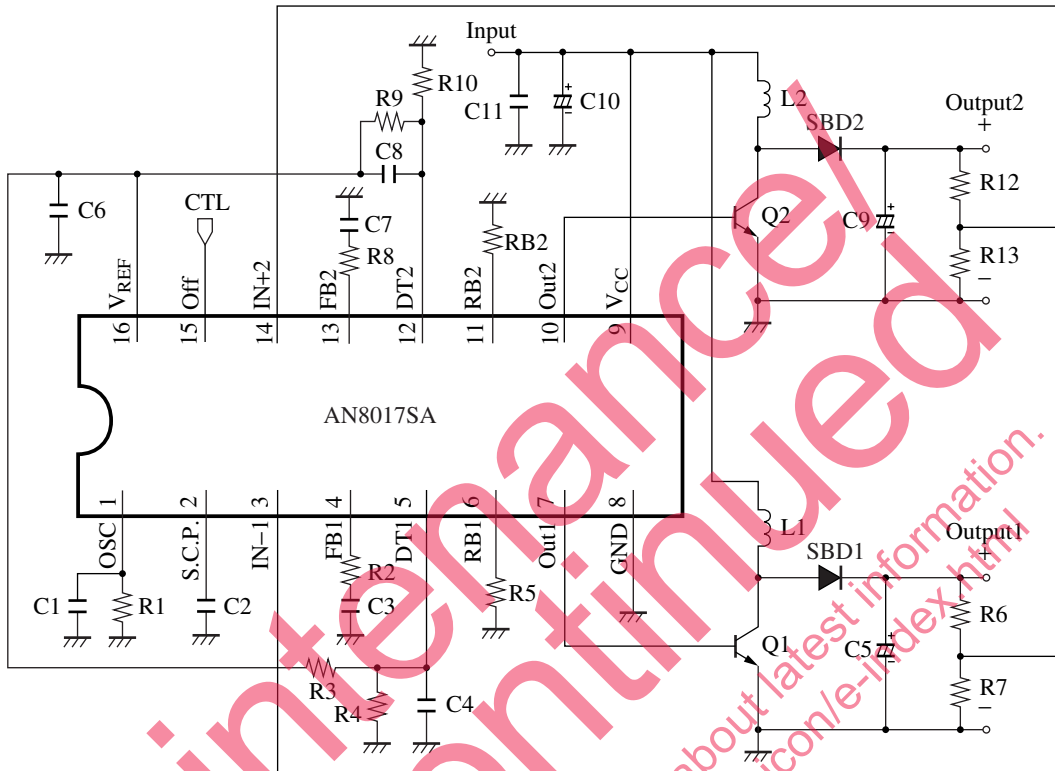


Maintenance

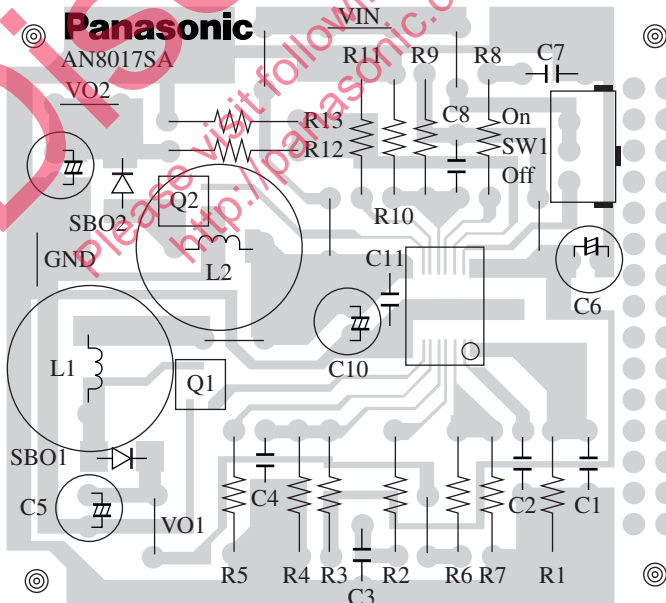
Please visit following URL about latest information.  
<http://panasonic.co.jp/semicon/info/index.html>

■ Application Circuit Examples

- Application circuit example 1



- Evaluation board





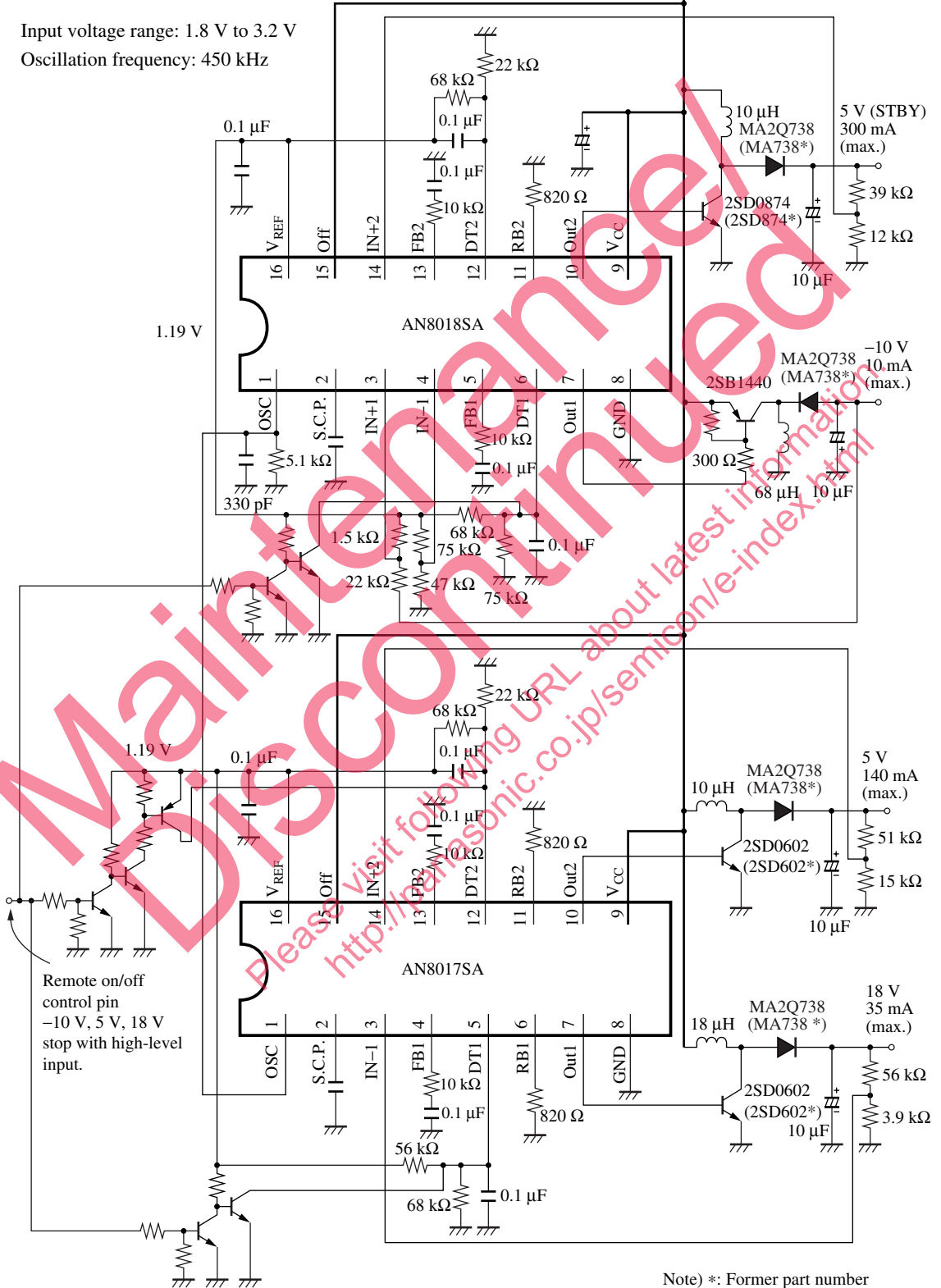
■ Application Circuit Examples (continued)

- Application circuit example 2 (Circuit using the AN8017SA/AN8018SA)

Input voltage range: 1.8 V to 3.2 V

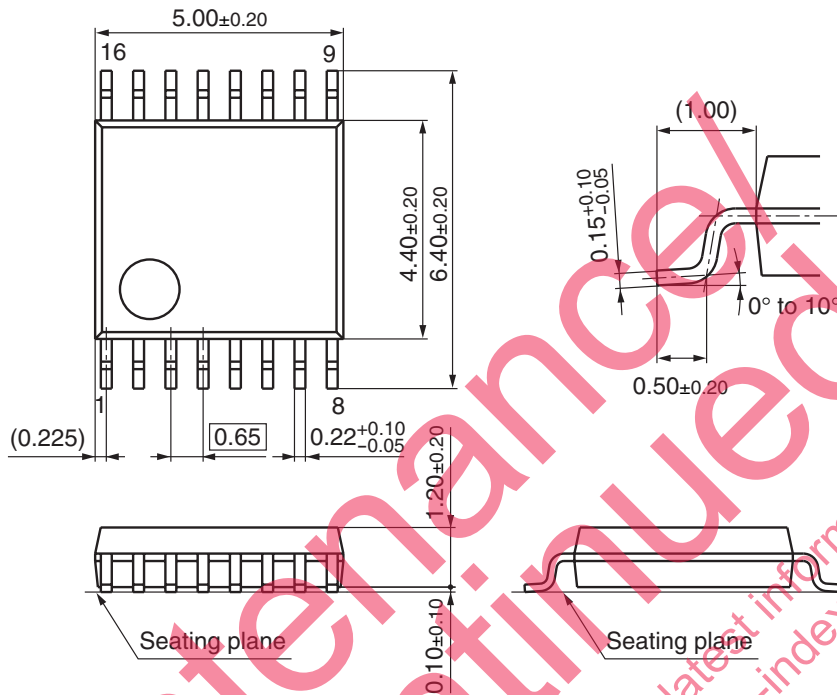
Oscillation frequency: 450 kHz

Input 1.8 V to 3.2 V



## ■ New Package Dimensions (Unit: mm)

- SSOP016-P-0225E (Lead-free package)



Maintenanced  
Discontinued

Please visit following URL about latest information.  
<http://panasonic.co.jp/semicon/e-index.html>

## Request for your special attention and precautions in using the technical information and semiconductors described in this book

- (1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.
- (2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products, and no license is granted under any intellectual property right or other right owned by our company or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.
- (3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).  
Consult our sales staff in advance for information on the following applications:
  - Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
  - Any applications other than the standard applications intended.
- (4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
- (5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
  - Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
- (6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
- (7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of Matsushita Electric Industrial Co., Ltd.