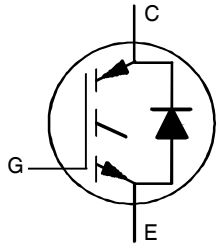
International
IOR Rectifier

IRG7PH42UD2PbF
IRG7PH42UD2-EP

INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRA-LOW VF DIODE FOR INDUCTION HEATING AND SOFT SWITCHING APPLICATIONS

Features

- Low $V_{CE\ (ON)}$ Trench IGBT Technology
- Low Switching Losses
- Square RBSOA
- 100% of the parts tested for 4X rated current (I_{LM})
- Positive $V_{CE\ (ON)}$ Temperature co-efficient
- Ultra-low V_F Diode
- Tight parameter distribution
- Lead Free Package



n-channel

V_{CES} = 1200V

I_C = 30A, T_C = 100°C

$V_{CE(on)}$ typ. = 1.69V

Benefits

- Device optimized for induction heating and soft switching applications
- High Efficiency due to Low $V_{CE(on)}$, Low Switching Losses and Ultra-low V_F
- Rugged transient Performance for increased reliability
- Excellent Current sharing in parallel operation
- Low EMI

TO-247AC
IRG7PH42UD2PbF

TO-247AD
IRG7PH42UD2-EP

G	C	E
Gate	Collector	Emitter

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRG7PH42UD2PbF	TO-247AC	Tube	25	IRG7PH42UD2PbF
IRG7PH42UD2-EP	TO-247AD	Tube	25	IRG7PH42UD2-EP

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1200	V
I_C @ T_C = 25°C	Continuous Collector Current	60	A
I_C @ T_C = 100°C	Continuous Collector Current	30	
I_{CM}	Pulse Collector Current, V_{GE}=15V	90	
I_{LM}	Clamped Inductive Load Current, V_{GE}=20V ①	120	
I_F @ T_C = 100°C	Diode Continous Forward Current	10	
I_{FSM}	Diode Non Repetitive Peak Surge Current @ T_J = 25°C ②	170	
I_{FM}	Diode Peak Repetitive Forward Current ②	90	
V_{GE}	Continuous Gate-to-Emitter Voltage	±30	V
P_D @ T_C = 25°C	Maximum Power Dissipation	321	W
P_D @ T_C = 100°C	Maximum Power Dissipation	128	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT)	—	—	0.39	°C/W
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode)	—	—	0.82	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	40	—	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 100µA ③	CT4
$V_{(BR)Transient}$	Repetitive Transient Collector-to-Emitter Voltage	—	—	1300	V	V_{GE} = 0V, T_J=75°C, PW ≤ 10µs	
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.18	—	V/°C	V_{GE} = 0V, I_C = 1mA (25°C-150°C)	CT4
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.69	2.02	V	I_C = 30A, V_{GE} = 15V, T_J = 25°C	4,5,6
		—	2.07	—		I_C = 30A, V_{GE} = 15V, T_J = 150°C	8,9,10
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	V_{CE} = V_{GE}, I_C = 1.0mA	8,9
$\Delta V_{GE(th)}/\Delta TJ$	Threshold Voltage temp. coefficient	—	-15	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.0mA (25°C - 150°C)	10,11
gfe	Forward Transconductance	—	32	—	S	V_{CE} = 50V, I_C = 30A, PW = 60µs	
I_{CES}	Collector-to-Emitter Leakage Current	—	1.0	150	µA	V_{GE} = 0V, V_{CE} = 1200V	
		—	450	1000		V_{GE} = 0V, V_{CE} = 1200V, T_J = 150°C	
V_{FM}	Diode Forward Voltage Drop	—	1.08	1.24	V	I_F = 10A	7
		—	1.0	1.15		I_F = 10A, T_J = 150°C	
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±30V	

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
Q_g	Total Gate Charge (turn-on)	—	156	234	nC	I_C = 30A	17
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	21	32		V_{GE} = 15V	CT1
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	69	104		V_{CC} = 600V	
E_{off}	Turn-Off Switching Loss	—	1320	1460	µJ	I_C = 30A, V_{CC} = 600V, V_{GE} = 15V R_G = 10Ω, L = 200µH,T_J = 25°C Energy losses include tail	CT3
$t_{d(off)}$	Turn-Off delay time	—	233	292	ns	I_C = 30A, V_{CC} = 600V, V_{GE} = 15V	
t_f	Fall time	—	64	85		R_G = 10Ω, L = 200µH,T_J = 25°C	
E_{off}	Turn-Off Switching Loss	—	2080	—	µJ	I_C = 30A, V_{CC} = 600V, V_{GE} = 15V R_G = 10Ω, L = 200µH,T_J = 150°C Energy losses include tail	CT3
$t_{d(off)}$	Turn-Off delay time	—	297	—	ns	I_C = 30A, V_{CC} = 600V, V_{GE} = 15V	WF1
t_f	Fall time	—	173	—		R_G=10Ω, L=200µH, T_J = 150°C	
C_{ies}	Input Capacitance	—	3338	—	pF	V_{GE} = 0V	16
C_{oes}	Output Capacitance	—	124	—		V_{CC} = 30V	
C_{res}	Reverse Transfer Capacitance	—	75	—		f = 1.0Mhz	
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 150°C, I_C = 120A V_{CC} = 960V, Vp =1200V Rg = 10Ω, V_{GE} = +15V to 0V	3 CT2

Notes:

① V_{CC} = 80% (V_{CES}), V_{GE} = 20V, L = 200µH, R_G = 10Ω.

② Pulse width limited by max. junction temperature.

③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.

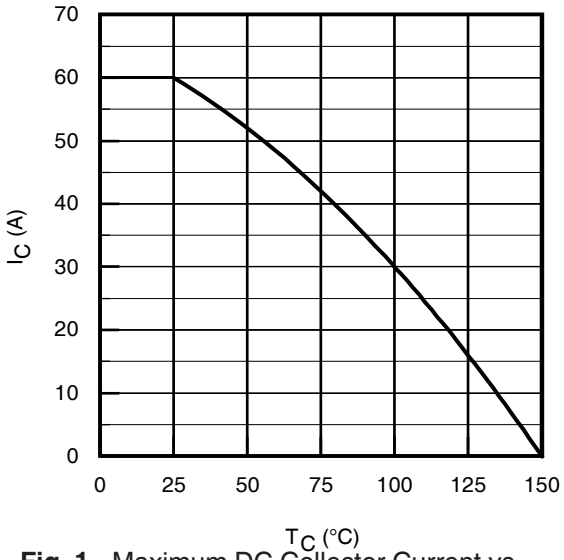


Fig. 1 - Maximum DC Collector Current vs. Case Temperature

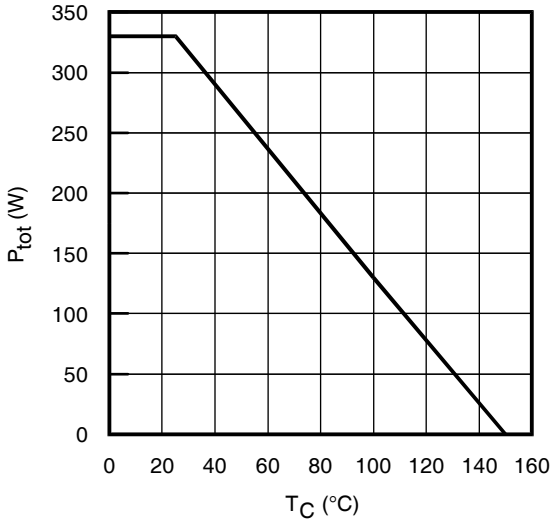


Fig. 2 - Power Dissipation vs. Case Temperature

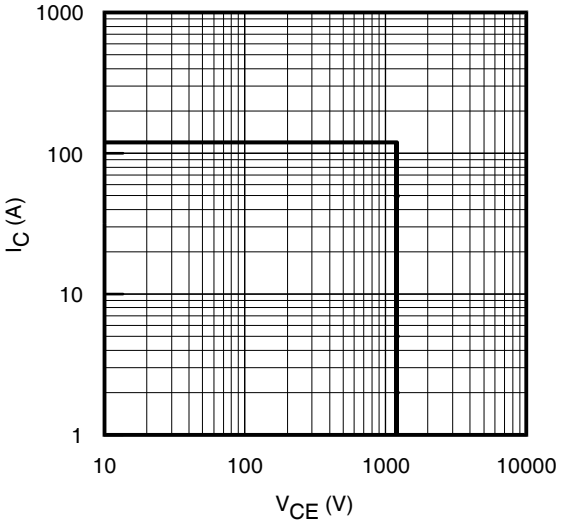


Fig. 3 - Reverse Bias SOA
T_J = 150°C; V_{GE} =15V

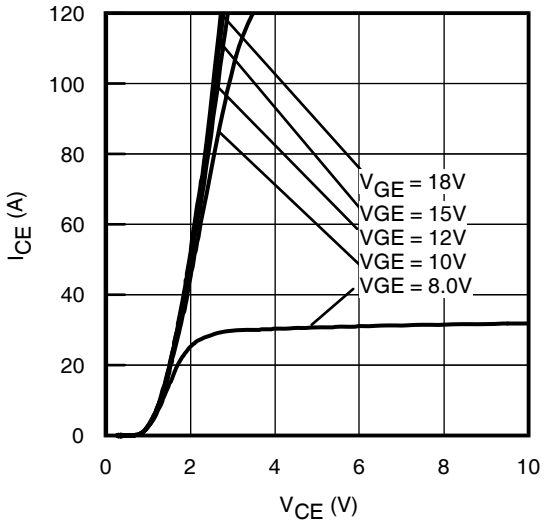


Fig. 4 - Typ. IGBT Output Characteristics
T_J = -40°C; tp = 80µs

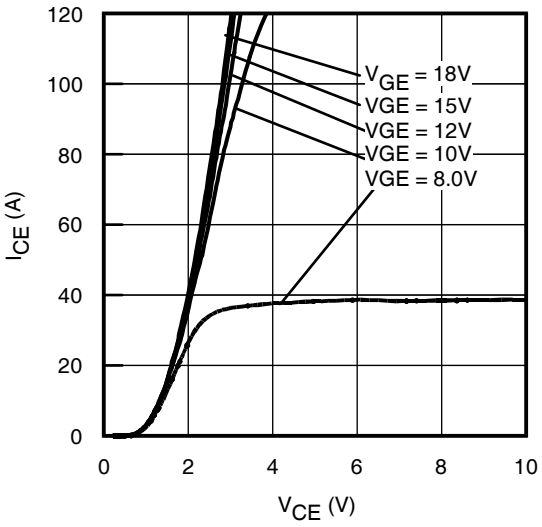


Fig. 5 - Typ. IGBT Output Characteristics
T_J = 25°C; tp = 80µs

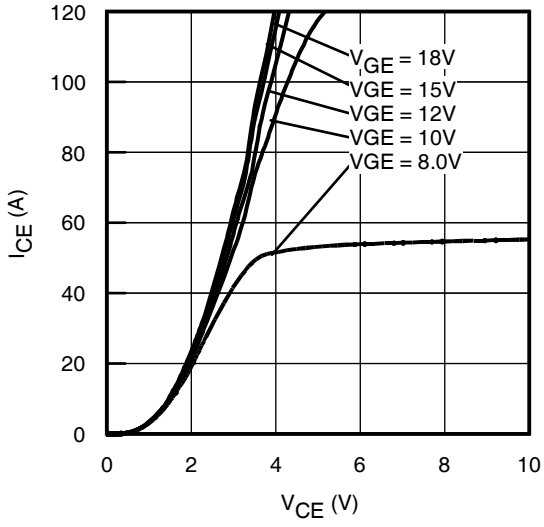


Fig. 6 - Typ. IGBT Output Characteristics
T_J = 150°C; tp = 80µs

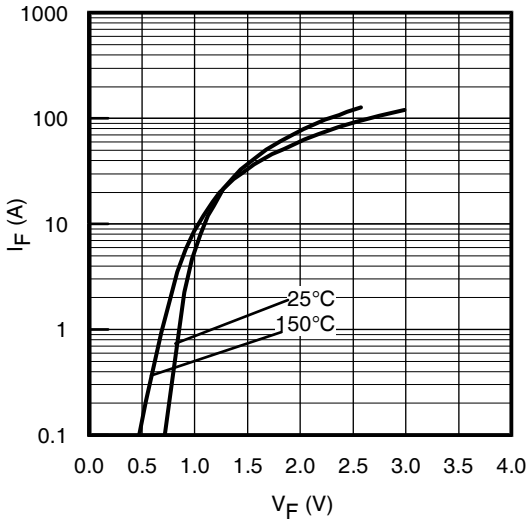


Fig. 7 - Typ. Diode Forward Voltage Drop Characteristics

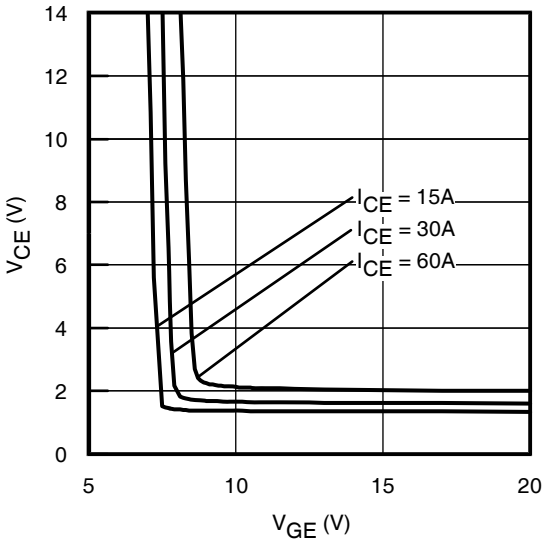


Fig. 8 - Typical V_{CE} vs. V_{GE}
T_J = -40°C

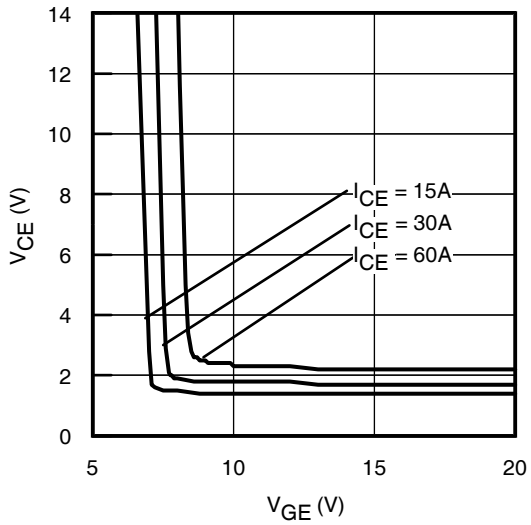


Fig. 9 - Typical V_{CE} vs. V_{GE}
T_J = 25°C

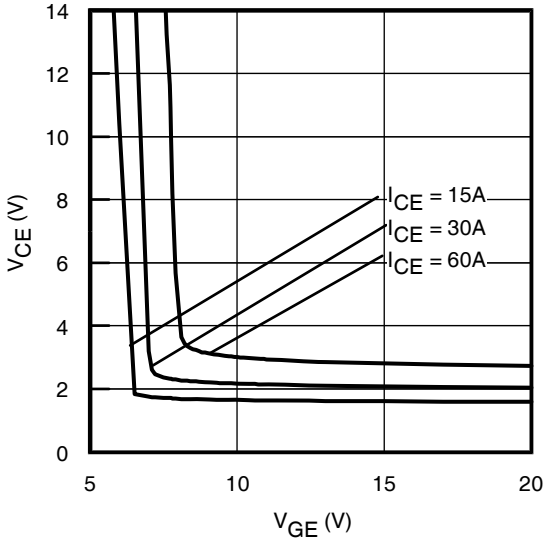


Fig. 10 - Typical V_{CE} vs. V_{GE}
T_J = 150°C

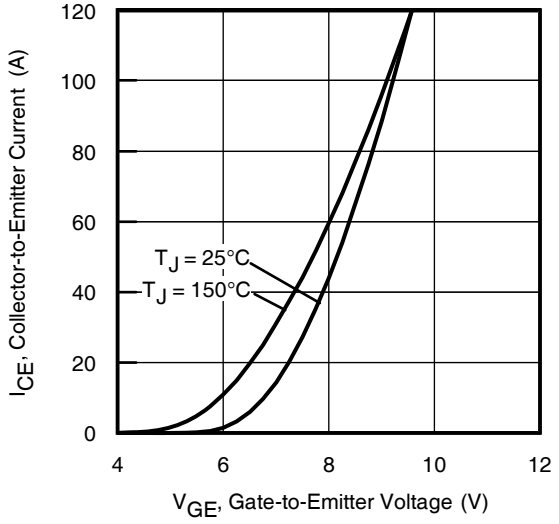


Fig. 11 - Typ. Transfer Characteristics
V_{CE} = 50V; tp = 10µs

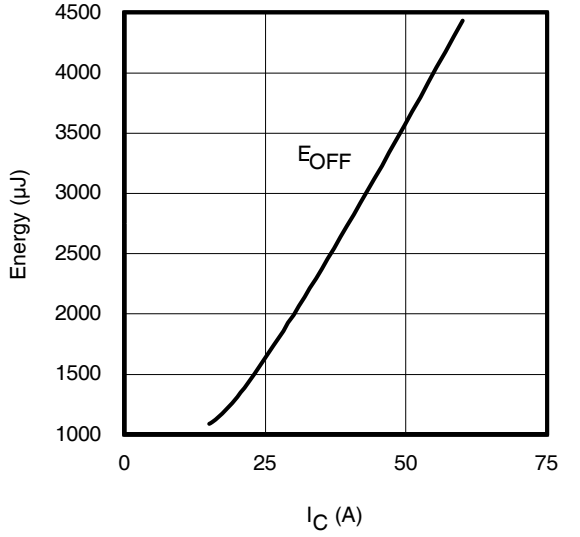


Fig. 12 - Typ. Energy Loss vs. I_C
T_J = 150°C; L = 200µH; V_{CE} = 600V, R_G = 10Ω; V_{GE} = 15V

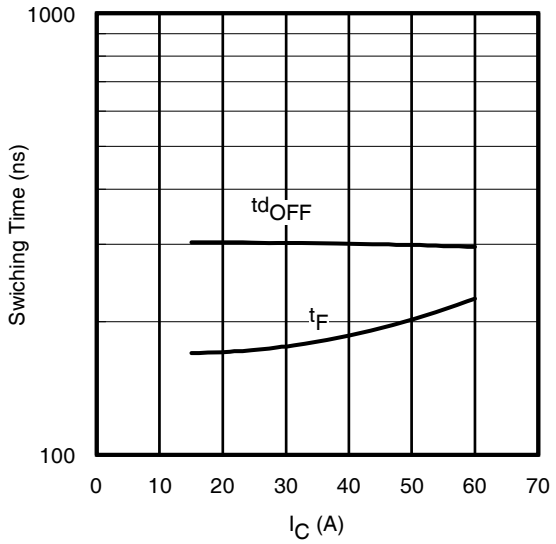


Fig. 13 - Typ. Switching Time vs. I_C
T_J = 150°C; L = 200µH; V_{CE} = 600V, R_G = 10Ω; V_{GE} = 15V

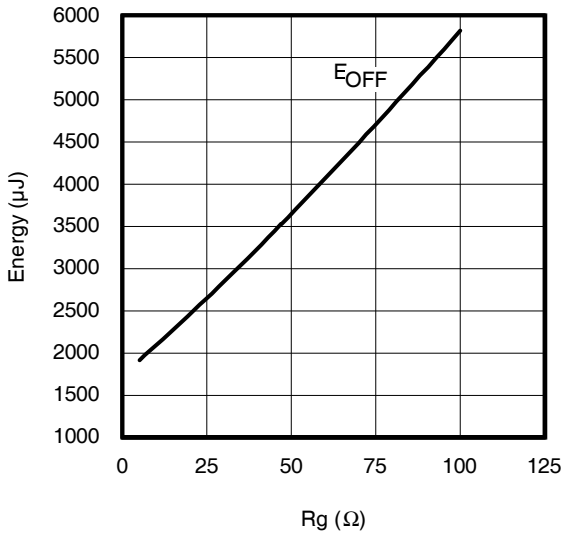


Fig. 14 - Typ. Energy Loss vs. R_G
T_J = 150°C; L = 200µH; V_{CE} = 600V, I_{CE} = 30A; V_{GE} = 15V

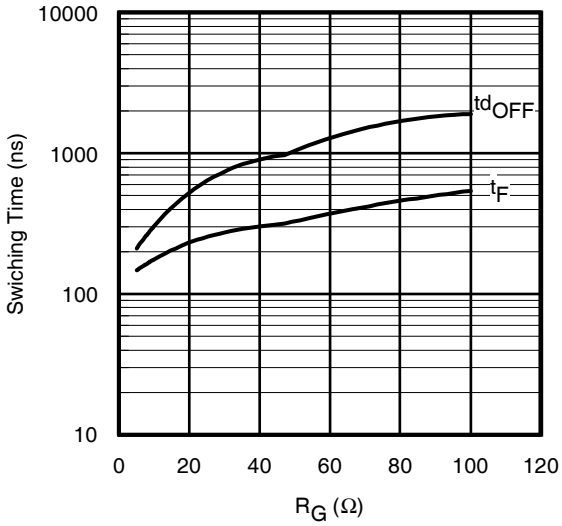


Fig. 15 - Typ. Switching Time vs. R_G
T_J = 150°C; L = 200µH; V_{CE} = 600V, I_{CE} = 30A; V_{GE} = 15V

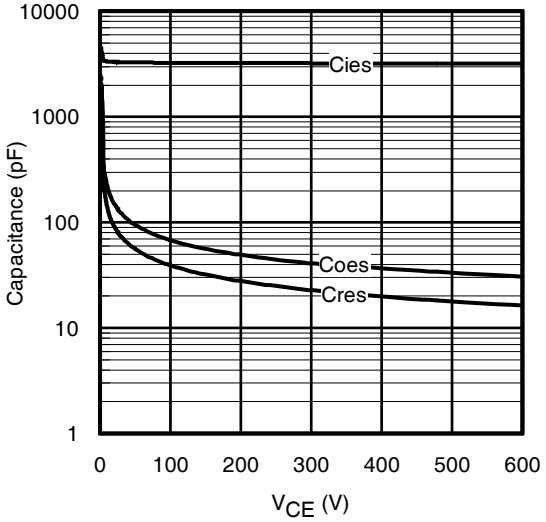


Fig. 16 - Typ. Capacitance vs. V_{CE}
V_{GE}= 0V; f = 1MHz

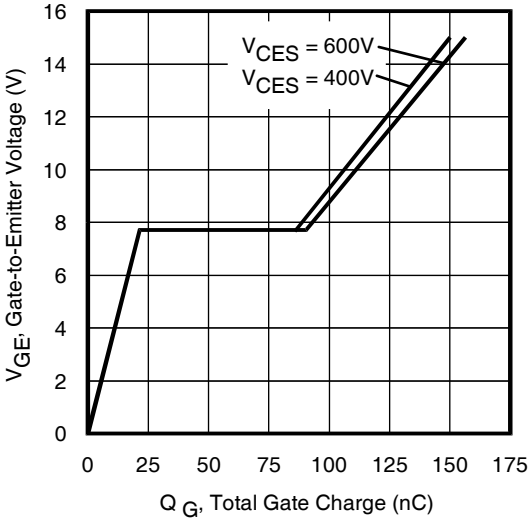


Fig. 17 - Typical Gate Charge vs. V_{GE}
I_{CE} = 30A; L = 600µH

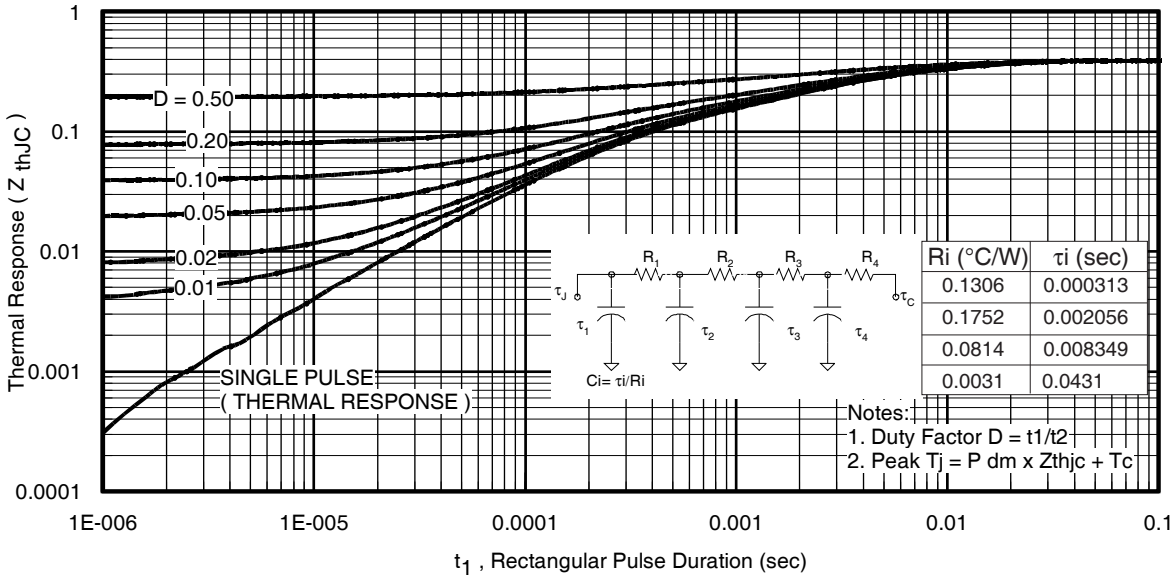


Fig 18. Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

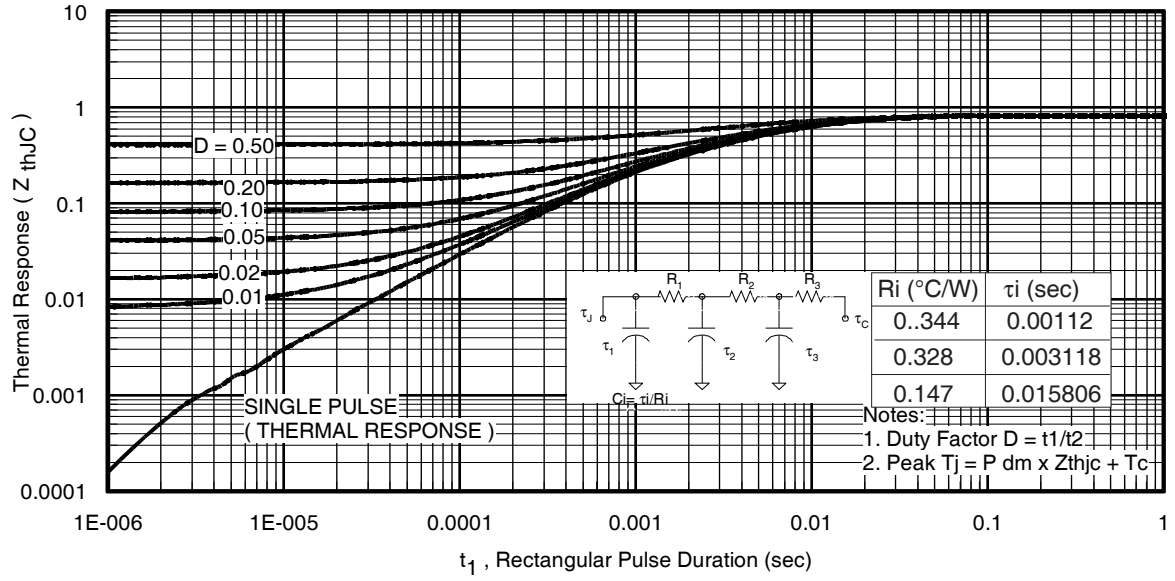


Fig. 19. Maximum Transient Thermal Impedance, Junction-to-Case (DIODE)

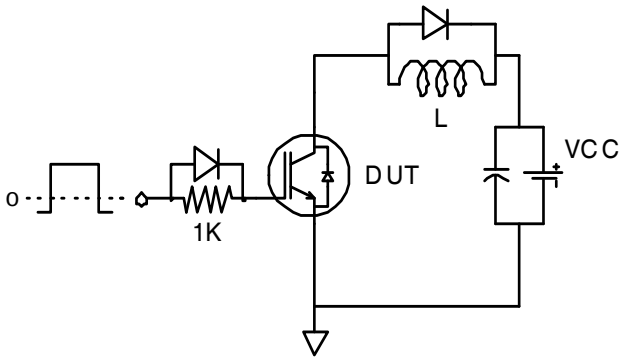


Fig.C.T.1 - Gate Charge Circuit (turn-off)

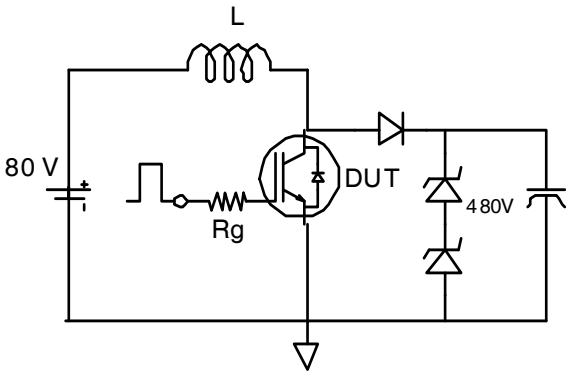


Fig.C.T.2 - RBSOA Circuit

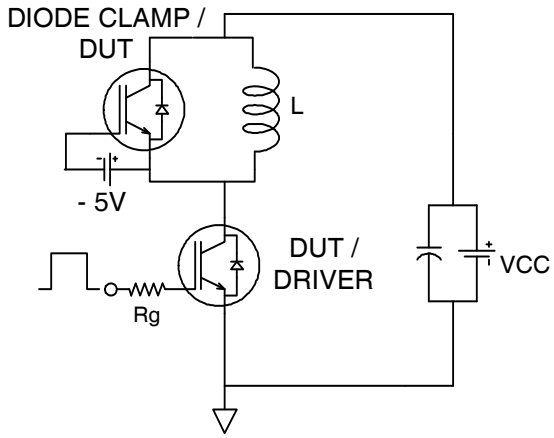


Fig.C.T.3 - Switching Loss Circuit

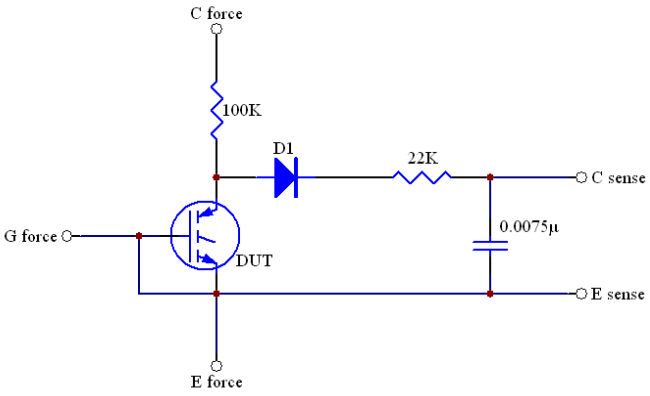


Fig.C.T.4 - BVCES Filter Circuit

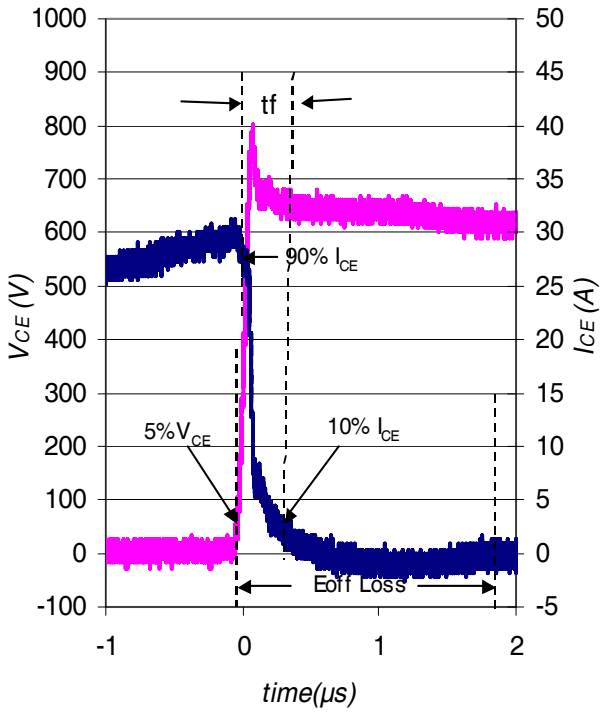
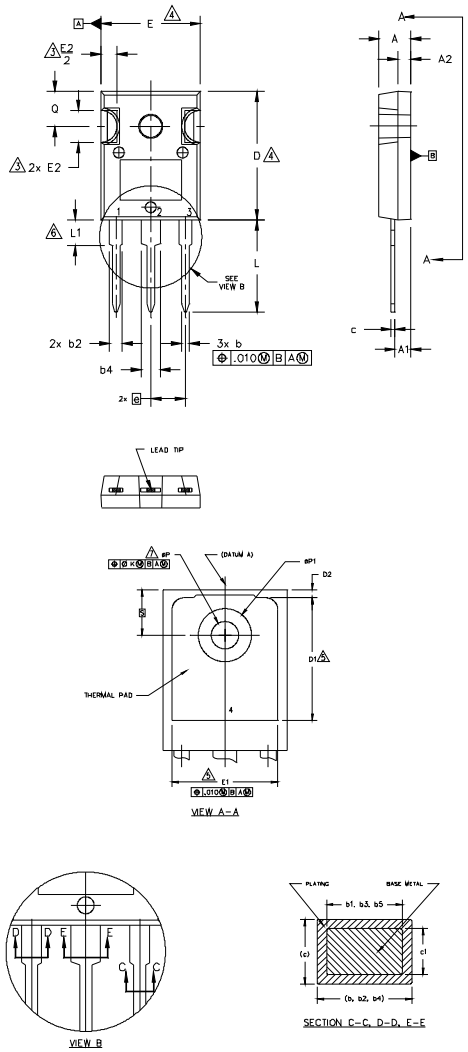


Fig. WF1 - Typ. Turn-off Loss Waveform
@ T_J = 150°C using Fig. CT.3

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

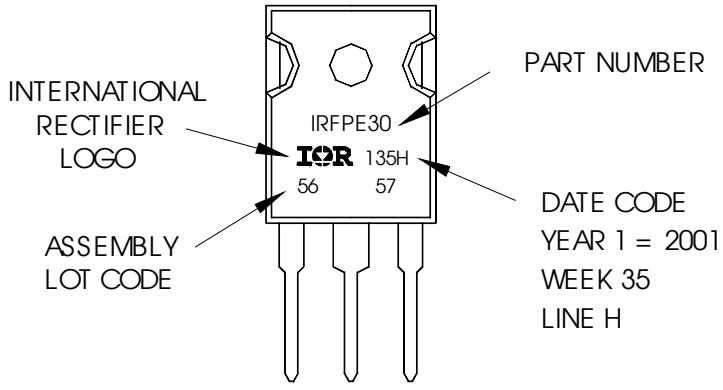
DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"

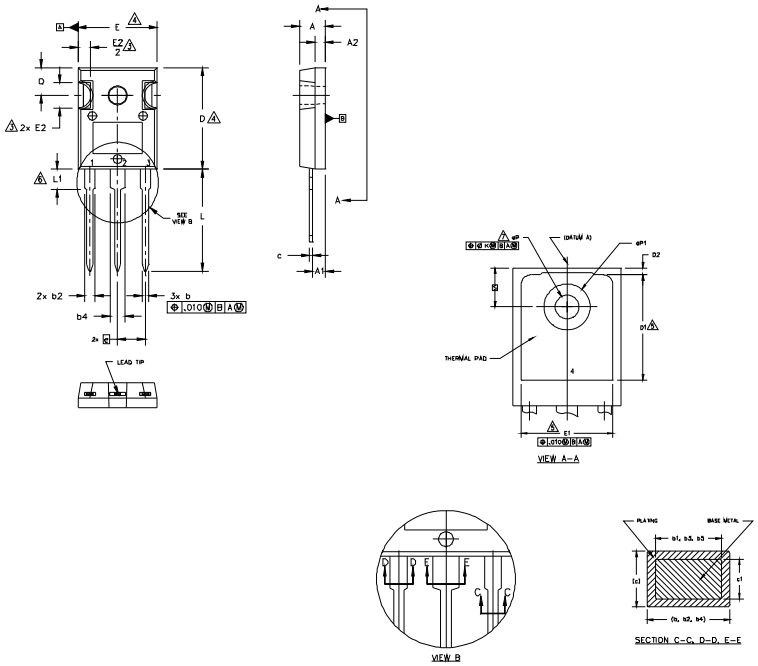


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. øP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	–	13.08	–	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	–	13.46	–	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	–	.291	–	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

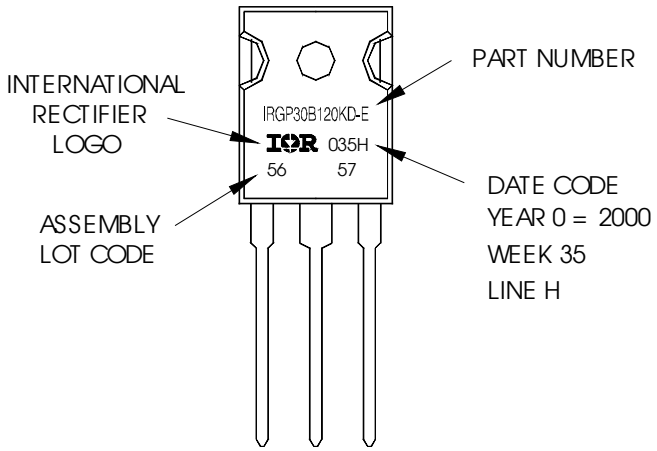
DIODES

1.– ANODE/OPEN
2.– CATHODE
3.– ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Qualification Information†

Qualification Level	Industrial† (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	TO-247AC	N/A
	TO-247AD	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability
†† Applicable version of JEDEC standard at the time of product release

Revision History

Date	Comments
8/20/2014	• Datasheet updated based on IR corporate template.
	• Removed "APPROVED (not released)" from top header on page 1.