

DATA SHEET

SKY13372-467LF: 0.1 to 6.0 GHz High-Isolation SPDT Absorptive Switch

Applications

- GSM, PCS, WCDMA base stations
- 2.4 and 5.8 GHz ISM devices
- Wireless local loops

Features

- Single, positive voltage control: 0 to 3 and 0 to 5 V
- High isolation 64 dB at 1 GHz and 2 GHz
- Integrated silicon CMOS driver
- Absorptive
- Small QFN (16-pin, 4 x 4 mm) Pb-free package (MSL1, 260 °C per JEDEC J-STD-020)



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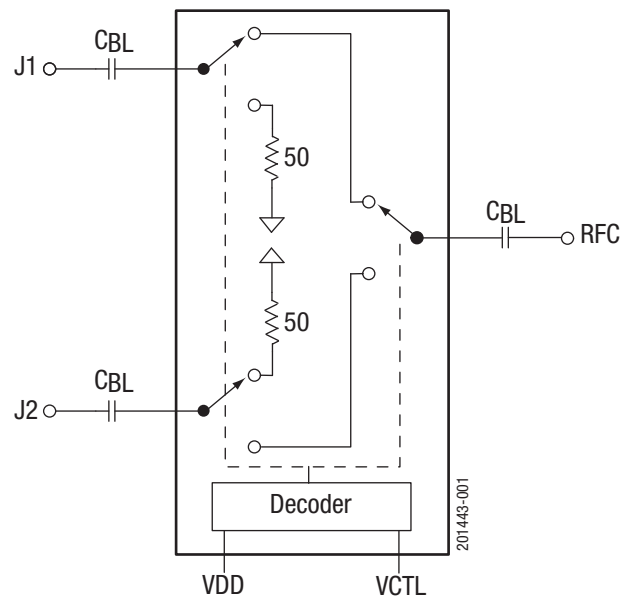


Figure 1. SKY13372-467LF Block Diagram

Description

The SKY13372-467LF is a GaAs pHEMT FET high-isolation, absorptive switch. The device is an ideal component for base station applications in which synthesizer isolation is critical.

The device is provided in a 4 x 4 mm, 16-pin Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

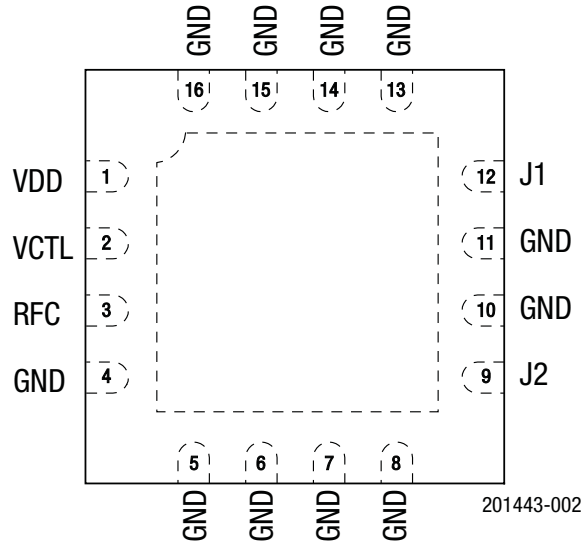


Figure 2. SKY13372-467LF Pinout (Top View)

Table 1. SKY13372-467LF Signal Descriptions¹

Pin	Name	Description	Pin	Name	Description
1	VDD	DC power supply	9	J2	RF output 2. Must be DC blocked.
2	VCTL	DC switch control pin. Switches insertion loss state from RFC to J1 or J2 (see Table 4).	10	GND	Ground
3	RFC	RF input. Must be DC blocked.	11	GND	Ground
4	GND	Ground	12	J1	RF output 1. Must be DC blocked.
5	GND	Ground	13	GND	Ground
6	GND	Ground	14	GND	Ground
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	GND	Ground

¹ Exposed pad on bottom of package must be grounded.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13372-467LF are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the SKY13372-467LF are illustrated in Figures 3 through 7.

The state of the SKY13372-467LF is determined by the logic provided in Table 4.

Table 2. SKY13372-467LF Absolute Maximum Ratings¹

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V _{DD}	2.7	5.5	V
RF input power @ >500 MHz (@ V _{DD} = 5 V)	V _I		1	W
RF input power @ >500 MHz (@ V _{DD} = 3 V)	V _I		0.25	W
Operating temperature	T _{OP}	-40	+105	°C
Storage temperature	T _{STG}	-65	+150	°C

ESD HANDLING: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.

Table 3. SKY13372-467LF Electrical Specifications¹ (1 of 2)

(V_{CTL} = 0 V/3 V, V_{DD} = 3 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z₀] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
CW insertion loss	IL	0.1 to 2.0 GHz		0.8	1.1	dB
		2.0 to 3.0 GHz		0.9	1.2	dB
		3.0 to 4.0 GHz		1.0	1.3	dB
		4.0 to 6.0 GHz		1.7	1.9	dB
Isolation	Iso	0.1 to 2.0 GHz	56	65		dB
		2.0 to 3.0 GHz	53	60		dB
		3.0 to 4.0 GHz	50	55		dB
		4.0 to 6.0 GHz	40	42		dB
Return loss (insertion loss state)	RL	0.1 to 2.0 GHz		22		dB
		2.0 to 3.0 GHz		22		dB
		3.0 to 4.0 GHz		17		dB
		4.0 to 6.0 GHz		15		dB
Return loss (isolation state)	RL	0.5 to 2.0 GHz		10		dB
		2.0 to 3.0 GHz		25		dB
		3.0 to 4.0 GHz		18		dB
		4.0 to 6.0 GHz		13		dB
1 dB input compression point (V _{DD} = V _{CTRL} = 5 V)	IP1dB	0.4 to 1.0 GHz	+27	+29		dBm
		1.0 to 2.0 GHz	+28	+30		dBm
		2.0 to 3.0 GHz	+28	+30		dBm
		3.0 to 4.0 GHz	+26	+28		dBm
Third order input intercept point (Δf = 1 MHz, P _{IN} = +7 dBm/tone) (V _{DD} = V _{CTRL} = 5 V)	IIP3	0.4 to 1.0 GHz	+45	+48		dBm
		1.0 to 2.0 GHz	+44	+47		dBm
		2.0 to 3.0 GHz	+42	+45		dBm
		3.0 to 4.0 GHz	+40	+43		dBm

Table 3. SKY13372-467LF Electrical Specifications¹ (2 of 2)
(V_{CTL} = 0 V/3 V, V_{DD} = 3 V, T_{OP} = +25 °C, P_{IN} = 0 dBm, Characteristic Impedance [Z₀] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications (continued)						
Switching rise time	T _{RISE}	10% to 90% RF		40		ns
Switching fall time	T _{FALL}	90% to 10% RF		40		ns
Switching on time	T _{ON}	50% V _{CTL} to 90% RF		100		ns
Switching off time	T _{OFF}	50% V _{CTL} to 10% RF		100		ns
Switching on time	T _{ON}	50% V _{CTL} to 98% RF, T _{OP} = -40 °C to +85 °C		1	2	μs
Switching off time	T _{OFF}	50% V _{CTL} to 2% RF, T _{OP} = -40 °C to +85 °C		100	300	ns
Insertion loss settling time	ΔIL	Insertion loss in dB measured @ 1 μs (referenced to a rising 10% RF level on J1 and J2) minus the CW insertion loss in dB. Freq = 2 GHz, T _{OP} = -40 °C to +85 °C, V _{CTL} = 5 V, pulse width = 1.15 ms, 50% duty cycle.			0.25	dB
DC Specifications						
Control voltage: Low High	V _{CTL}		-1 0.7 × V _{DD} ; 3.0 for V _{DD} > 4.0 V		0.3 × V _{DD} V _{DD}	V V
Control current	I _{CTL}				5	μA
Supply voltage	V _{DD}		2.7		5.0	V
Supply current	I _{DD}				100	μA
Supply voltage: V _{DD} = 5.0 and V _{CTL} = 2.7 V ²						

¹ Performance is guaranteed only under the conditions listed in this table.

² For lowest possible I_{DD}, V_{CTL} should be as close as possible to V_{DD}.

Typical Performance Characteristics

($V_{CTL} = 0\text{ V}$, $V_{DD} = 3\text{ V}$, $T_{OP} = +25\text{ }^{\circ}\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\text{ }\Omega$, Unless Otherwise Noted)

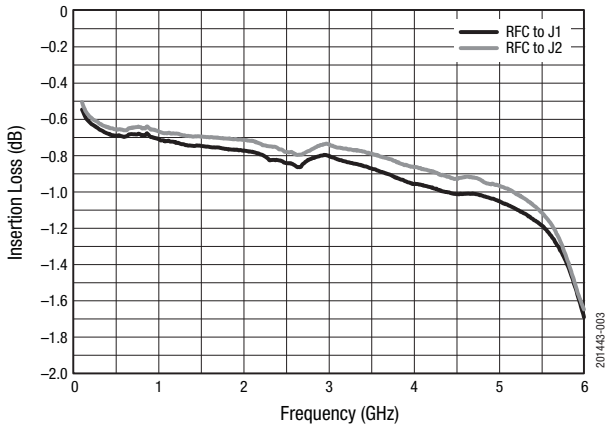


Figure 3. Insertion Loss vs Frequency

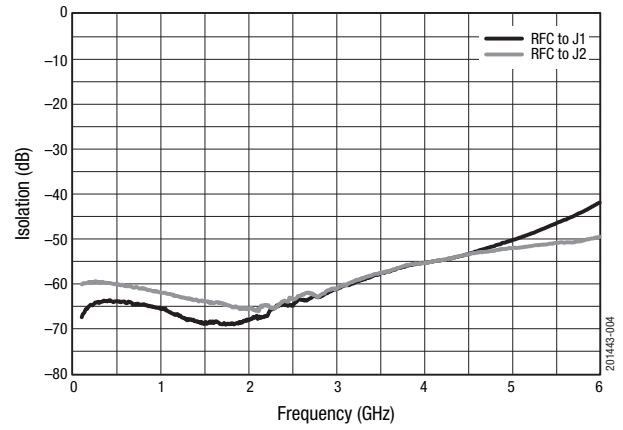


Figure 4. Isolation vs Frequency

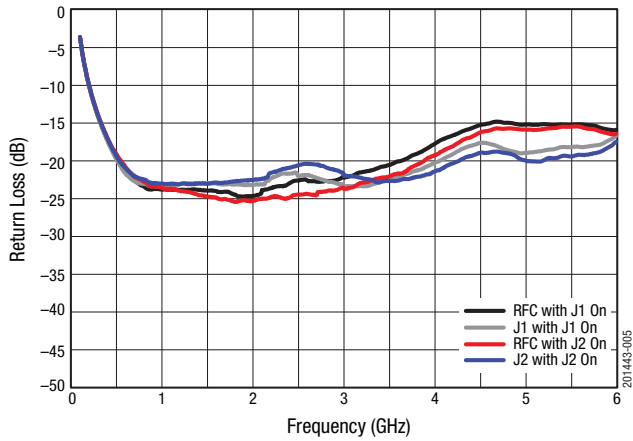


Figure 5. Return Loss vs Frequency (Insertion Loss State)

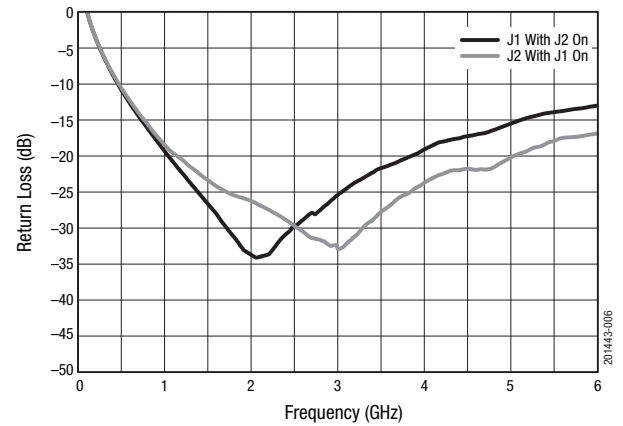


Figure 6. Return Loss vs Frequency (Isolation State)

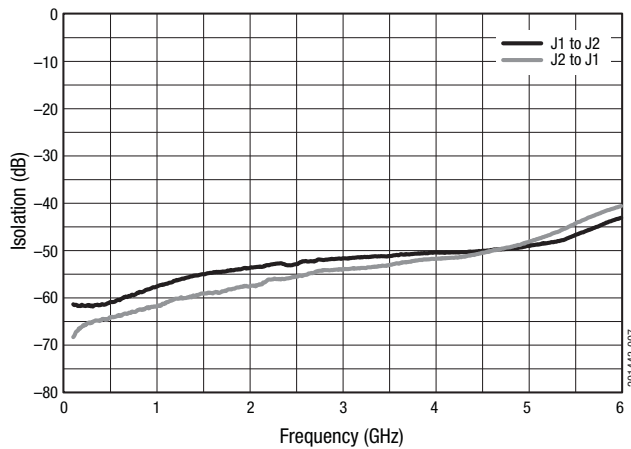


Figure 7. Output to Output Isolation vs Frequency

Table 4. SKY13372-467LF Truth Table

VCTL	RFC to J1	RFC to J2
0	Insertion loss	Isolation
1	Isolation	Insertion loss

Evaluation Board Description

The SKY13372-467LF Evaluation Board is used to test the performance of the SKY13372-467LF SPDT absorptive switch.

An assembly drawing for the Evaluation Board is shown in Figure 8.

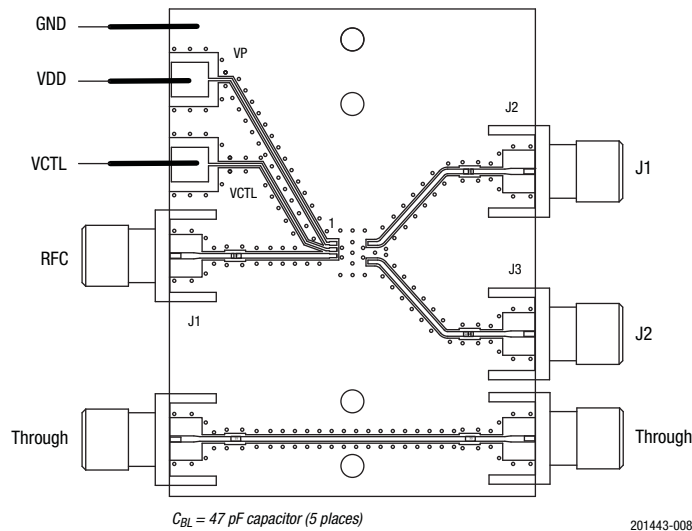


Figure 8. SKY13372-467LF Evaluation Board Assembly Diagram

Package Dimensions

The PCB layout footprint for the SKY13372-467LF is shown in Figure 9. Typical part markings are noted in Figure 10. Package dimensions are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13372-467LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

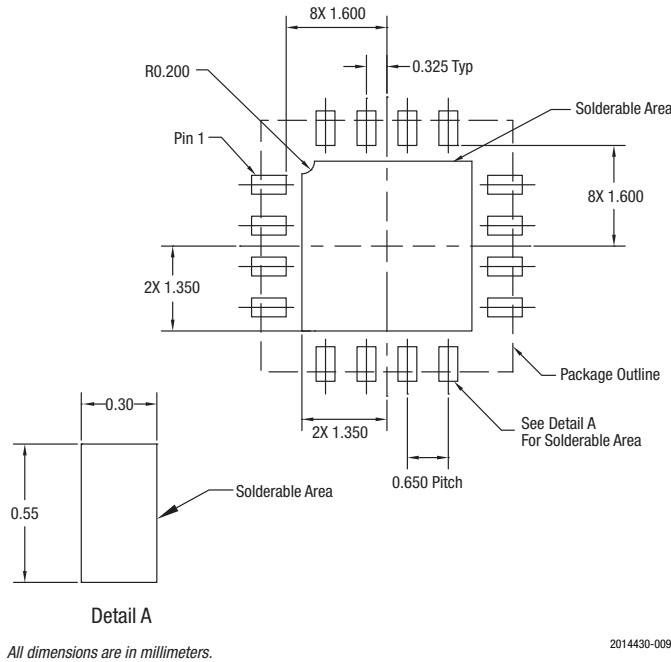


Figure 9. SKY13372-467LF PCB Layout Footprint

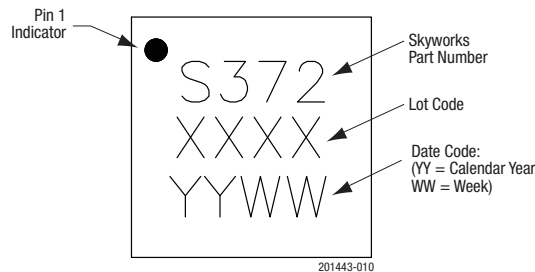
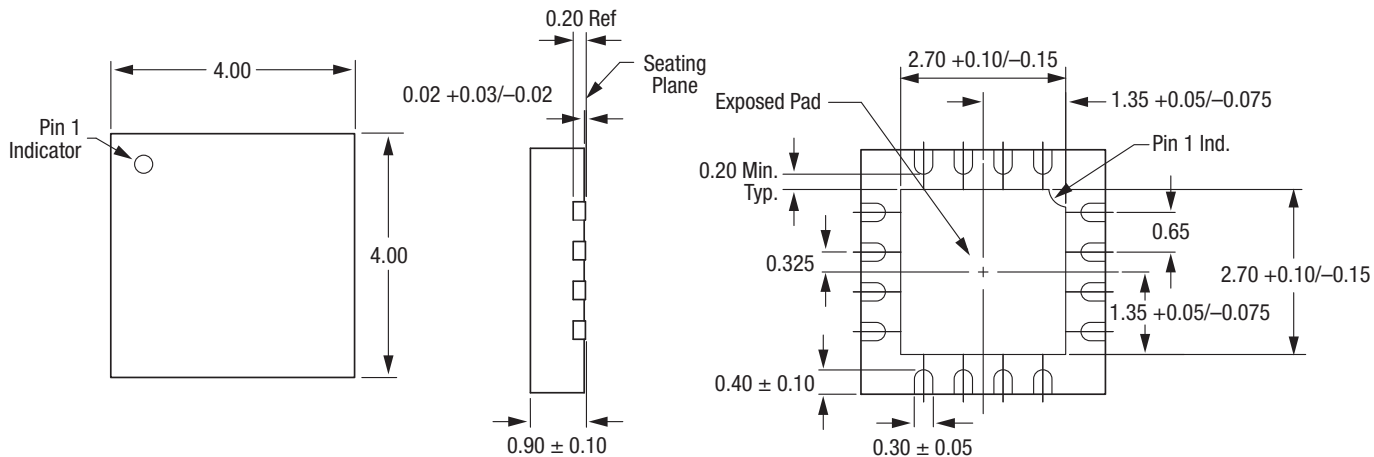


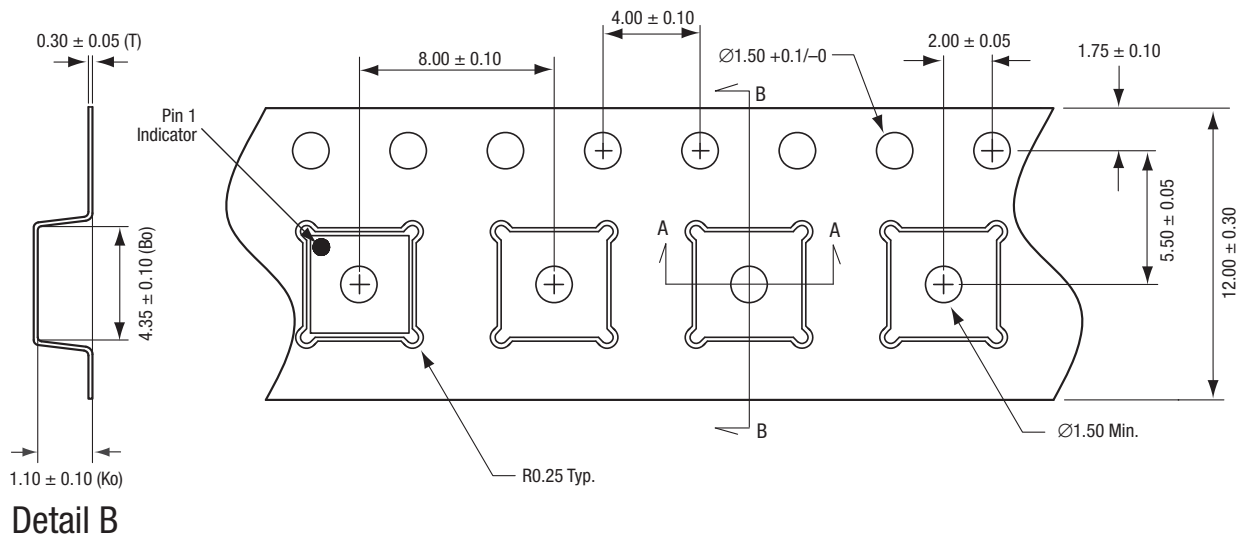
Figure 10. Typical Part Markings



All dimensions are in millimeters

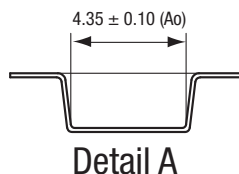
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Figure 11. SKY13372-467LF Package Dimensions



Notes:

1. Carrier tape material: black conductive polystyrene, non-bakeable
2. Cover tape material: transparent conductive HSA
3. Cover tape size: 9.2 mm width
4. ESD surface resistivity is $\geq 1 \times 10^5 \sim 1 \times 10^{10}$ Ohms/square per EIA, JEDEC TNR Specification.
5. All measurements are in millimeters



Detail A

201443-012

Figure 12. SKY13372-467LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13372-467LF SPDT Absorptive Switch	SKY13372-467LF	SKY13372-467-EVB

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