PIC10(L)F320/322

PIC10(L)F320/322 Family
Silicon Errata and Data Sheet Clarification

The PIC10(L)F320/322 family devices that you have received conform functionally to the current Device Data Sheet (DS40001585**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC10(L)F320/322 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC10(L)F320/322 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEV<8:0>[1]	Revision ID for Silicon Revision[2]			
		A1	A2	A3	A4
PIC10F320	10 1001 101	0 0001	0 0010	0 0011	0 0100
PIC10LF320	10 1001 111	0 0001	0 0010	0 0011	0 0100
PIC10F322	10 1001 100	0 0001	0 0010	0 0011	0 0100
PIC10LF322	10 1001 110	0 0001	0 0010	0 0011	0 0100

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of the Configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC10(L)F320/322 Flash Memory Programming Specification"* (DS41572) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2:   SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]			
				A1	A2	A3	A4
Ipd and Idd	Maximum Limit	1.1	Maximum current limits may be higher than specified in Tables 24-2 and 24-3 of the data sheet.	X	X	X	
Complementary Waveform Generator (CWG)	Auto-Shutdown/ Auto-Restart	2.1	Auto-Shutdown improper overrides.	X	X		
Numerically Controlled Oscillator (NCO)	Output Control	3.1	Output Control affected by Reference Clock Output Control.	X	X	X	X
FVR	FVR Module	4.1	Use of FVR module can cause device to Reset.	X	X	X	X
Data Memory (SRAM)	Memory Size	5.1	The data memory size on the PIC10(L)F320 devices is 32 bytes.	X			

Note 1:   Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: I_PD and I_DD

1.1 I_PD and I_DD Maximum Limits

The I_PD and I_DD limits do not match the data sheet, and may be higher at lower oscillator speeds 32 kHz and 500 kHz.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X					

2. Module: Complementary Waveform Generator (CWG)

2.1 CWG Auto-Shutdown Termination

When the Auto-Shutdown Event Status bit, GxASE, is cleared, the shutdown overrides are improperly relinquished enabling the CWG outputs immediately. The proper operation is for the overrides to remain in effect until the first input rising edge after the G1ASE bit is cleared.

Work around

None.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X						

3. Module: Numerically Controlled Oscillator (NCO)

3.1 NCO Output Pin (NCO1)

The NCO module normally requires that the TRIS bit associated with the NCO1 output pin is cleared to enable output, (i.e., TRISA2 = 0). When the clock reference module output is also enabled, (CLKROE = 1), the TRIS bit function will inadvertently be overridden, configuring the port pin as an output.

Work around

Disable the Reference Clock Output, (CLKROE = 0), when using the NCO1 output.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

4. Module: FVR

4.1 FVR Module

When using the FVR Module, if the gain amplifier output is set via the ADFVR bit in FVRCON while the module is disabled (FVREN = 0), the internal oscillator frequency may shift, the device current consumption can increase and a Brown-out Reset may occur. Additionally, after the FVREN is enabled, a switch from 4x to 1x can also cause a Reset.

Work around

Set the FVREN bit of FVRCON to enable the module, prior to adjusting the amplifier output selection with the ADFVR bit.

Always set the amplifier output selection to off ('0') before disabling the FVR module. When switching from 4x to 1x, first switch from 4x to 2x and then from 2x to 1x.

Affected Silicon Revisions

A1	A2	A3	A4				
X	X	X	X				

5. Module: Data Memory (SRAM)

5.1 Data Memory Size

On the PIC10(L)F320 devices with a silicon revision of A1, the data memory size is 32 bytes. On the subsequent revisions of the PIC10(L)F320 devices (A2 and greater), the data memory size has been increased to 64 bytes.

Work around

If more data memory is required, an upgrade to a later silicon revision (A2 and greater) is required.

Affected Silicon Revisions

A1	A2	A3	A4				
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001585**C**):

> **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

PIC10(L)F320/322

APPENDIX A: REVISION HISTORY

Rev A Document (09/2011)

Initial release of this document.

Rev B Document (03/2012)

Data Sheet Clarifications: Added Modules 1 to 5.

Rev C Document (04/2012)

Data Sheet Clarifications: Added Module 6.

Rev D Document (06/2013)

Added Modules 4 and 5; Other minor corrections.

Rev E Document (07/2013)

Added Silicon Revision A3; Other minor corrections.

Rev F Document (12/2013)

Added Silicon Revision A4; Added Module 6; Other minor corrections.

Rev G Document (5/2015)

Revised Module 1; Removed Module 6; Other minor corrections.

Data Sheet Clarifications: Removed – data sheet updated.

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