

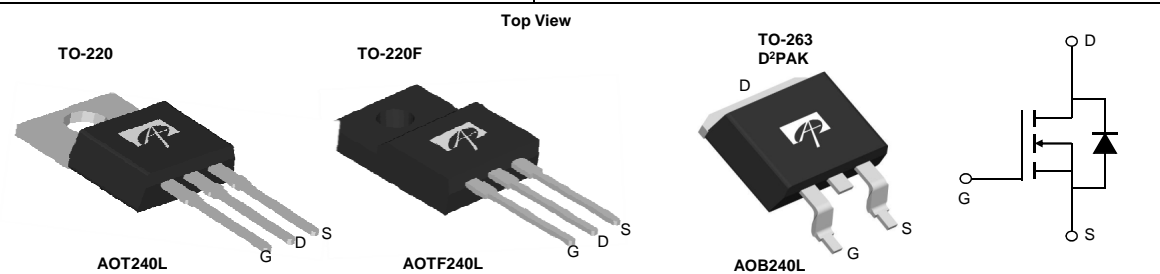
General Description

The AOT240L & AOB240L & AOTF240L uses Trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and C_{rss} .

Product Summary

V_{DS}	40V
I_D (at $V_{GS}=10V$)	105A/85A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 2.9m Ω (< 2.6m Ω^*)
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 3.7m Ω (< 3.5m Ω^*)

100% UIS Tested
 100% R_g Tested


Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	AOT240L/AOB240L	AOTF240L	Units
Drain-Source Voltage	V_{DS}	40		V
Gate-Source Voltage	V_{GS}	± 20		V
Continuous Drain Current ^G	$T_C=25^\circ C$	105	85	A
	$T_C=100^\circ C$	82	60	
Pulsed Drain Current ^C	I_{DM}	400		
Continuous Drain Current	$T_A=25^\circ C$	20		A
	$T_A=70^\circ C$	16		
Avalanche Current ^C	I_{AS}	68		A
Avalanche energy $L=0.1mH$ ^C	E_{AS}	231		mJ
Power Dissipation ^B	$T_C=25^\circ C$	176	41	W
	$T_C=100^\circ C$	88	20	
Power Dissipation ^A	$T_A=25^\circ C$	1.9		W
	$T_A=70^\circ C$	1.2		
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175		$^\circ C$

Thermal Characteristics

Parameter	Symbol	AOT240L/AOB240L	AOTF240L	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	15	15	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	65	65
Maximum Junction-to-Case	$R_{\theta JC}$	0.85	3.6	$^\circ C/W$

* Surface mount package TO263

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.7	2.2	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	400			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A TO220/TO220F T _J =125°C		2.4	2.9	mΩ
		V _{GS} =4.5V, I _D =20A TO220/TO220F		3	3.7	
		V _{GS} =10V, I _D =20A TO263		2.1	2.6	mΩ
		V _{GS} =4.5V, I _D =20A TO263		2.7	3.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		78		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.65	1	V
I _S	Maximum Body-Diode Continuous Current ^G				105	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		3510		pF
C _{oss}	Output Capacitance			1070		pF
C _{rss}	Reverse Transfer Capacitance			68		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.5	1	1.5	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A		49	72	nC
Q _g (4.5V)	Total Gate Charge			22	32	nC
Q _{gs}	Gate Source Charge			9		nC
Q _{gd}	Gate Drain Charge			7		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =1Ω, R _{GEN} =3Ω		11		ns
t _r	Turn-On Rise Time			10		ns
t _{D(off)}	Turn-Off DelayTime			38		ns
t _f	Turn-Off Fall Time			11		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		21		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		58		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. The maximum current limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

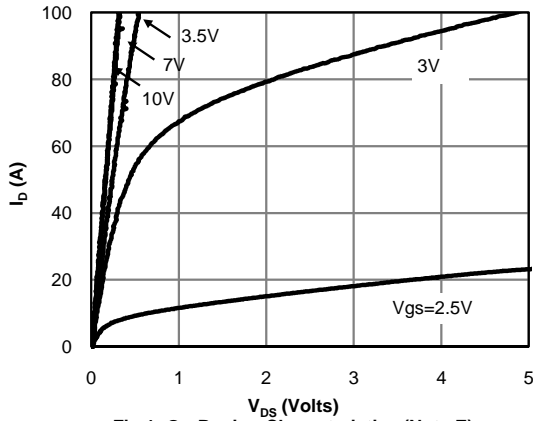


Fig 1: On-Region Characteristics (Note E)

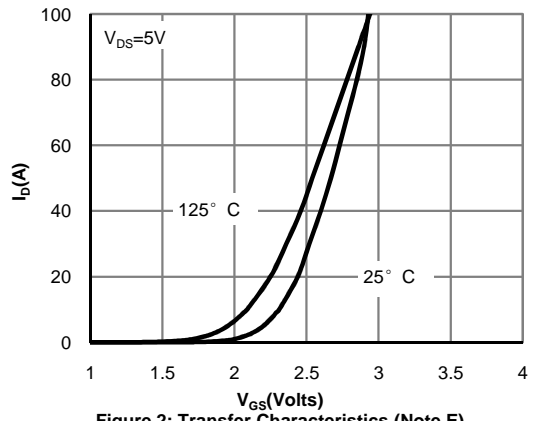


Figure 2: Transfer Characteristics (Note E)

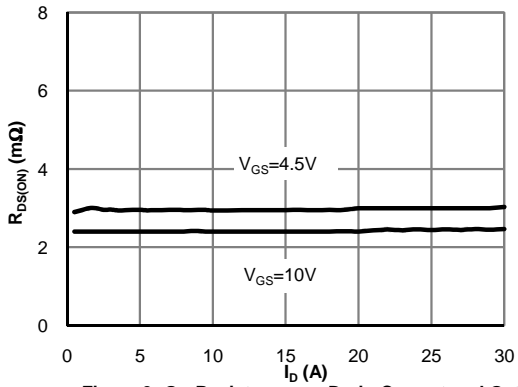


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

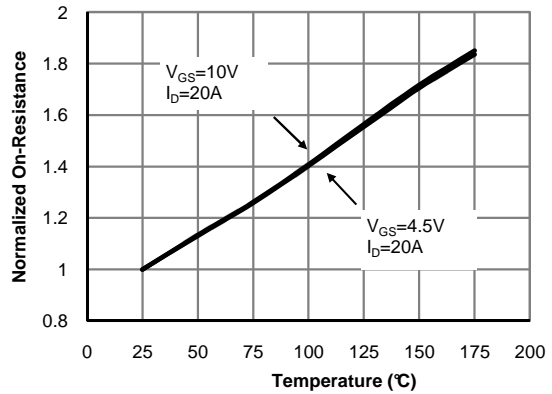


Figure 4: On-Resistance vs. Junction Temperature (Note E)

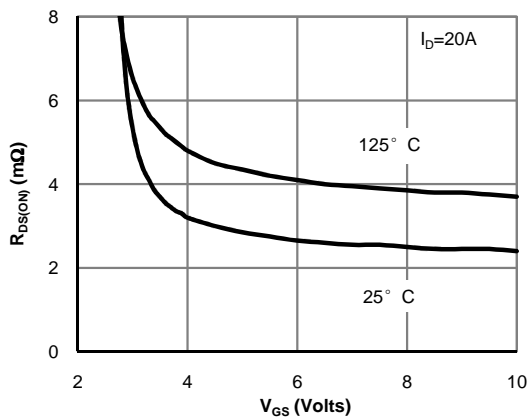


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

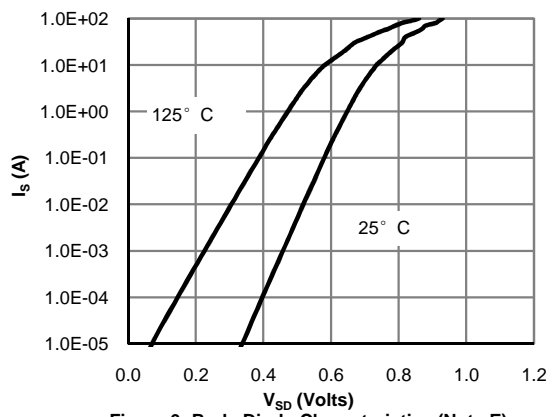


Figure 6: Body-Diode Characteristics (Note E)

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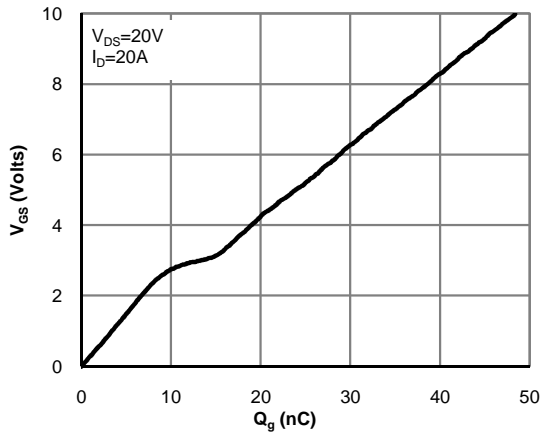


Figure 7: Gate-Charge Characteristics

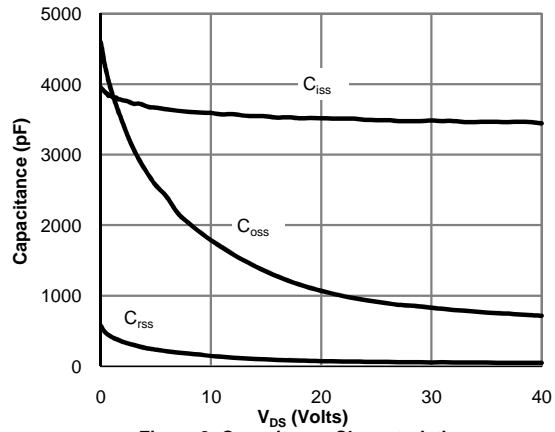


Figure 8: Capacitance Characteristics

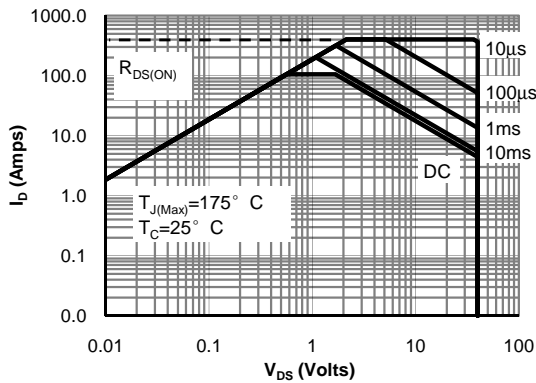


Figure 9: Maximum Forward Biased Safe Operating Area for AOT240L and AOB240L (Note F)

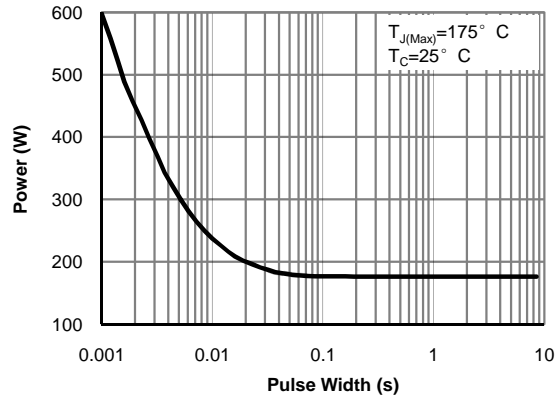


Figure 10: Single Pulse Power Rating Junction-to-Case for AOT240L and AOB240L (Note F)

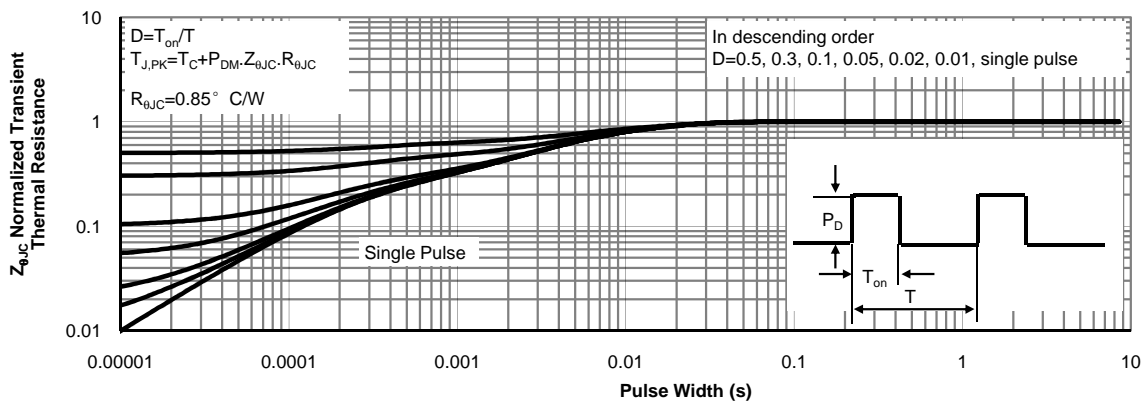


Figure 11: Normalized Maximum Transient Thermal Impedance for AOT240L and AOB240L (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

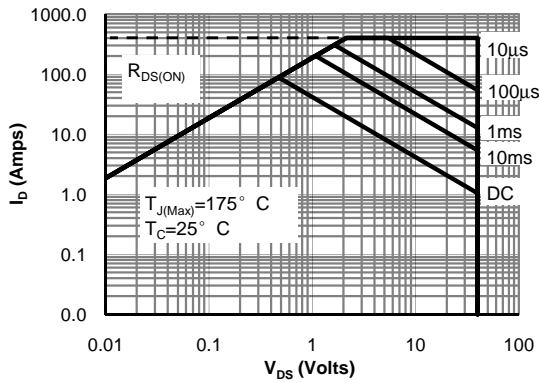


Figure 12: Maximum Forward Biased Safe Operating Area for AOTF240L

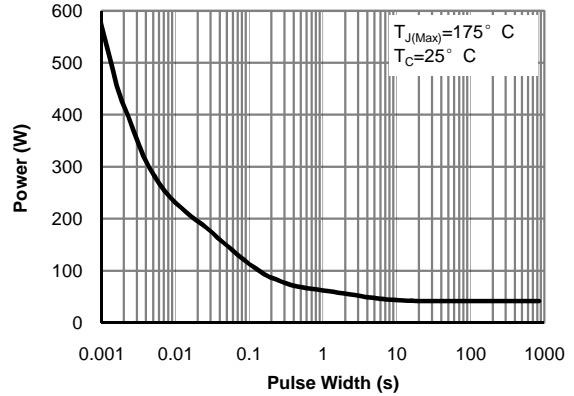


Figure 13: Single Pulse Power Rating Junction-to-Case for AOTF240L (Note F)

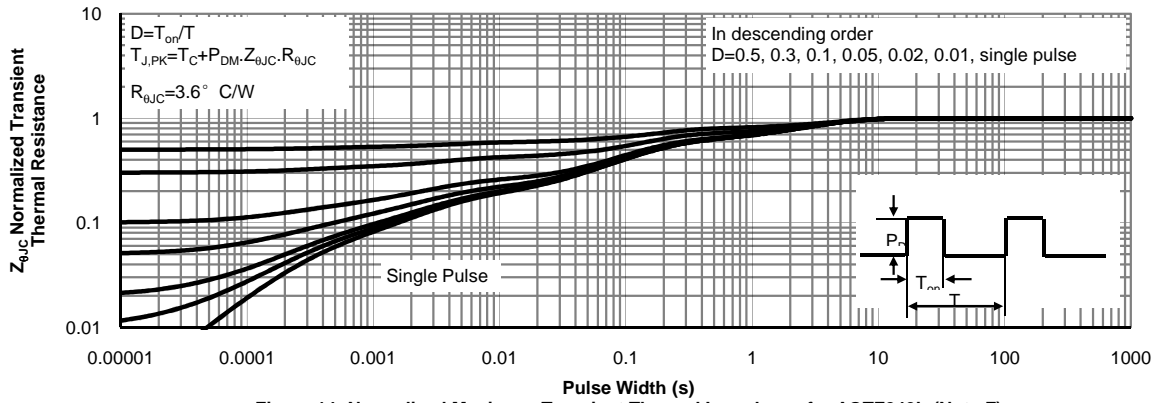


Figure 14: Normalized Maximum Transient Thermal Impedance for AOTF240L (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

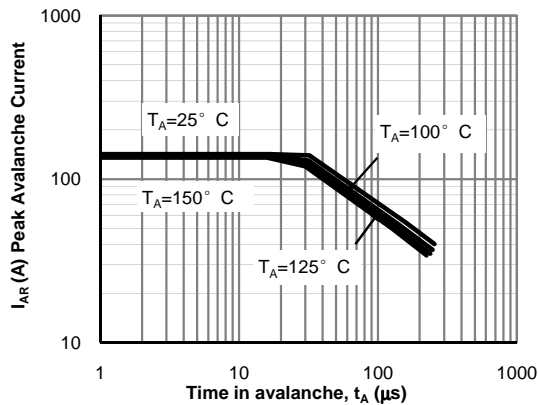


Figure 15: Single Pulse Avalanche capability (Note C)

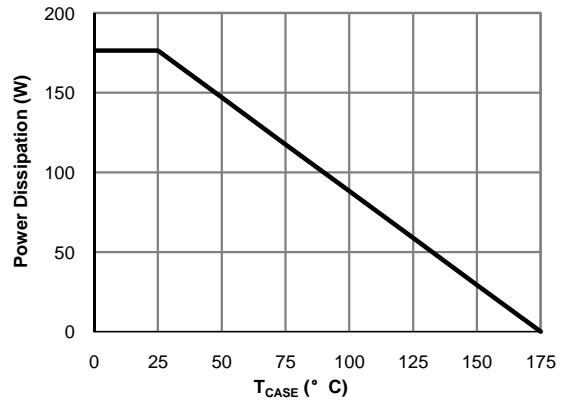


Figure 16: Power De-rating (Note F)

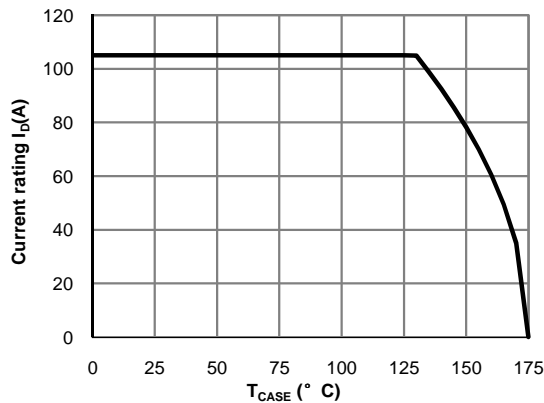


Figure 17: Current De-rating (Note F)

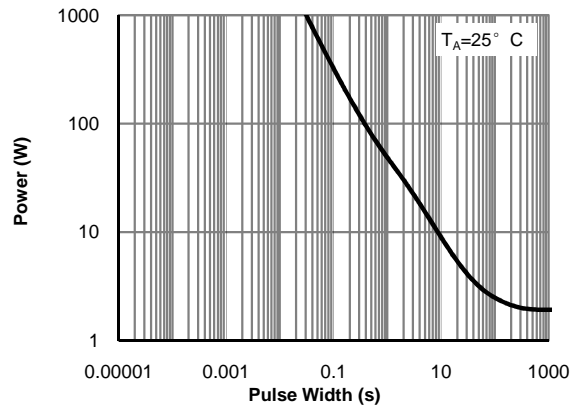


Figure 18: Single Pulse Power Rating Junction-to-Ambient (Note H)

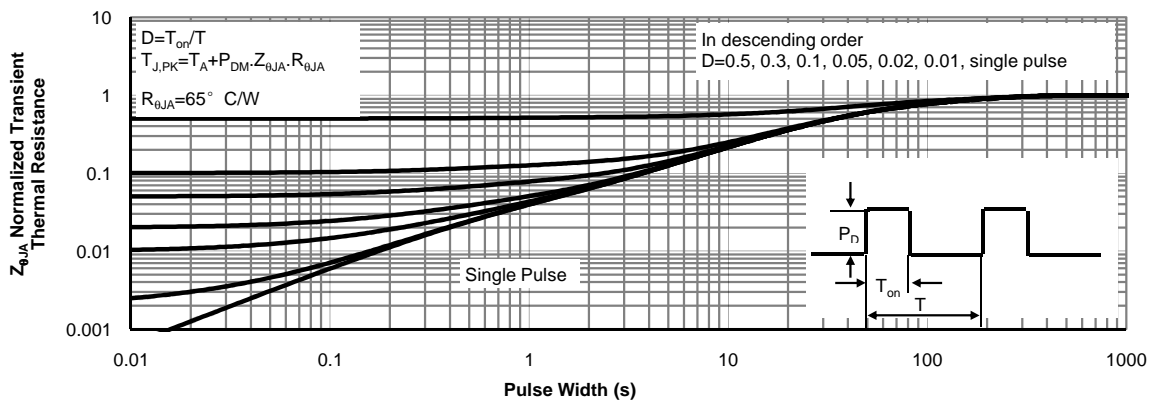
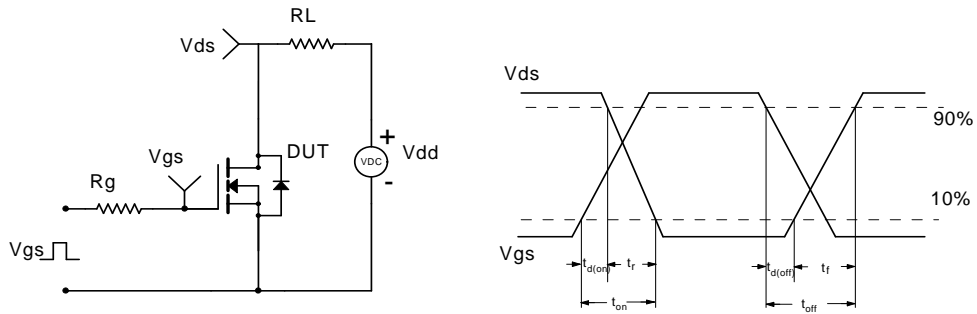


Figure 19: Normalized Maximum Transient Thermal Impedance (Note H)

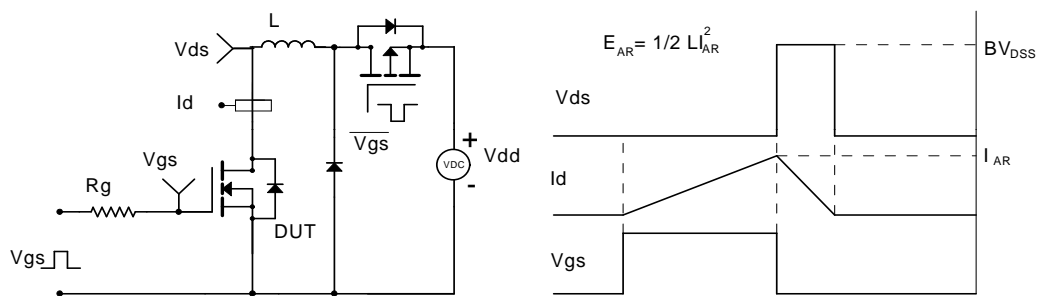
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

