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SerDes™ FIN424C / FIN425C

20-Bit Ultra-Low-Power Serializer / Deserializer for μ Controller and RGB Displays

Features

| | |
|------------------------------|--------------------------|
| Data & Control Bits | 20 |
| Frequency | 10MHz |
| Capability | QVGA |
| Interface | Microcontroller / RGB |
| μ Controller Usage | 186 & m68 |
| Selectable Edge Rates | Yes |
| Dynamic Current | 9mA / Pair |
| Standby Current | 10 μ A |
| Core Voltage ($V_{DDA/S}$) | 2.5 to 3.0V |
| I/O Voltage (V_{DDP}) | 1.6V to $V_{DDA/S}$ |
| ESD | 15KV (IEC) |
| Package | MLP-32 (5 x 5mm) |
| Ordering Information | FIN424CMLX FIN425CMLX |

Description

The FIN424C and FIN425C μ SerDes™ are a low-power serializer/ deserializer pair that can help minimize the cost and power of an LCD interface. They are designed to operate transparently between the baseband processor and LCD. /WE and chip-select timing is maintained from the serializer to the deserializer. Through the use of serialization, the number of signals transferred from one point to another can be significantly reduced. Typical reduction is 5:1. Through the use of differential signaling, shielding, and EMI filters can also be minimized, further reducing the cost of serialization. Differential signaling is important for providing a noise-insensitive signal that can withstand radio and electrical noise sources. Major reduction in power consumption allows minimal impact on battery life in mobile applications.

Applications

- Slider, Folder, and Clamshell Mobile Handsets
- GSM and CDMA Phones

Related Resources

For more information, please visit:
<http://www.fairchildsemi.com/products/interface/userdes.html>

Typical Application

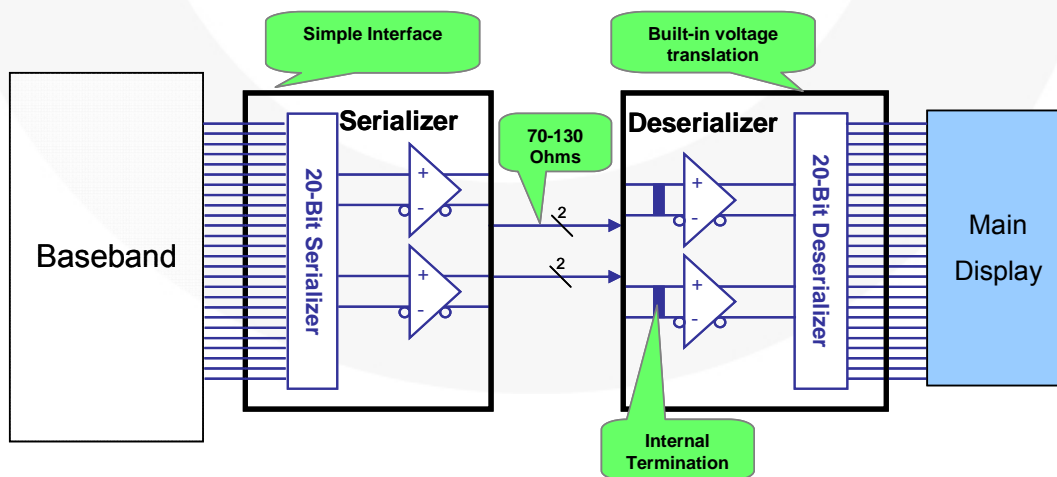


Figure 1. Mobile Phone Example

FIN424C Serializer Pin Descriptions

| Pin Name | Description | |
|------------|---|--|
| STRB | LVCMOS Strobe Signal for Latching Data into the Serializer (On Rising Edge) | |
| DP[19:0] | LVCMOS Data Input | |
| /RES | Low-Power Mode | 0 Serializer Low Power |
| | | 1 Serializer Enabled |
| /STBY | SerDes Standby | 0 Serializer and Deserializer in Low Power |
| | | 1 Serializer and Deserializer Enabled |
| Test | Internal Use (Should be GND) | |
| DS+, DS- | Serial Data Output | |
| CKS+, CKS- | Serial Clock Output | |
| VDDP | Power Supply for Parallel I/O and Internal Circuitry | |
| VDDS | Power Supply for Serial I/O | |
| VDDA | Power Supply for Core | |
| GND | Ground Pins | |

Notes:

- 0 = V_{IL} ; 1 = V_{IH} .
- All GND and VDDP pins must be connected to ground and VDDP, respectively.

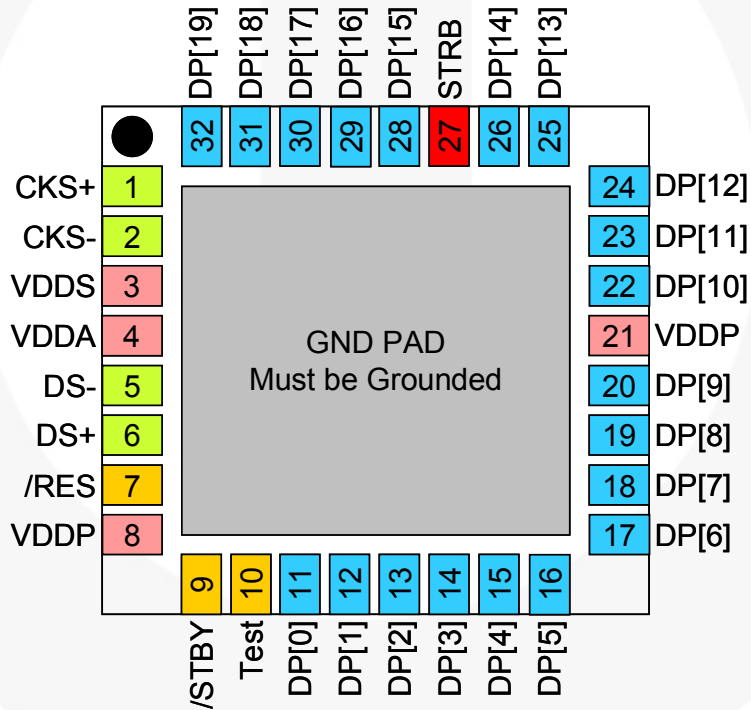


Figure 2. FIN424CMLX MLP-32 Pinout (Top Through View)

FIN425C Deserializer Pin Descriptions

| Pin Name | Description | | |
|------------|--|---|------------------------|
| WCLK | LVC MOS STRB Output | | |
| DP[19:0] | LVC MOS Data Output | | |
| /RES | Low-Power Mode | 0 | Deserializer Low Power |
| | | 1 | Deserializer Enabled |
| SLEW | Parallel Output Edge Rate Control | 0 | Slow Output Edge Rates |
| | | 1 | Fast Output Edge Rates |
| Test | Internal Use (Should be GND) | | |
| DS+, DS- | Serial Data Input | | |
| CKS+, CKS- | Serial Clock Input | | |
| VDDP | Power Supply for Parallel I/O and internal circuitry | | |
| VDDS | Power Supply for Serial I/O | | |
| VDDA | Power Supply for Core | | |
| GND | Ground Pins | | |

Notes:

- 0 = V_{IL} ; 1 = V_{IH} .
- All GND and VDDP pins must be connected to ground and VDDP, respectively.

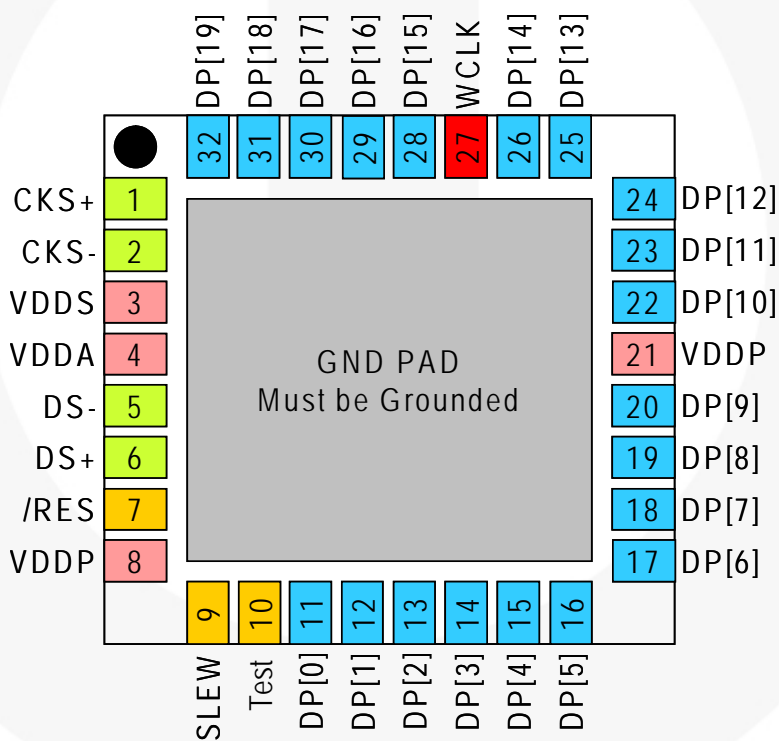


Figure 3. FIN425CMLX MLP-32 Pinout (Top Through View)

Table 1. Reset and Standby Modes / States

| /RES FIN424C FIN425C | /STBY FIN424C | Mode | Pins | FIN424C Parallel Input State | FIN425C Parallel Output State |
|----------------------------|------------------|----------------|-------------|---------------------------------|----------------------------------|
| 0 | X | Reset Mode | DP[19:0] | Disabled | LOW |
| | | | STRB / WCLK | Disabled | HIGH |
| 1 | 0 | Standby Mode | DP[19:0] | Disabled | LAST STATE |
| | | | STRB / WCLK | Disabled | HIGH |
| 1 | 1 | Operating Mode | DP[19:0] | Enabled | ENABLED |
| | | | STRB / WCLK | Enabled | ENABLED |

Application Diagram

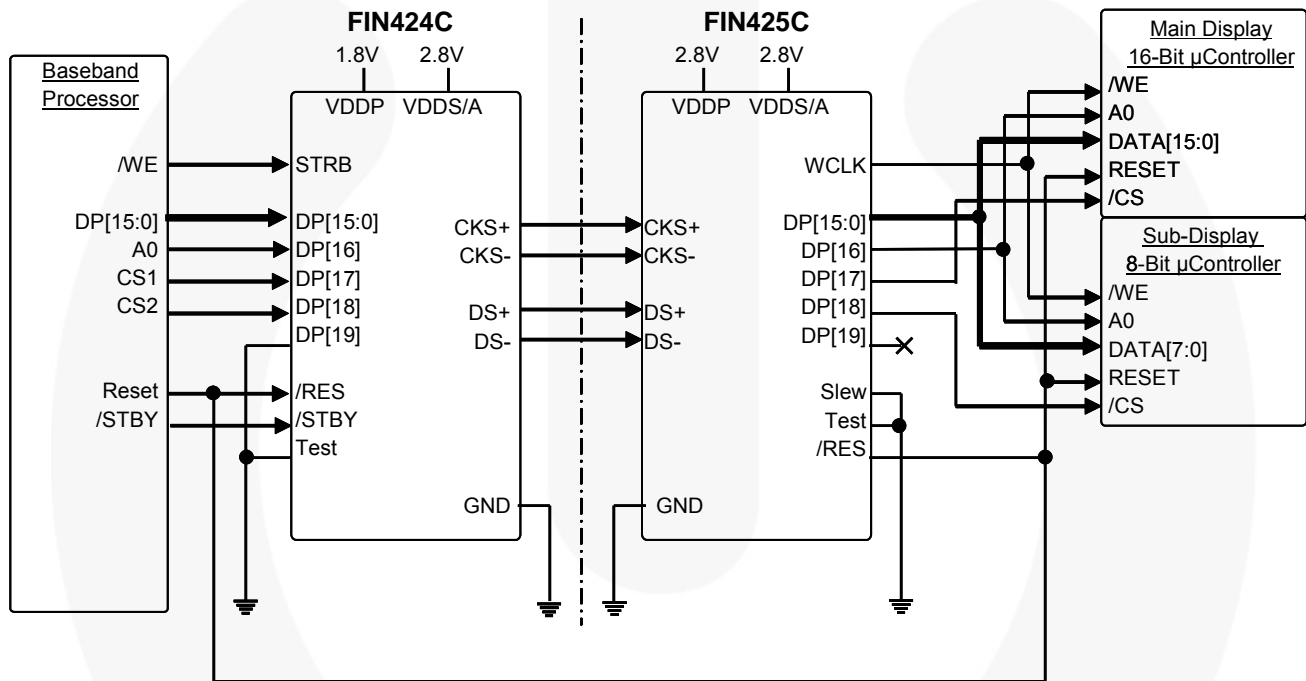


Figure 4. Dual-Display, 16-Bit, μController Interface

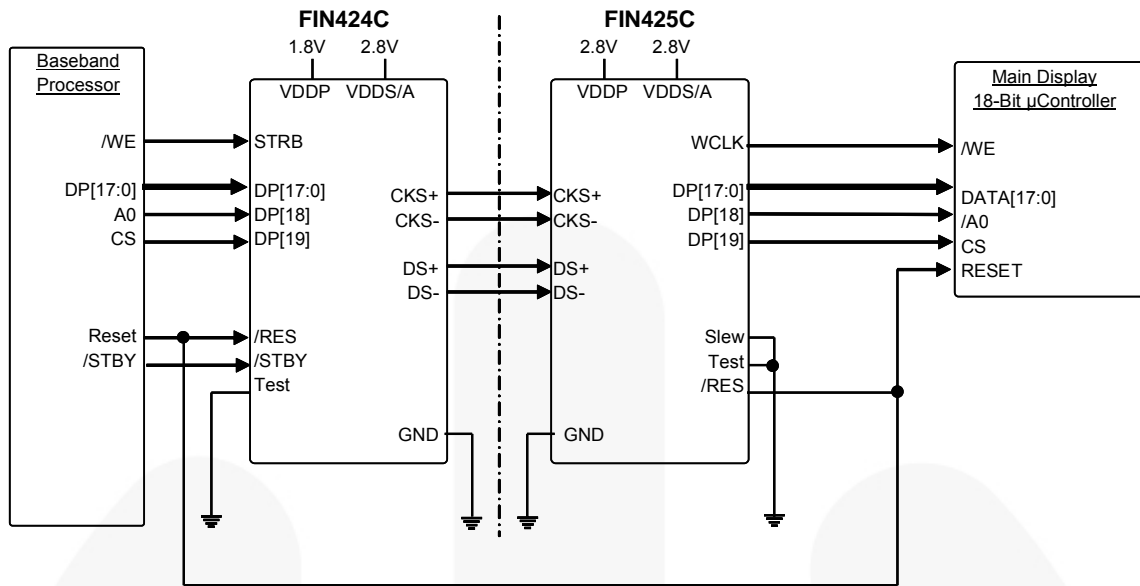


Figure 5. Single-Display, 18-Bit, μController Interface

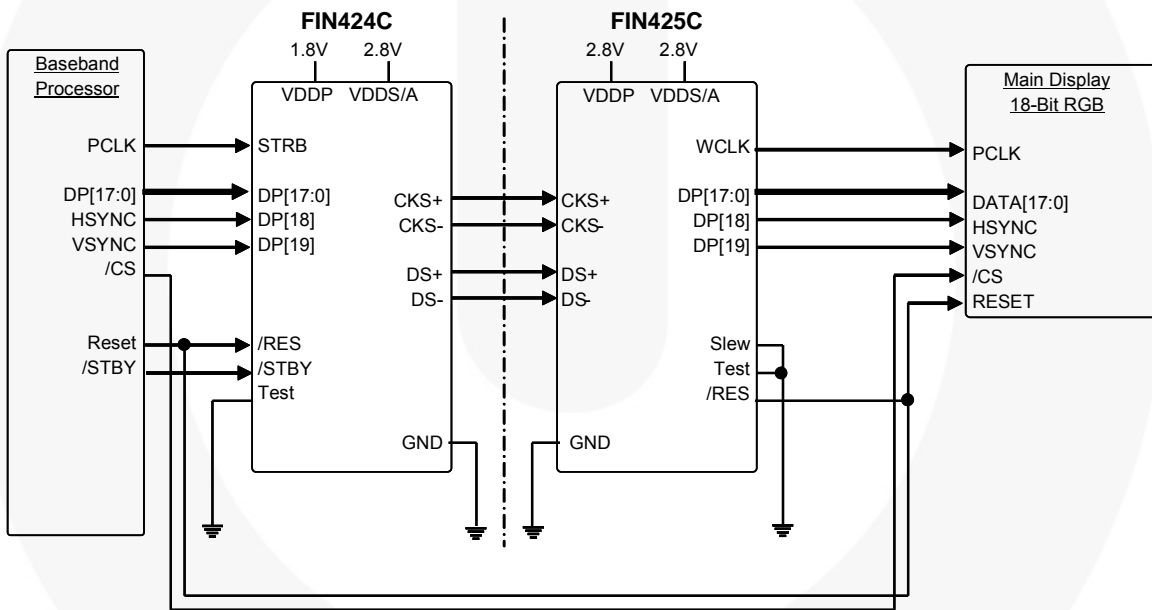


Figure 6. Single-Display, 18-Bit, RGB Interface

Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

- Keep all four differential serial wires the same length.
- Do not allow noisy signals over or near differential serial wires. Example: No CMOS traces over differential serial wires.
- Use a design goal of 70 to 130Ω differential characteristic impedance.
- Do not place test points on differential serial wires.
- Design differential serial wires a minimum of 2cm away from the antenna.
- Visit Fairchild's website at <http://www.fairchildsemi.com/products/interface/userdes.html>, contact your sales representative, or contact Fairchild directly at interface@fairchildsemi.com for applications notes or flex guidelines.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|--|----------------------------------|-----------------------|------|
| V _{DD} | Supply Voltage | -0.5 | +3.6 | V |
| V _{IO} | All Input / Output Voltage | -0.5 | V _{DDP} +0.5 | V |
| T _{STG} | Storage Temperature Range | -65 | +150 | °C |
| T _J | Maximum Junction Temperature | | +150 | °C |
| T _L | Lead Temperature (Soldering, Four Seconds) | | +260 | °C |
| ESD | IEC 61000 Board Level | | 15.0 | kV |
| | Human Body Model, JESD22-A114 | All Pins | 7.5 | |
| | | Serial I/O, /RES, PAR/SPI to GND | 14.0 | |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

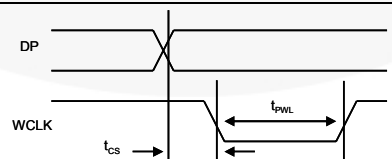
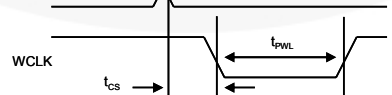
| Symbol | Parameter | Min. | Max. | Unit |
|--|-----------------------|------|--------------------|------|
| V _{DDA} , V _{DDS} ⁽⁵⁾ | Supply Voltage | 2.5 | 3.0 | V |
| V _{DDP} | Supply Voltage | 1.6 | V _{DDA/S} | V |
| T _A | Operating Temperature | -30 | +85 | °C |

Notes:

- V_{DDA} and V_{DDS} supplies must be hardwired together to the same power supply. V_{DDP} must be less than or equal to V_{DDA}/V_{DDS}.
- Typical values are tested at T_A=25°C and 2.75V.

Electrical Specifications

Values valid for over-supply voltage and operating temperature ranges unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|--|---|------------------------|------|------------------------|------|
| DC Parallel I/O and Serial Characteristics | | | | | | |
| V _{IH} | Input High Voltage | | 0.7 x V _{DDP} | | V _{DDP} | V |
| V _{IL} | Input Low Voltage | | GND | | 0.3 x V _{DDP} | V |
| V _{OH} | Output High Voltage | SLEW=0 I _{OH} =-250µA | 0.8 x V _{DDP} | | | V |
| | | SLEW=1 I _{OH} =-1mA | | | | |
| V _{OL} | Output Low Voltage | SLEW=0 I _{OL} =250µA | | | 0.2 x V _{DDP} | V |
| | | SLEW=1 I _{OL} =1mA | | | | |
| I _{IN} | Input Current | | -5 | | 5 | µA |
| V _{GO} | Serial Input Voltage Ground Offset | FIN425C to FIN424C | | 0 | | V |
| Z | Serial Transmission Line Impedance | | 70 | 100 | 130 | Ω |
| Power Characteristics | | | | | | |
| I _{DYN_FIN424C} | Dynamic Current FIN424C | V _{DDA/S} =2.75V, V _{DDP} =1.8V, /STBY=1, /RES=1 | 5.44MHz | | 4 | mA |
| I _{DYN_FIN425C} | Dynamic Current FIN425C | V _{DDA/S} =2.75V V _{DDP} =1.8V, /STBY=1, /RES=1, C _L =0pF | 5.44MHz | | 5 | mA |
| I _{BRST_FIN424C} | Burst Standby Current FIN424C | V _{DDA/S} =2.75V, V _{DDP} =1.8V, /STBY=1, /RST=1, No STROBE Signal, | | | 1.3 | mA |
| I _{BRST_FIN425C} | Burst Standby Current FIN425C | V _{DDA/S} =2.75V, V _{DDP} =1.8V, /STBY=1, /RST=1, No STROBE Signal, C _L =0pF | | | 1.8 | mA |
| I _{STBY} | Standby Current | FIN424C / FIN425C V _{DDA/S} =V _{DDP} =3.0V, /STBY=0, /RST=1 | | | 10 | µA |
| I _{RES} | Reset Current | FIN424C / FIN425C V _{DDA/S} =V _{DDP} =3.0V, /RST=0 | | | 10 | µA |
| AC FIN424C Specifications | | | | | | |
| f _{WSTRB0} | Strobe Frequency | | 0 | | 10 | MHz |
| t _R , t _F | Input Edge Rates | | | | 40 | ns |
| t _{S1} | DP Setup Time | DP Before STRBn ↑ ⁽⁷⁾ | 5 | | | ns |
| t _{H1} | DP Hold Time | DP After STRBn ↑ ⁽⁷⁾ | 15 | | | ns |
| AC FIN425C Specifications | | | | | | |
| t _{R0} , t _{F0} | Output Edge Rates of WCLK | SLEW=0, C _L =5pF 20% to 80% ⁽⁷⁾ | 8 | | 17 | ns |
| | | SLEW=1, C _L =5pF 20% to 80% ⁽⁷⁾ | | | 10 | |
| t _{R1} , t _{F1} | Output Edge Rates of DP[19:0] | SLEW=0, C _L =5pF 20% to 80% ⁽⁷⁾ | 8 | | 22 | ns |
| | | SLEW=1, C _L =5pF 20% to 80% ⁽⁷⁾ | | | 17 | |
| t _{CS} | DP[19:0] to Falling edge of WCLK C _L =5pF 20% to 80% |  | 0 | 4 | | |
| t _{PWL} | WCLK Output Pulse Width Low, Measured 30% to 30% ⁽⁷⁾ |  | 50 | 56 | | ns |
| AC Oscillator Specifications | | | | | | |
| f _{OSC} | Serial Operating Frequency | | 240 | 275 | 310 | MHz |
| t _{OSC-STBY} | Oscillator Stabilization Time After Standby | V _{DDA} =V _{DDS} =2.75V /RES=1, /STBY ↑ Transition | | 15 | 30 | µs |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|------------------------------------|---|--|-----------|------|-----------|---------|
| $t_{OSC-RES}$ | Oscillator Stabilization Time After Reset | $V_{DDA}=V_{DDs}=2.75V$ $/STBY=1, /RES \uparrow$ Transition | | 30 | 50 | μs |
| AC Reset and Standby Timing | | | | | | |
| $t_{STRB-RES}$ | $/RES$ after last $STRBn \uparrow$ | | 0 | | | ns |
| $t_{STRB-STBY}$ | Standby Time After Last Strobe | | 200 | | | ns |
| $t_{VDD-SKEW}$ | Allowed Power up Skew between V_{DDP} and $V_{DDA/S}$ | | $-\infty$ | | $+\infty$ | ms |
| $t_{VDD-RES}$ | Minimum Reset Low Time After V_{DD} Stable | | 20 | | | μs |
| $t_{RES-STBY}$ | $/STBY$ Wait Time After $/RES \uparrow$ | | 20 | | | μs |

Note:

7. Characterized, but not production tested.

Physical Dimensions

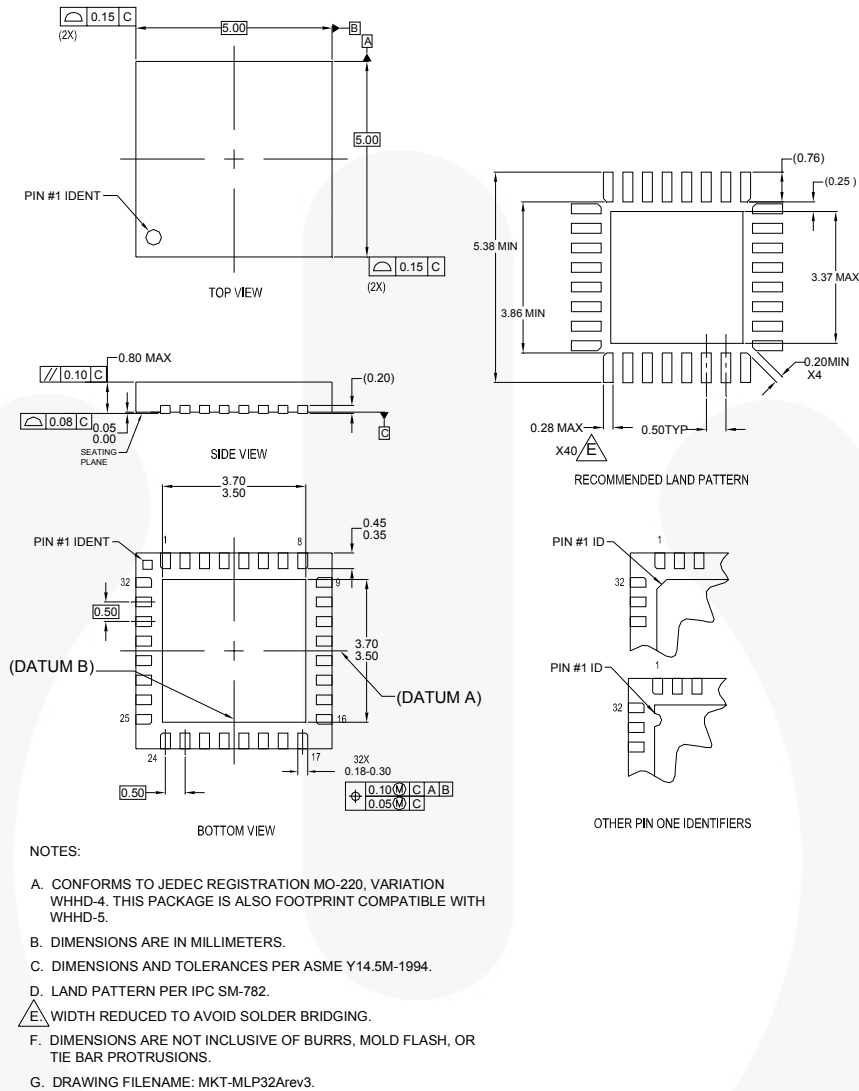


Figure 7. 32-Lead, Molded Leadless Package (MLP), QUAD, JEDEC MO-220, Variation WHHD-4, 5mm Square

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<http://www.fairchildsemi.com/packaging/>

Ordering Information

| Part Number | Operating Temperature Range | Eco Status | Package | Packing Method |
|-------------|-----------------------------|------------|--|----------------|
| FIN424CMLX | -30 to +85°C | Green | 32-Lead, Molded Leadless Package (MLP), QUAD, JEDEC MO-220, Variation WHHD-4, 5mm Square | Tape and Reel |
| FIN425CMLX | -30 to +85°C | Green | 32-Lead, Molded Leadless Package (MLP), QUAD, JEDEC MO-220, Variation WHHD-4, 5mm Square | Tape and Reel |

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| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
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