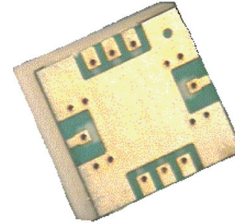
AMMP-6408

6 to 18 GHz 1 W Power Amplifier in SMT Package

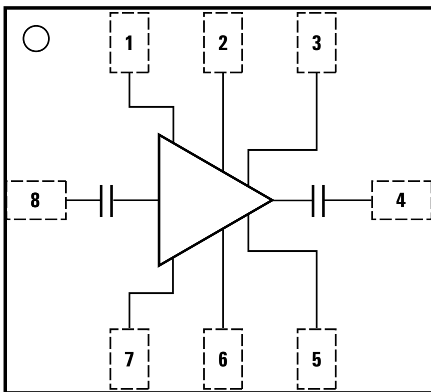
Data Sheet



Description

The AMMP-6408 MMIC is a broadband 1W power amplifier in a surface mount package designed for use in transmitters that operate in various frequency bands between 6 GHz and 18 GHz. At 8 GHz, it provides 29 dBm of output power (P-1dB) and 20 dB of small-signal gain from a small easy-to-use device. This MMIC optimized for linear operation with an output third order intercept point (OIP3) of 38 dBm.

Pin Connections (Top View)



PIN	FUNCTION
1	Vgg
2	Vdd
3	DET_O
4	RF_out
5	DER_R
6	Vdd
7	Vgg
8	RF_in

PACKAGE BASE GND

Features

- 5 x 5 mm Surface Mount Package
- Wide frequency range 6-18 GHz
- Highly linear: OIP3 = 38 dBm
- Integrated RF power detector
- ESD protection (50 V MM, and 250 V HBM)
- Input port partially matched
  (For narrowband applications, customer may obtain optimum matching and gain with an additional matching circuit.)

Specifications (Vd = 5 V, Idsq = 650 mA)

- Frequency range 6 to 18 GHz
- Small signal gain of 18 dB
- Return loss: input: -3 dB, Output: -9 dB
- High Power: @ 8 GHz, P-1dB = 29 dBm

Application

- Microwave radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband wireless access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 1A)
Refer to Avago Technologies Application Note A004R: Electrostatic Discharge, Damage and Control.

Note: This MMIC uses depletion mode pHEMT devices.
Negative supply is used for the DC gate biasing.

Absolute Maximum Ratings[1]

Symbol	Parameters[1]	Units	Value	Notes
V_d	Positive Supply Voltage	V	6	note 2
V_g	Gate Supply Voltage	V	-3 to 0.5	
I_d	Drain Current	mA	900	
P_D	Power Dissipation	W	4.6	note 2,3
P_{in}	CW Input Power	dBm	23	note 2
$T_{ch, max}$	Maximum Operating Channel Temperature	°C	+155	note 4,5
T_{stg}	Storage Case Temperature	°C	-65 to +155	
T_{max}	Maximum Assembly Temp (20 sec. max.)	°C	+260	

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Combinations of supply voltage, drain current, input power, and output power shall not exceed PD.
3. When operating at this condition with a base plate temperature of 85°C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET.
5. Junction operating temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

DC Specifications/Physical Properties

Symbol	Parameters and Test Conditions	Units	Value
I_d	Drain Supply Current (V_d = 5 V, V_g set for I_d Typical)	mA	650
V_g	Gate Supply Operating Voltage ($I_{d(Q)}$ = 650 (mA))	V	-1.1
$R_{\theta jc}$	Thermal Resistance[6] (Channel-to-Base Plate)	°C/W	20
T_{ch}	Channel Temperature	°C	150.6

Note:
6. Assume SnPb soldering to an evaluation RF board at 80°C base plate temperatures. Worst case for the channel temperature is under the quiescent operation. At saturated output power, DC power consumption rises to 4.26 W with 1.14 W RF power delivered to load. Power dissipation is 3.11 W and the temperature rise in the channel is 68.4°C. In this condition, the base plate temperature must be remained below 86.6°C to maintain maximum operating channel temperature below 155°C.

RF Specifications[1,2,3,4]

T_A = 25°C, V_d = 5 V, $Id_{(Q)}$ = 650 mA, Z_o = 50 Ω

Symbol	Parameters and Test Conditions	Units	Minimum	Typical	Maximum
Freq.	Operational Frequency	GHz	6		18
Gain	Small-Signal Gain S21[3,4]	dB	17.5 (@ Freq = 8 GHz) 15.5 (@ Freq = 17 GHz)	18	
P_{-1dB}	Output Power at 1 dB[3] Gain Compression[2]	dBm	28 (@ Freq = 8 GHz) 27 (@ Freq = 17 GHz)	28.5	
P_{-3dB}	Output Power at 3 dB Gain Compression[3]	dBm		29.5	
OIP_3	Third Order Intercept Point; Δf = 100 MHz; Pin = -20 dBm	dBm		38	
RLin	Input Return Loss[2]	dB		3	
RLout	Output Return Loss[2]	dB		9	
Isolation	Reverse Isolation	dB		45	

Notes:
1. Small/large-signal data measured in packaged form on a 2.4 mm connecter based evaluation board at T_A = 25°C.
2. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies.
3. Specifications are derived from measurements in a 50 Ω test environment. Aspects of the amplifier performance may be improved over a narrower bandwidth by application of additional conjugate, linearity, or power matching.
4. Preassembly into package performance verified 100% on-wafer published specifications at frequencies = 7, 12, and 17 GHz.

Typical Performances

(Data Obtained from 3.5-mm Connector Based Test Fixture, and This Data is Including Connecter Loss, and Board Loss.)

(T_A = 25°C, V_d = 5 V, I_D = 650 mA, Z_{in} = Z_{out} = 50 Ω)

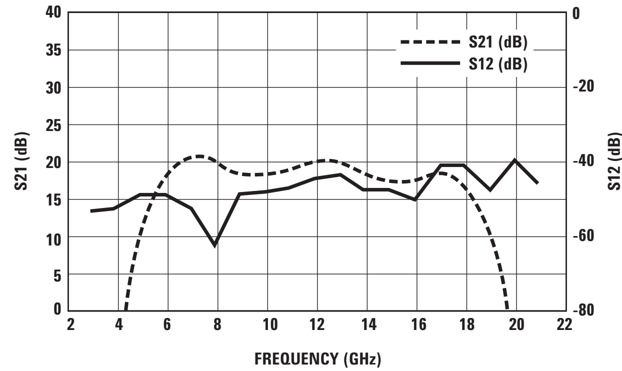


Figure 1. Typical gain and reverse isolation

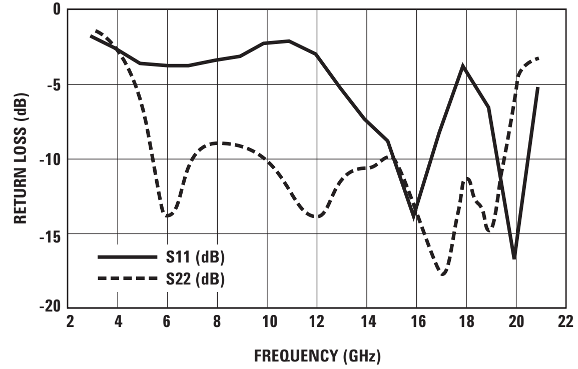


Figure 2. Typical return loss (input and output)

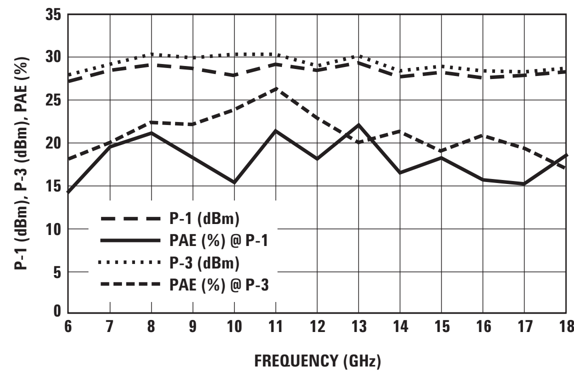


Figure 3. Typical output power (@P-1, P-3) and PAE and frequency

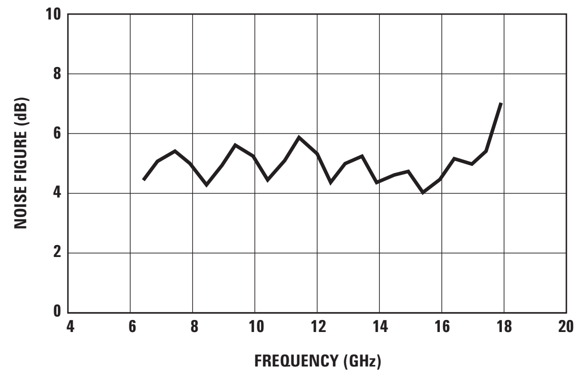


Figure 4. Typical noise figure

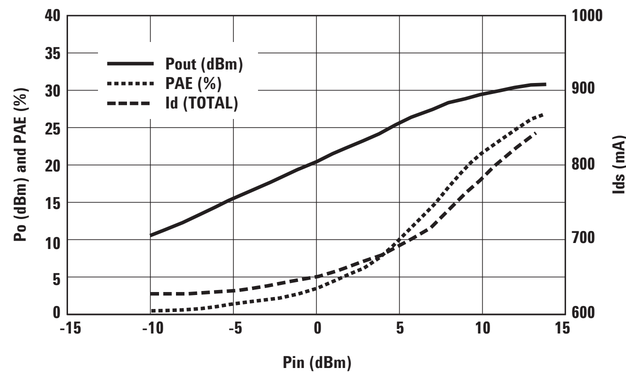


Figure 5. Typical output power, PAE, and total drain current versus input power at 8 GHz

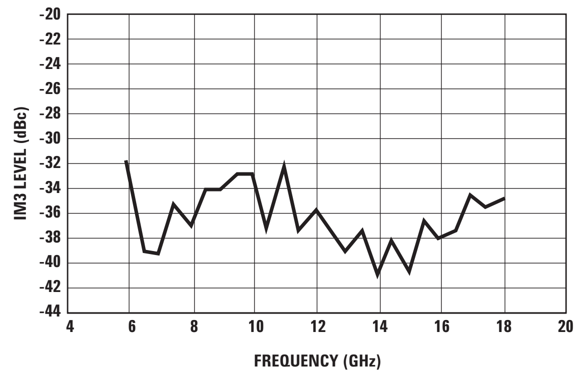


Figure 6. Typical IM3 level vs. frequency at +20 dBm output single carrier level (SCL)

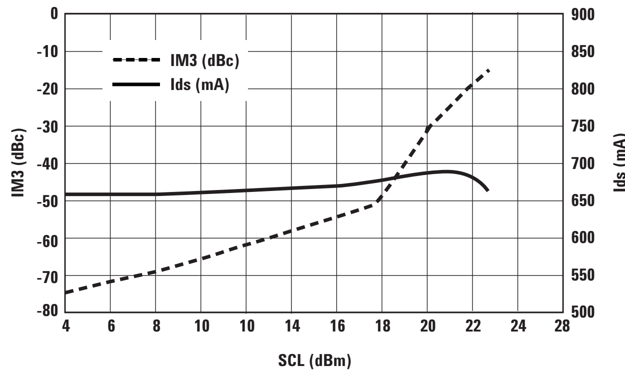


Figure 7. Typical IM3 level and Ids vs. single carrier output level at 6 GHz

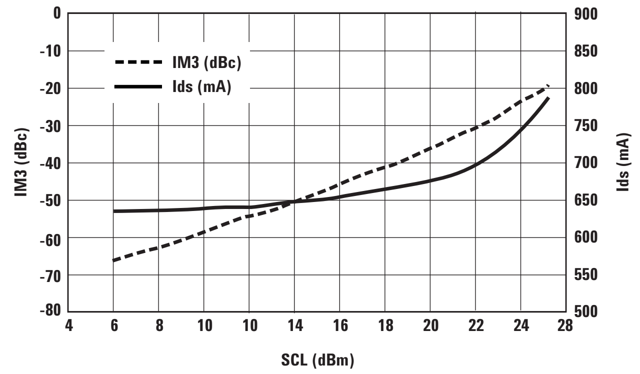


Figure 8. Typical IM3 level and Ids vs. single carrier output level at 8 GHz

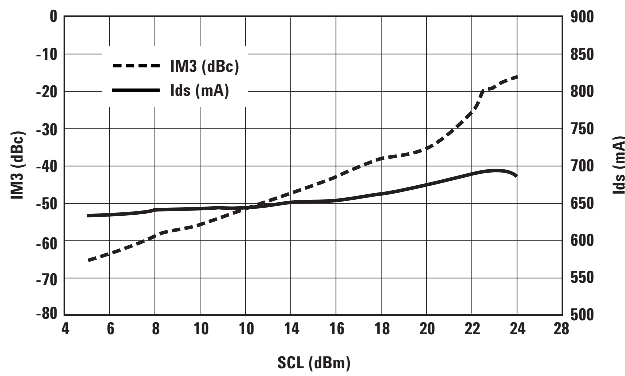


Figure 9. Typical IM3 level and Ids vs. single carrier output level at 12 GHz

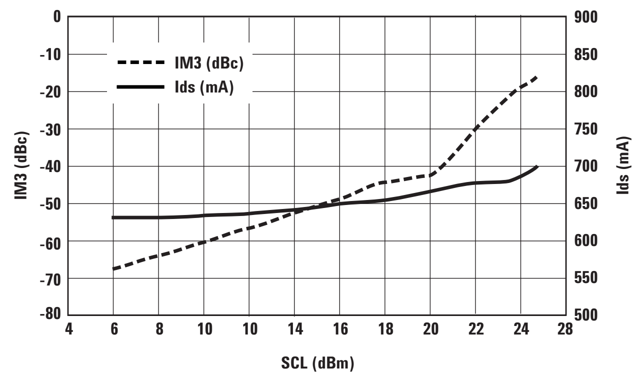


Figure 10. Typical IM3 level and Ids vs. single carrier output level at 14 GHz

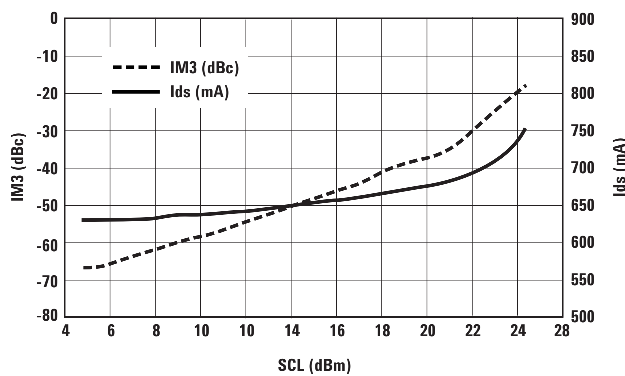


Figure 11. Typical IM3 level and Ids vs. single carrier output level at 16 GHz

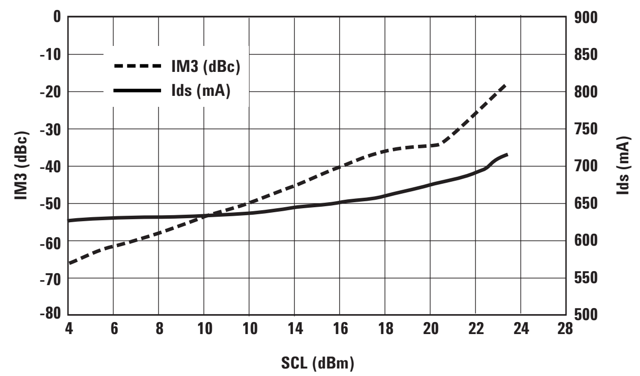


Figure 12. Typical IM3 level and Ids vs. single carrier output level at 18 GHz

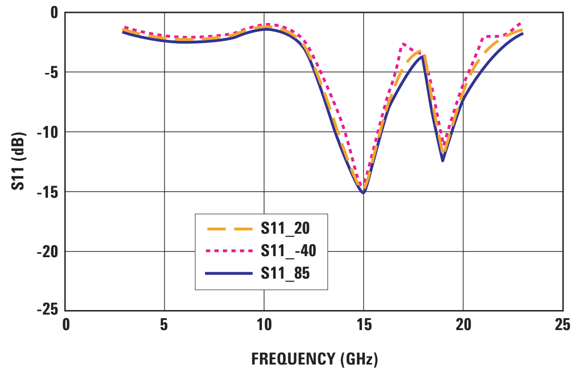


Figure 13. Typical S11 over temperature

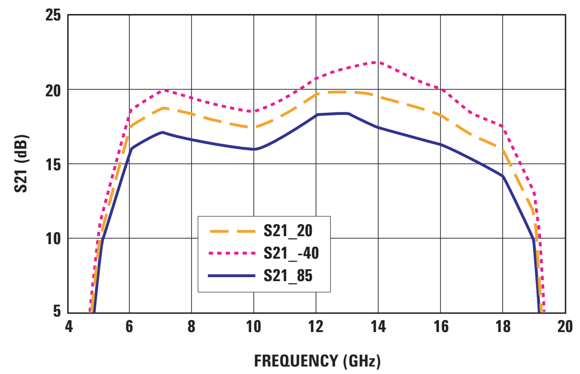


Figure 14. Typical gain over temperature

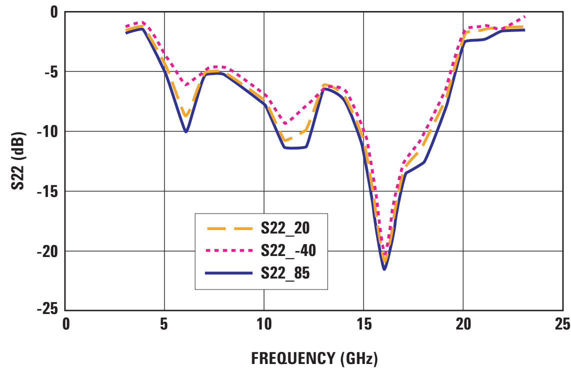


Figure 15. Typical S22 over temperature

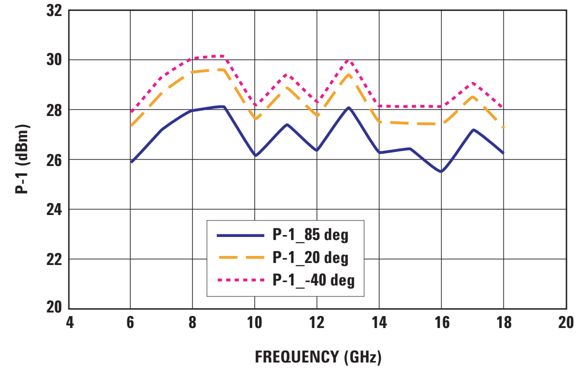


Figure 16. Typical P-1 over temperature

Typical Scattering Parameters [1], (T_A = 25°C, Vd =5 V, I_D = 650 mA, Z_{in} = Z_{out} = 50 Ω)

Freq		**S11**			**S21**			**S12**			**S22**	
[GHz]	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**
6	-3.83	0.64	-7.36	18.46	8.37	-45.38	-49.36	3.41E-03	59.85	-9.89	0.32	-112.35
7	-4.33	0.61	-37.59	22.06	12.67	-160.68	-47.90	4.03E-03	-10.90	-24.54	0.06	-97.72
8	-4.35	0.61	-57.25	21.82	12.33	105.82	-55.02	1.78E-03	-87.02	-12.59	0.23	-116.00
9	-2.87	0.72	-67.80	20.57	10.67	30.27	-58.31	1.21E-03	155.08	-11.66	0.26	-123.36
10	-2.18	0.78	-81.97	19.45	9.38	-34.10	-56.32	1.53E-03	87.15	-9.47	0.34	-111.81
11	-1.88	0.81	-99.66	19.28	9.21	-91.39	-50.78	2.89E-03	36.92	-8.10	0.39	-107.66
12	-2.85	0.72	-125.26	20.24	10.27	-154.70	-48.77	3.64E-03	5.73	-8.11	0.39	-96.60
13	-5.02	0.56	-151.04	20.41	10.49	130.30	-45.72	5.17E-03	-42.89	-5.74	0.52	-95.19
14	-6.38	0.48	-177.19	19.28	9.20	56.72	-45.56	5.27E-03	-90.74	-5.64	0.52	-116.87
15	-6.79	0.46	167.29	18.74	8.65	-8.92	-46.62	4.67E-03	-134.99	-6.02	0.50	-158.25
16	-8.64	0.37	129.42	19.07	8.98	-83.27	-47.25	4.34E-03	-179.47	-8.44	0.38	163.63
17	-14.40	0.19	34.52	19.99	9.99	-174.68	-45.92	5.06E-03	31.89	-12.65	0.23	142.26
18	-4.82	0.57	-87.84	18.06	7.99	61.47	-42.49	7.50E-03	-86.04	-12.88	0.23	-156.34
19	-3.86	0.64	-142.34	9.17	2.88	-58.13	-50.94	2.84E-03	-115.71	-5.42	0.54	127.81
20	-19.84	0.10	171.38	-6.42	0.48	-160.84	-39.18	1.10E-02	-92.64	-6.15	0.49	-6.31
21	-4.51	0.60	-70.79	-16.88	0.14	-164.95	-42.22	7.74E-03	-168.17	-2.48	0.75	-89.99
22	-1.76	0.82	-104.56	-24.20	0.06	137.84	-64.23	6.15E-04	172.50	-1.13	0.88	-122.31
23	-1.30	0.86	-129.94	-33.63	0.02	69.70	-46.41	4.78E-03	-96.28	-1.28	0.86	-144.94
24	-1.04	0.89	-159.31	-42.07	0.01	-90.70	-41.89	8.05E-03	-130.89	-1.01	0.89	-164.03
25	-0.57	0.94	176.91	-50.13	0.00	109.52	-50.58	2.96E-03	122.04	-0.82	0.91	173.03
26	-0.12	0.99	158.94	-44.39	0.01	-58.10	-41.20	8.71E-03	-50.18	-0.33	0.96	155.22

Note:
1. Data obtained from an ICM test fixture with TRL calibration. Reference planes were defined at RF I/O on the package.

Biasing and Operation

The recommended quiescent DC bias condition for optimum efficiency, performance, and reliability is Vdd = 5 volts with Vg set for Idd = 650 mA. Minor improvements in performance are possible depending on the application. The drain bias voltage range is 3 to 5 V. A single DC gate supply connected to Vg will bias all gain stages. Muting can be accomplished by setting Vgg to the pinch-off voltage Vp.

A simplified schematic for the AMMP6408 MMIC die is shown in Figure 17. The MMIC die contains ESD and over voltage protection diodes for Vg, Vd1, and Vd2 terminals. In a finalized package form, Vd1 and Vd2 terminals are commonly connected to the Vdd terminal. The package diagram for the recommended assembly is shown in Figure 18. In finalized package form, ESD diodes protect all possible ESD or over voltage damages between Vgg and ground, Vgg and Vdd, Vdd and ground. Typical ESD diode current versus diode voltage for 11-connected diodes in series is shown in Figure 13. Under the recommended DC quiescent biasing condition at Vds = 5 V, Ids = 650 mA, Vgg = -1 V, typical gate terminal current is approximately 0.3mA. If an active biasing technique is selected for the AMMP6408 MMIC PA DC biasing, the active biasing circuit must have more than 10-times higher internal current that the gate terminal current.

An optional output power detector network is also provided. A typical measured detector voltage versus output power at 18 GHz is shown Figure 20. The differential voltage between the Det-Ref and Det-Out pads can be correlated with the RF power emerging from the RF output port. The detected voltage is given by,

$$V = (V_{ref} - V_{det}) - V_{ofs}$$

where V_{ref} is the voltage at the *DET _R* port, V_{det} is a voltage at the *DET _O* port, and V_{ofs} is the zero-input-power offset voltage. There are three methods to calculate V_{ofs}:

1. V_{ofs} can be measured before each detectore measurement (by removing or switching off the power source and measuring $V_{ref} - V_{det}$). This method gives an error due to temperature drift of less than 0.01 dB/50°C.
2. V_{ofs} can be measured at a single reference temperature. The drift error will be less than 0.25 dB.
3. V_{ofs} can either be characterized over temperature and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate V_{ofs} at any temperature. This method gives an error close to the method #1.

The RF ports are AC coupled at the RF input to the first stage and the RF output of the final stage. No ground wired are needed since ground connections are made with plated through-holes to the backside of the device.

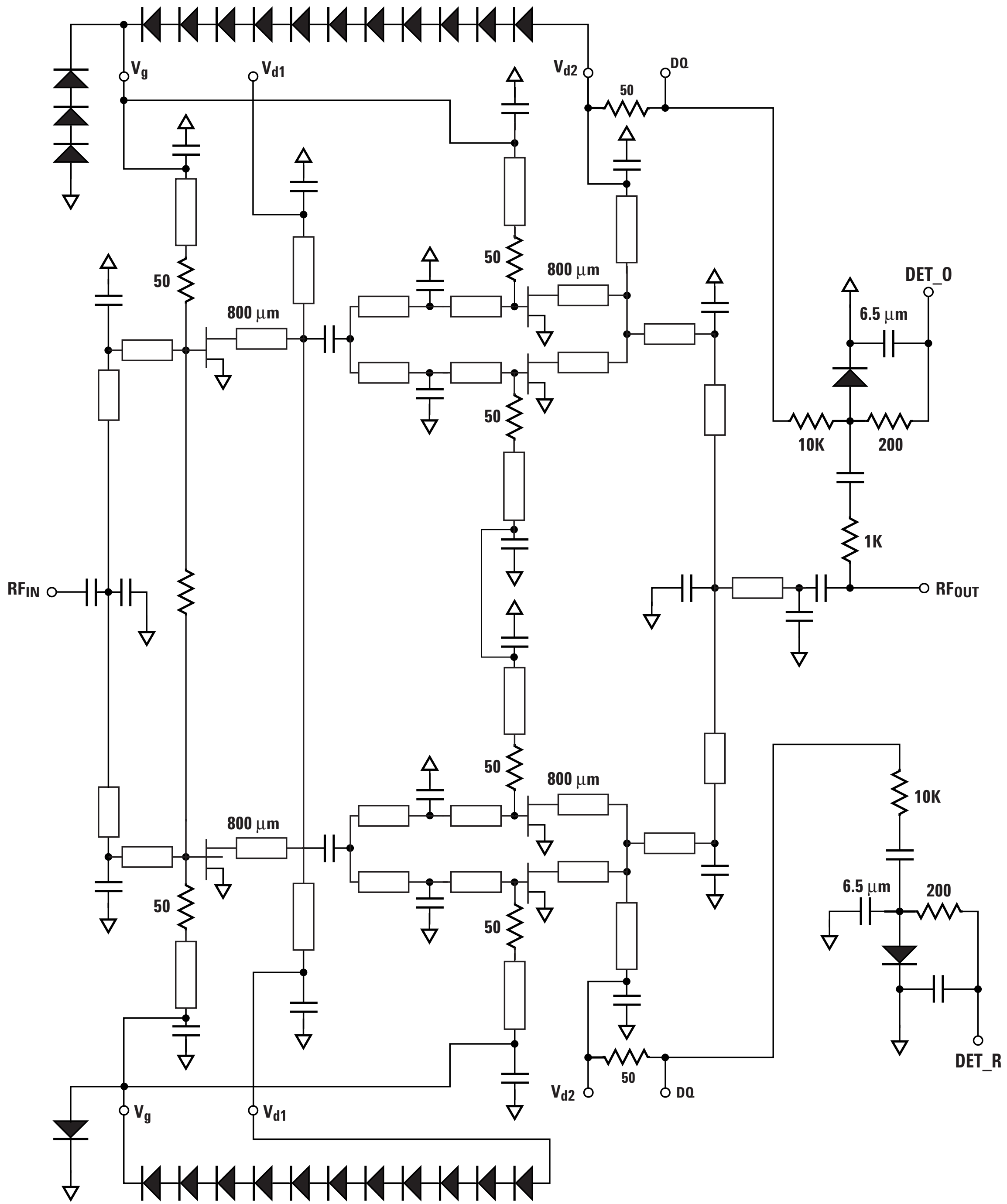
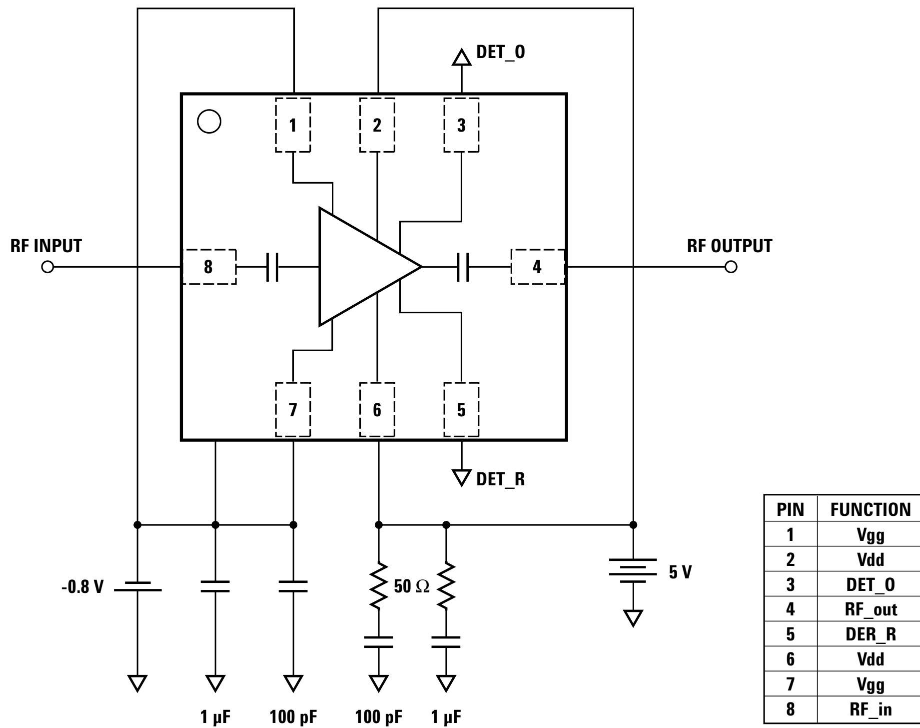


Figure 17. Simplified schematic for the MMIC die



PIN	FUNCTION
1	Vgg
2	Vdd
3	DET_O
4	RF_out
5	DER_R
6	Vdd
7	Vgg
8	RF_in

Note:
1. Vdd may be applied to either Pin 2 or Pin 6.
2. Vgg may be applied to either Pin 1 or Pin 7.

Figure 18. Schematic for recommended Bias circuitry

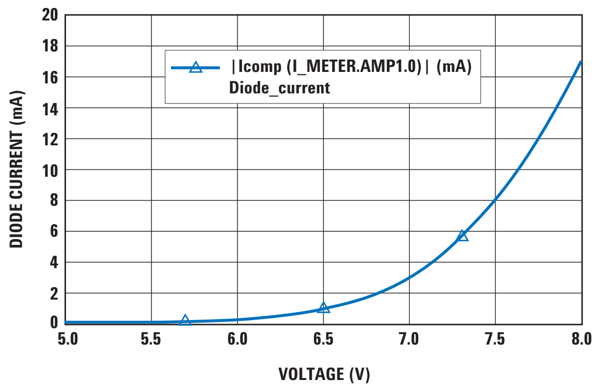


Figure 19. Typical ESD diode current versus diode voltage for 11-connected diodes in series

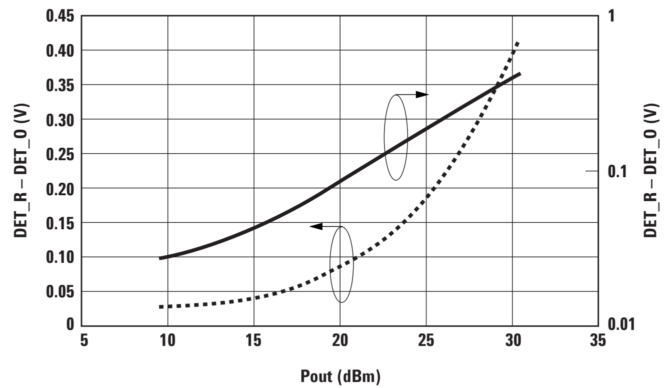


Figure 20. Typical detector voltage and output power, freq. = 18 GHz

Recommended SMT Attachment for 5x5 Package

The AMMP Packaged Devices are compatible with high volume surface mount PCB assembly processes.

The PCB material and mounting pattern, as defined in the data sheet, optimizes RF performance and is strongly recommended. An electronic drawing of the land pattern is available upon request from Avago Sales & Application Engineering.

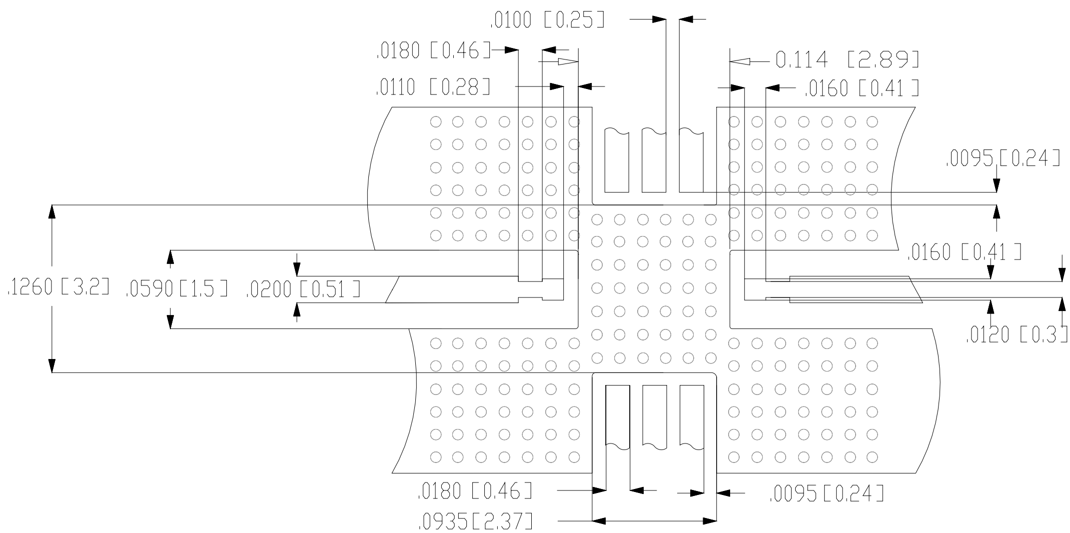


Figure 21. Suggested PCB Land Pattern and Stencil Layout

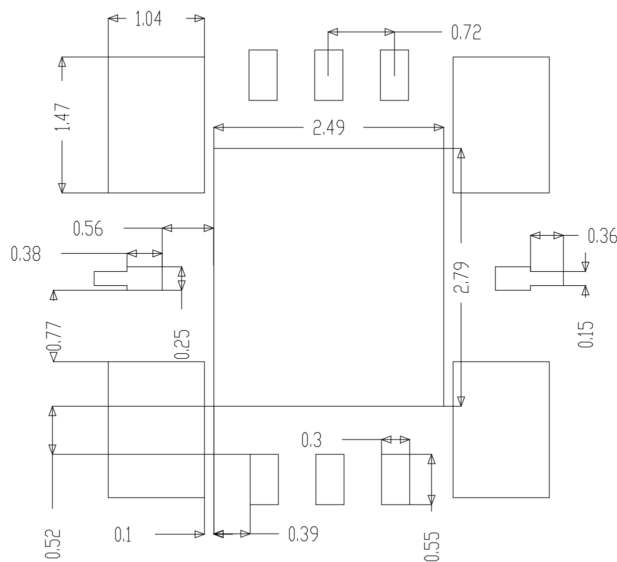


Figure 22. Stencil Outline Drawing (mm)

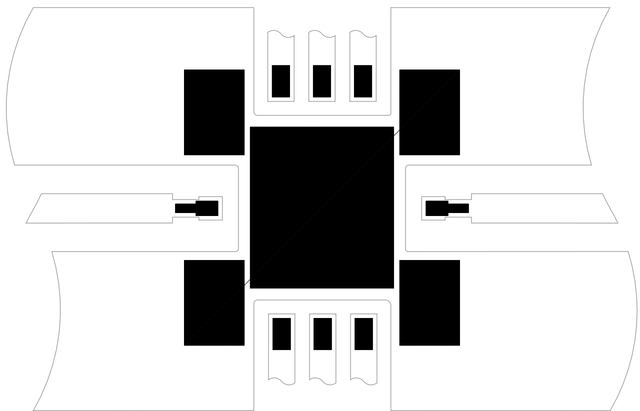


Figure 23. Combined PCB and Stencil Layouts

Manual Assembly

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers.
- Recommended attachment is conductive solder paste. Please see recommended solder reflow profile. Neither Conductive epoxy or hand soldering is recommended.
- Apply solder paste using a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance.
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp. to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 seconds. Verify that the profile will not expose device beyond these limits.

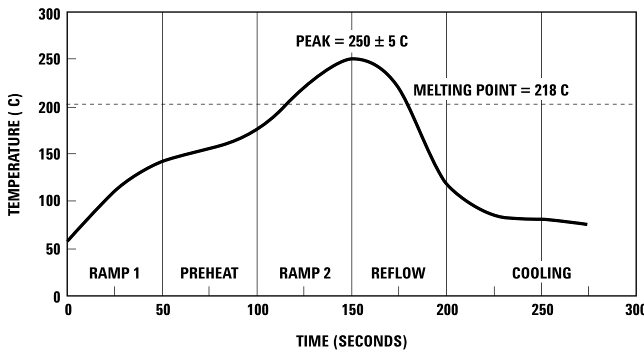


Figure 22. Suggested lead-free reflow profile for SnAgCu solder paste

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 21. The stencil has a solder paste deposition opening approximately 70% to 90% of the PCB pad. Reducing stencil opening can potentially generate more voids underneath. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use a laser cut stencil composed of 0.127 mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline.

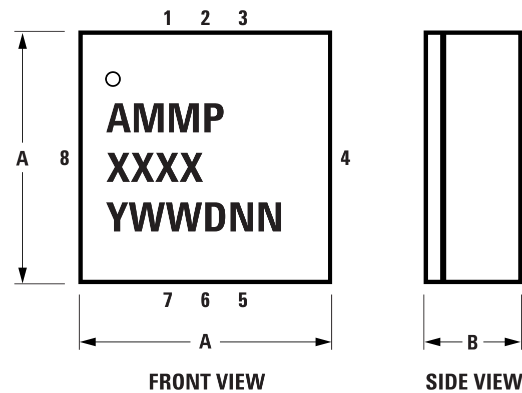
The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. The suggested reflow profile for automated reflow processes is shown in Figure 22. This profile is designed to ensure reliable finished joints. However, the profile indicated in Figure 1 will vary among different solder pastes from different manufacturers and is shown here for reference only.

Ordering Information

AMMP-6408 Part Number Ordering Information

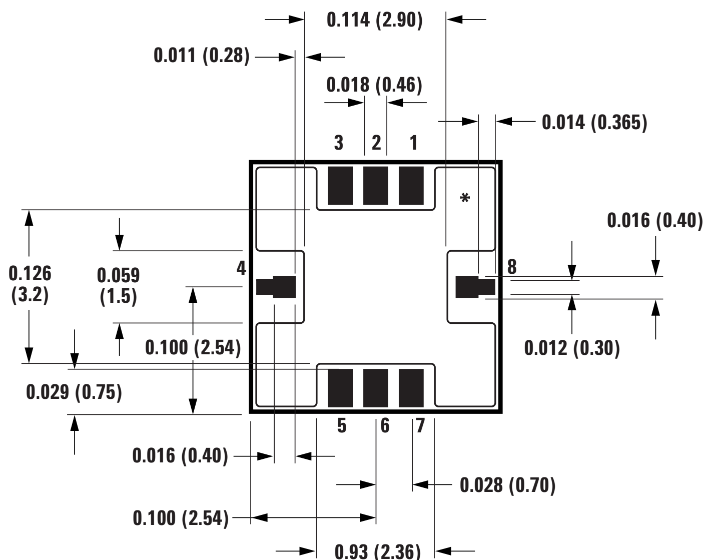
Part Number	Devices per Container	Container
AMMP-6408-BLKG	10	Antistatic bag
AMMP-6408-TR1G	100	7" Reel
AMMP-6408-TR2G	500	7" Reel

Package Dimensions

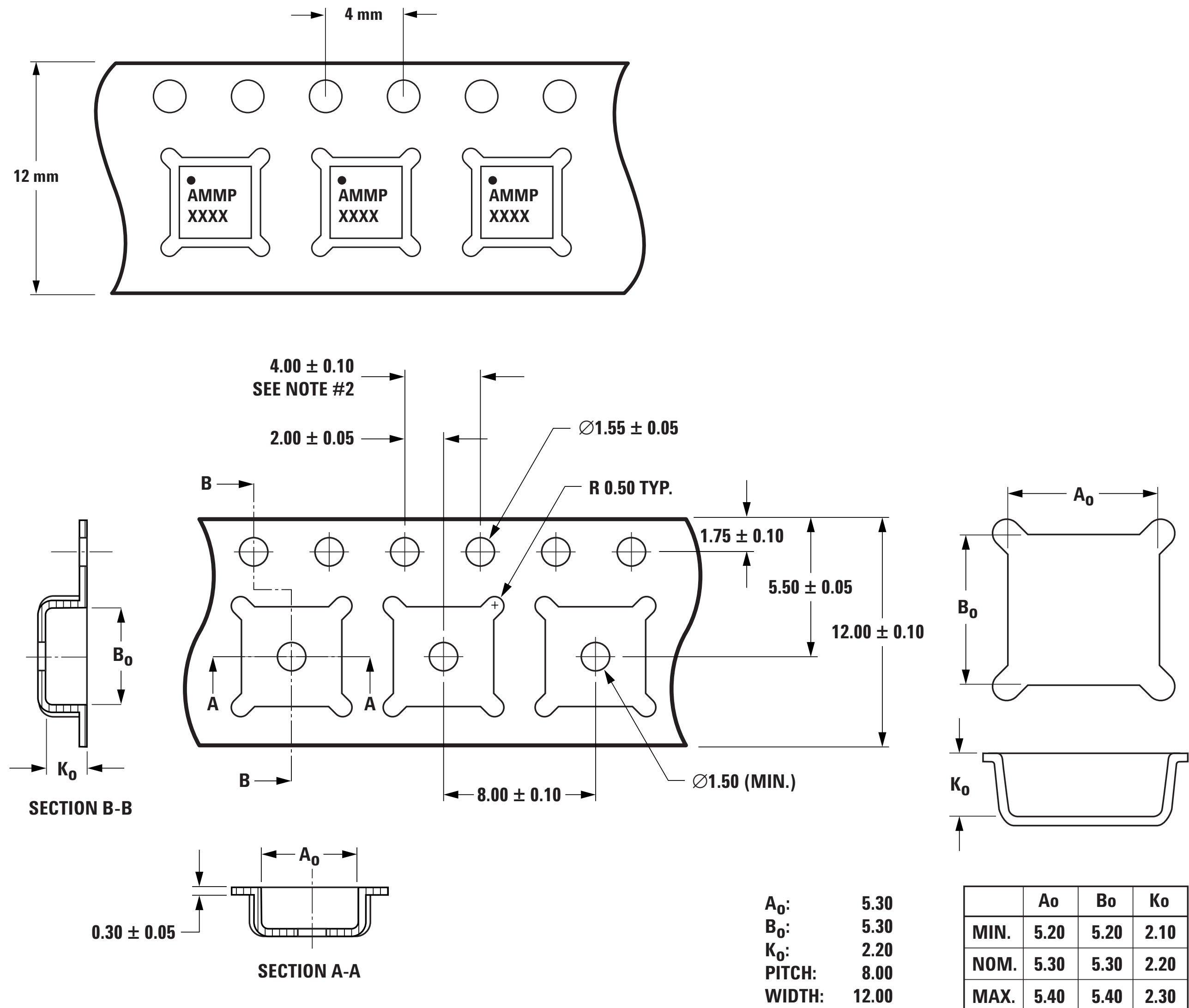


SYMBOL	MIN.	MAX.
A	0.198 (5.03)	0.213 (5.4)
B	0.0685 (1.74)	0.088 (2.25)

DIMENSIONS ARE IN INCHES (MM)



Carrier Tape and Pocket Dimensions



	Ao	Bo	Ko
MIN.	5.20	5.20	2.10
NOM.	5.30	5.30	2.20
MAX.	5.40	5.40	2.30

NOTES:

1. A_0 AND B_0 MEASURED AT 0.3 mm ABOVE BASE OF POCKET.
2. 10 PITCHES CUMULATIVE TOLERANCE IS ± 0.2 mm.
3. DIMENSIONS ARE IN MILLIMETERS (mm).

Note: No RF performance degradation is seen due to ESD up to 250 V HBM and 50 V MM. The DC characteristics in general show increased leakage at lower ESD discharge voltages. The user is reminded that this device is ESD sensitive and needs to be handled with all necessary ESD protocols.

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