4 OUTPUT PCIE GEN1/2/3 SYNTHESIZER

IDT5V41236

Recommended Applications

Four output synthesizer for PCIe Gen1/2/3

General Description

The IDT5V41236 is a PCIe Gen2/3 compliant spread-spectrum-capable clock generator. The device has 4 differential HCSL outputs and can be used in communication or embedded systems to substantially reduce electro-magnetic interference (EMI). The spread amount and output frequency are selectable via select pins.

Output Features

- 4 - 0.7V current mode differential HCSL output pairs

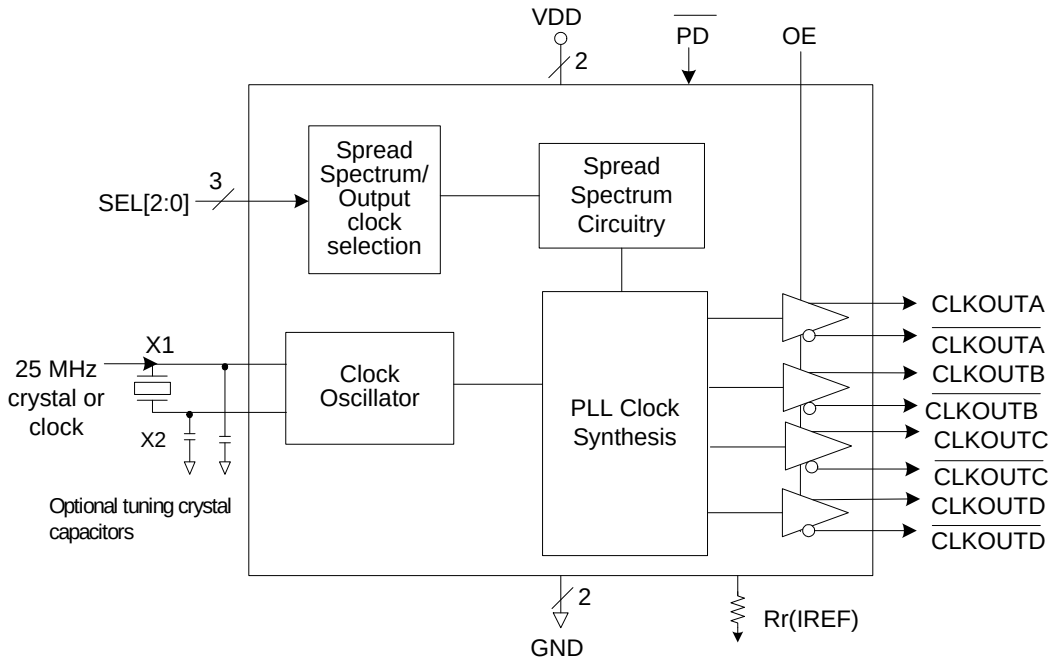
Features/Benefits

- 20-pin TSSOP/VFQFPN packages; small board footprint
- Spread-spectrum capable; reduces EMI
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- Power down pin; greater system power management
- OE control pin; greater system power management
- Spread% and frequency pin selection; no software required to configure device
- Industrial temperature range available; supports demanding embedded applications

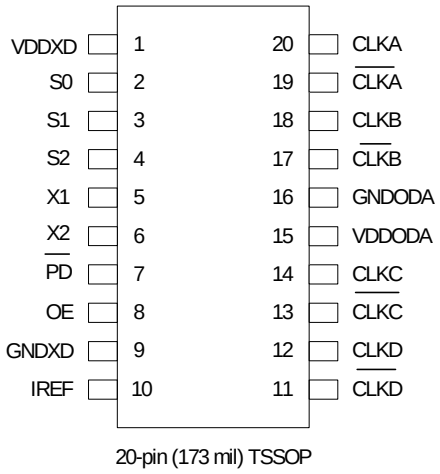
Key Specifications

- Cycle-to-cycle jitter < 100 ps
- Output-to-output skew < 50 ps
- PCIe Gen2 phase jitter < 3.0ps RMS
- PCIe Gen3 phase jitter < 1.0ps RMS

Block Diagram

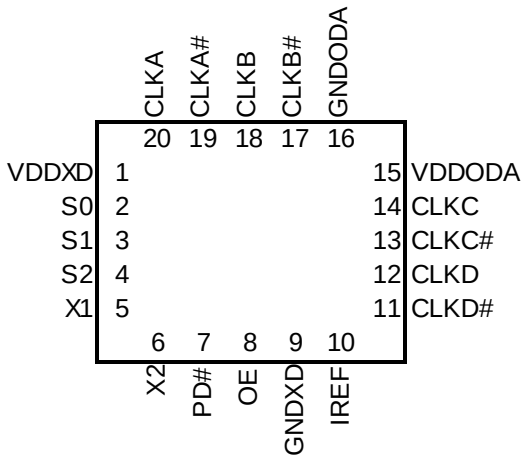


Pin Assignment (20TSSOP)



20-pin (173 mil) TSSOP

Pin Assignment (20VFQFPN)



Spread Spectrum Selection Table

S2	S1	S0	Spread%	Spread Type	Output Frequency
0	0	0	-0.5	Down	100
0	0	1	-1.0	Down	100
0	1	0	-1.5	Down	100
0	1	1	No Spread	Not Applicable	100
1	0	0	-0.5	Down	200
1	0	1	-1.0	Down	200
1	1	0	-1.5	Down	200
1	1	1	No Spread	Not Applicable	200

Pin Descriptions

Pin	Pin Name	Pin Type	Pin Description
1	VDDXD	Power	Connect to +3.3V digital supply.
2	S0	Input	Spread spectrum select pin #0. See table above. Internal pull-up resistor.
3	S1	Input	Spread spectrum select pin #1. See table above Internal pull-up resistor.
4	S2	Input	Spread spectrum select pin #2. See table above. Internal pull-up resistor.
5	X1	Input	Crystal connection. Connect to a fundamental mode crystal or clock input.
6	X2	Output	Crystal connection. Connect to a fundamental mode crystal or leave open.
7	PD#	Input	Powers down all PLLs and tri-states outputs when low. Internal pull-up resistor.
8	OE	Input	Provides output on, tri-states output (High = enable outputs; Low = disable outputs). Internal pull-up resistor.
9	GND	Power	Connect to digital ground.
10	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
11	CLKD#	Output	Selectable 100/200MHz spread spectrum differential complement output clock D.
12	CLKD	Output	Selectable 100/200MHz spread spectrum differential true output clock D.
13	CLKC#	Output	Selectable 100/200MHz spread spectrum differential complement output clock C.
14	CLKC	Output	Selectable 100/200MHz spread spectrum differential true output clock C.
15	VDDODA	Power	Connect to +3.3V analog supply.
16	GND	Power	Connect to analog ground.
17	CLKB#	Output	Selectable 100/200MHz spread spectrum differential complement output clock B.
18	CLKB	Output	Selectable 100/200MHz spread spectrum differential true output clock B.
19	CLKA#	Output	Selectable 100/200MHz spread spectrum differential complement output clock A.
20	CLKA	Output	Selectable 100/200MHz spread spectrum differential true output clock A.

Application Information

Decoupling Capacitors

As with any high-performance mixed-signal IC, the IDT5V41236 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the IDT5V41236.

This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 µF should be connected between VDD and GND pairs (1,9 and 15,16) as close to the device as possible.

On chip capacitors- Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value (in pf) of these crystal caps equal (C_L-12)*2 in this equation, C_L=crystal load capacitance in pf. For example, for a crystal with a 16 pF load cap, each external crystal cap would be 8 pF. [(16-12)x2]=8.

Current Reference Source R_r (Iref)

If board target trace impedance (Z) is 50Ω, then Rr = 475Ω (1%), providing IREF of 2.32 mA, output current (I_{OH}) is equal to 6*IREF.

Load Resistors R_L

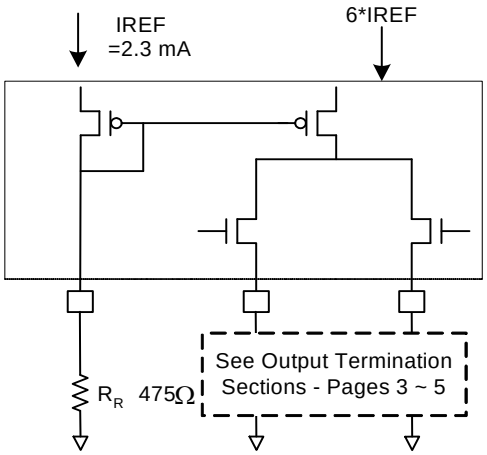
Since the clock outputs are open source outputs, 50 ohm external resistors to ground are to be connected at each clock output.

Output Termination

The PCI-Express differential clock outputs of the IDT5V41236 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The IDT5V41236 can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.

2. No vias should be used between decoupling capacitor and VDD pin.

3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41236.This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Layout Guidelines

SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

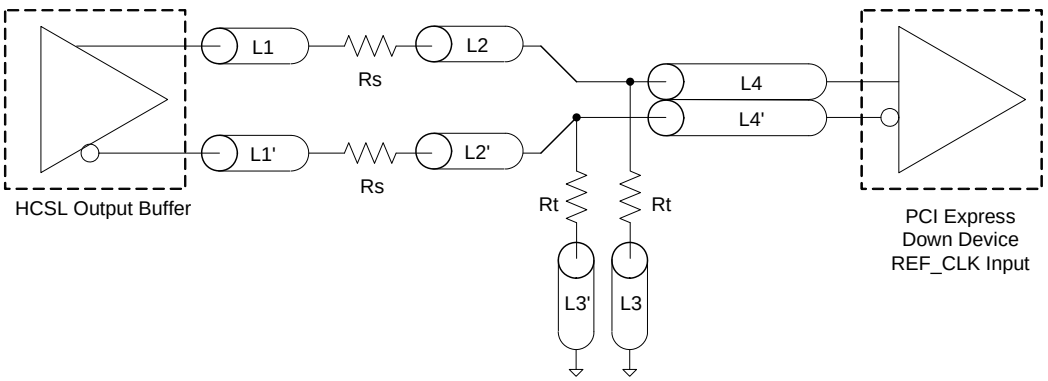
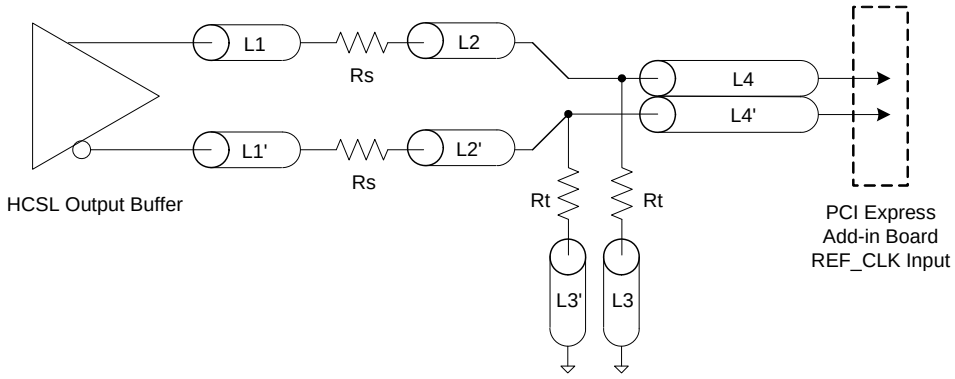


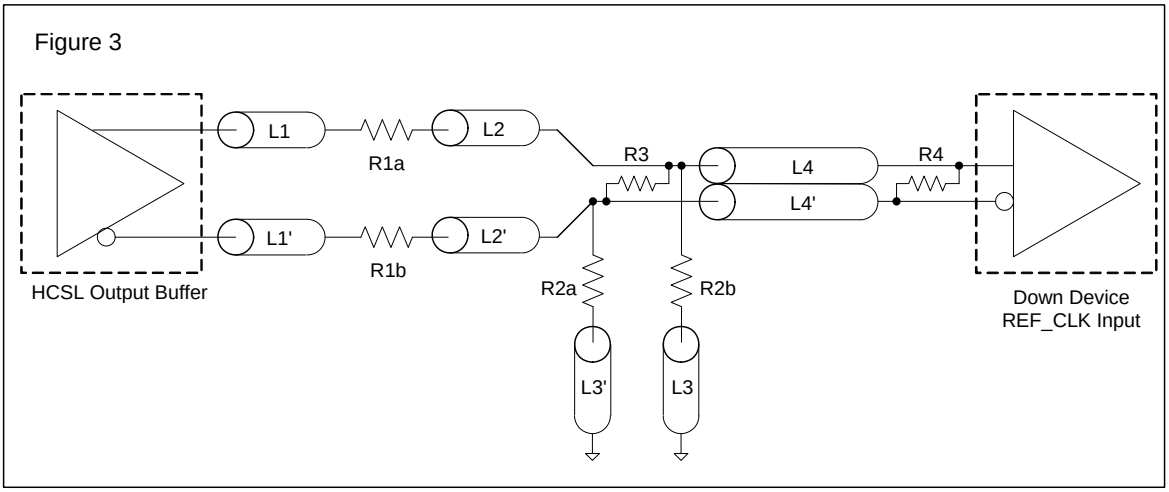
Figure 2: PCI Express Connector Routing



Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

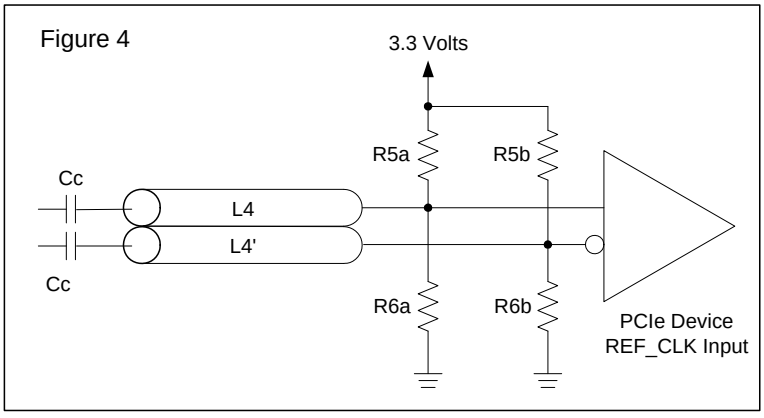
R1a = R1b = R1
R2a = R2b = R2

Figure 3

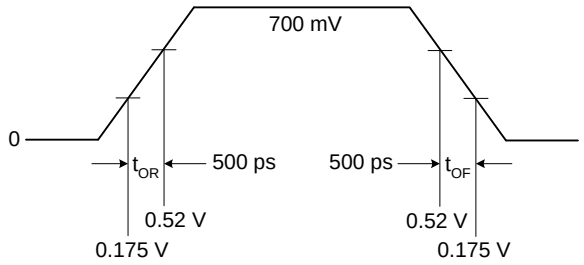


Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

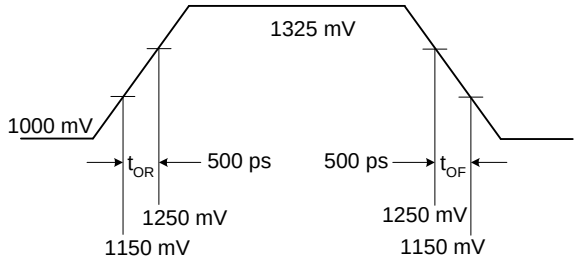
Figure 4



Typical PCI-Express (HCSL) Waveform



Typical LVDS Waveform



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41236. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, VDDA	5.5V
All Inputs and Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature (commercial)	0 to +70°C
Ambient Operating Temperature (industrial)	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (Input)	2000V min. (HBM)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		3.135	3.3	3.465	
Input High Voltage[1]	V_{IH}	S0, S1, S2, OE, X1, PD#	2.2		VDD +0.3	V
Input Low Voltage[1]	V_{IL}	S0, S1, S2, OE, X1, PD#	VSS-0.3		0.8	V
Input Leakage Current[2]	I_{IL}	0 < Vin < VDD	-5		5	µA
Operating Supply Current @100 MHz	I_{DD}	R_S=33Ω, R_P=50Ω, C_L=2 pF		113	125	mA
	I_{DDOE}	OE =Low		42	50	mA
Input Capacitance	C_{IN}	Input pin capacitance			7	pF
Output Capacitance	C_{OUT}	Output pin capacitance			6	pF
X1, X2 Capacitance	C_{INX}				5	pF
Pin Inductance	L_{PIN}				5	nH
Output Impedance	Zo	CLK outputs	3.0			kΩ
Pull-up Resistance	R_{PUP}	S0, S1, OE, S2, PD#		100		kΩ

1. Single edge is monotonic when transitioning through region.
2. Inputs with pull-ups/-downs are not included.

AC Electrical Characteristics - CLKOUT (A:D)

Unless stated otherwise, **VDD=3.3V ±5%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Frequency		HCSL termination	25		200	MHz
Output Max. Voltage[1,2]	V_{MAX}		660	863	1150	mV
Output Min. Voltage[1,2]	V_{MIN}		-300	-53		mV
Crossing Point Voltage[1,2]		Absolute	250	377	550	mV
Crossing Point Voltage[1,2,4]		Variation over all edges		45	140	mV
Jitter, Cycle-to-Cycle[1,3]				29	125	ps
Modulation Frequency		Spread spectrum	30	32.9	33	kHz
Rise Time[1,2]	t_{OR}	From 0.175V to 0.525V	175	237	700	ps
Fall Time[1,2]	t_{OF}	From 0.525V to 0.175V	175	286	700	ps
Rise/Fall Time Variation[1,2]				73	125	ps
Skew between Outputs				8	50	ps
Duty Cycle[1,3]			45	52	55	%
Output Enable Time[5]		All outputs			100	ns
Output Disable Time[5]		All outputs			100	ns
Stabilization Time	t_{STABLE}	From power-up VDD=3.3V		1	1.8	ms
Spread Change Time	t_{SPREAD}	Settling period after spread change			30	ms

[1] Test setup is R_S=33Ω, R_P=50Ω with C_L=2 pF, Rr = 475Ω (1%).

[2] Measurement taken from a single-ended waveform.

[3] Measurement taken from a differential waveform.

[4] Measured at the crossing point where instantaneous voltages of both CLKOUT and $\overline{\text{CLKOUT}}$ are equal.

[5] CLKOUT pins are tri-stated when OE is asserted low. CLKOUT is driven differential when OE is high unless its $\overline{\text{PD}}$ = low.

Electrical Characteristics - Differential Phase Jitter

T_A = Commercial and Industrial, Supply Voltage VDD = 3.3 V +/-5%			SPEC				
PARAMETER	Symbol	Conditions	Min	Typ	Max	Units	Notes
Jitter, Phase	$t_{jphaseG1}$	PCIe Gen 1		30	86	ps (p-p)	1,2,3
	$t_{jphaseG2Lo}$	PCIe Gen 2 10kHz < f < 1.5MHz		1	3	ps (RMS)	1,2,3
	$t_{jphaseG2High}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		2.3	3.1	ps (RMS)	1,2,3
	$t_{jphaseG3}$	PCIe Gen 3		0.7	1	ps (RMS)	1,2,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See http://www.pcisig.com for complete specs

[3]Applies to 100MHz, spread off and 0.5% down spread only.

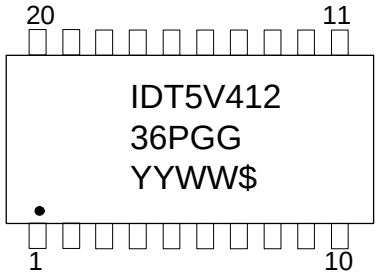
Thermal Characteristics (20TSSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		93		°C/W
	θ_{JA}	1 m/s air flow		78		°C/W
	θ_{JA}	3 m/s air flow		65		°C/W
Thermal Resistance Junction to Case	θ_{JC}			20		°C/W

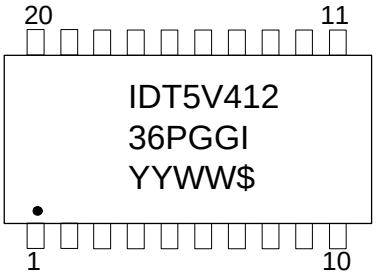
Thermal Characteristics (20VFQFPN)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Marking Diagram (5V41236PGG)



Marking Diagram (5V41236PGGI)



Marking Diagram (5V41236NLG)

Marking Diagram (5V41236NLGI)

Notes:

1."**" denotes lot sequence; "YYWW" or "YWW" – Date code; "$" – mark code.

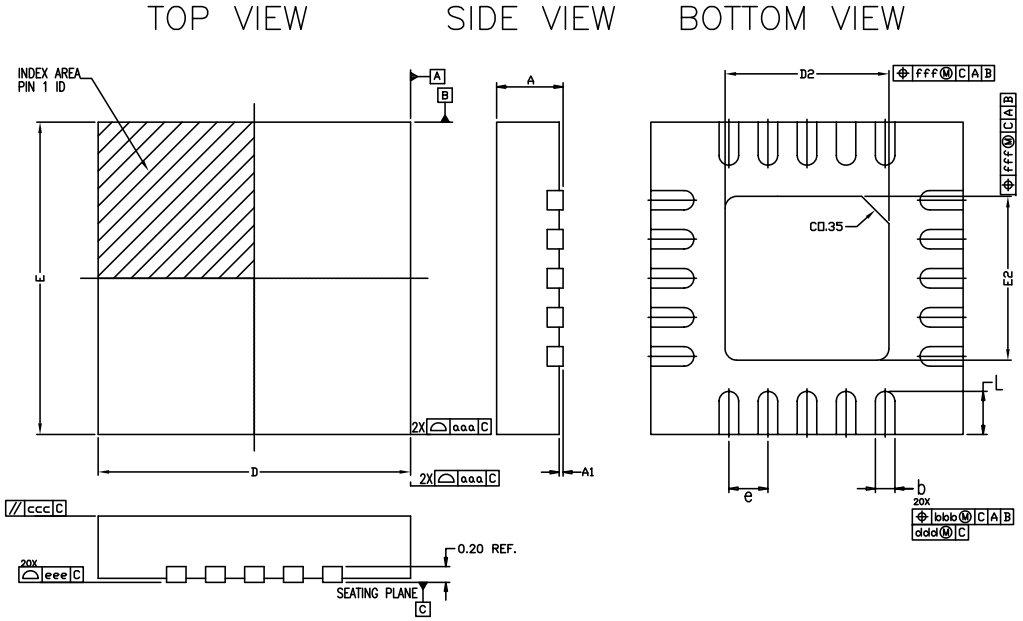
2. "G" after the two-letter package code designates RoHS compliant package.

3. "I" at the end of part number indicates industrial temperature range.

4. Bottom marking: country of origin if not USA. (PGG/I only)

Package Outline and Dimensions (4 x 4 mm, 0.50 Pitch 20-VFQFPN),

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/19/16	JH

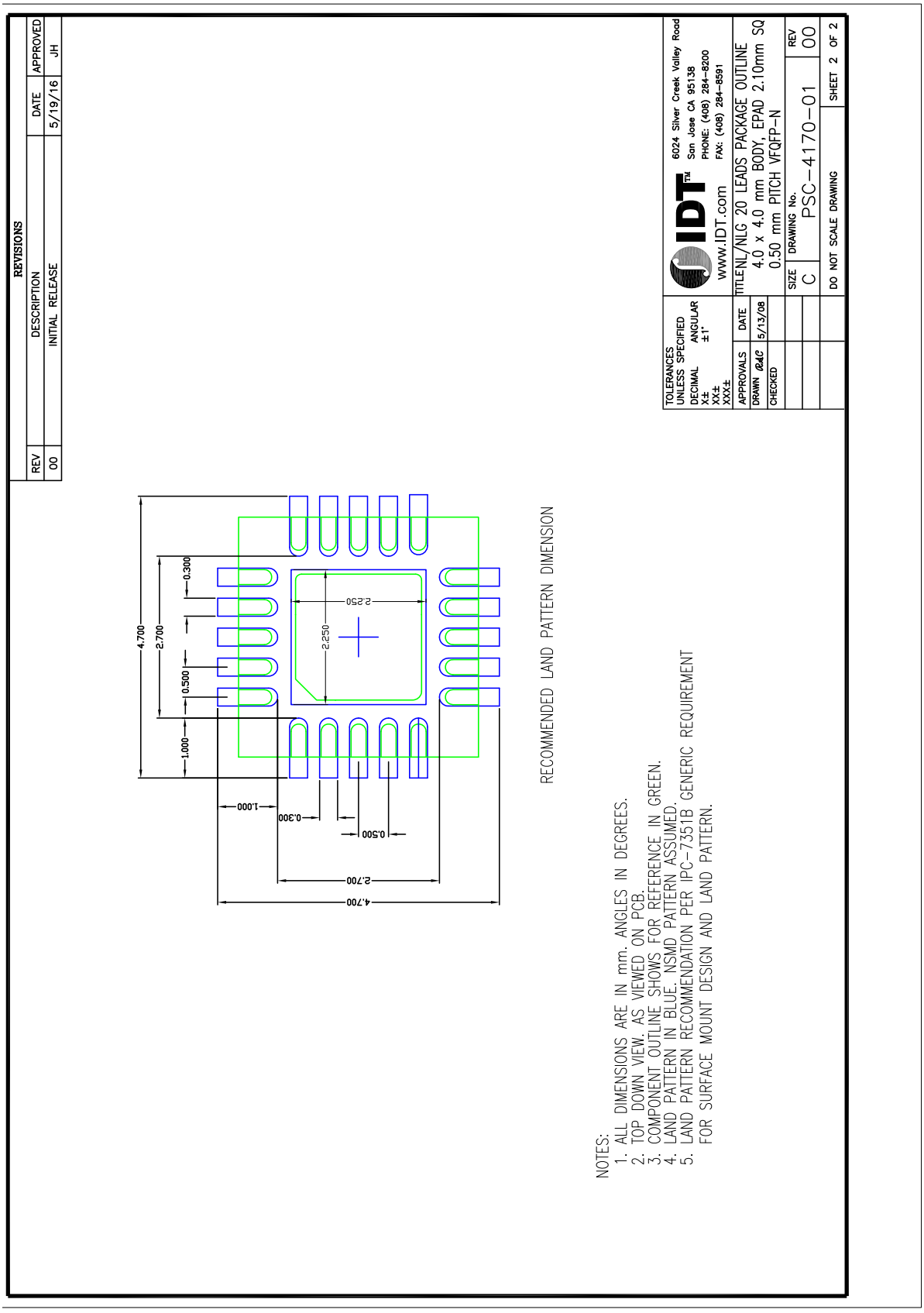


SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	1.95	2.10	2.25
E2	1.95	2.10	2.25
L	0.45	0.55	0.65
e	0.50 BSC		
N	20		
b	0.20	0.25	0.30
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

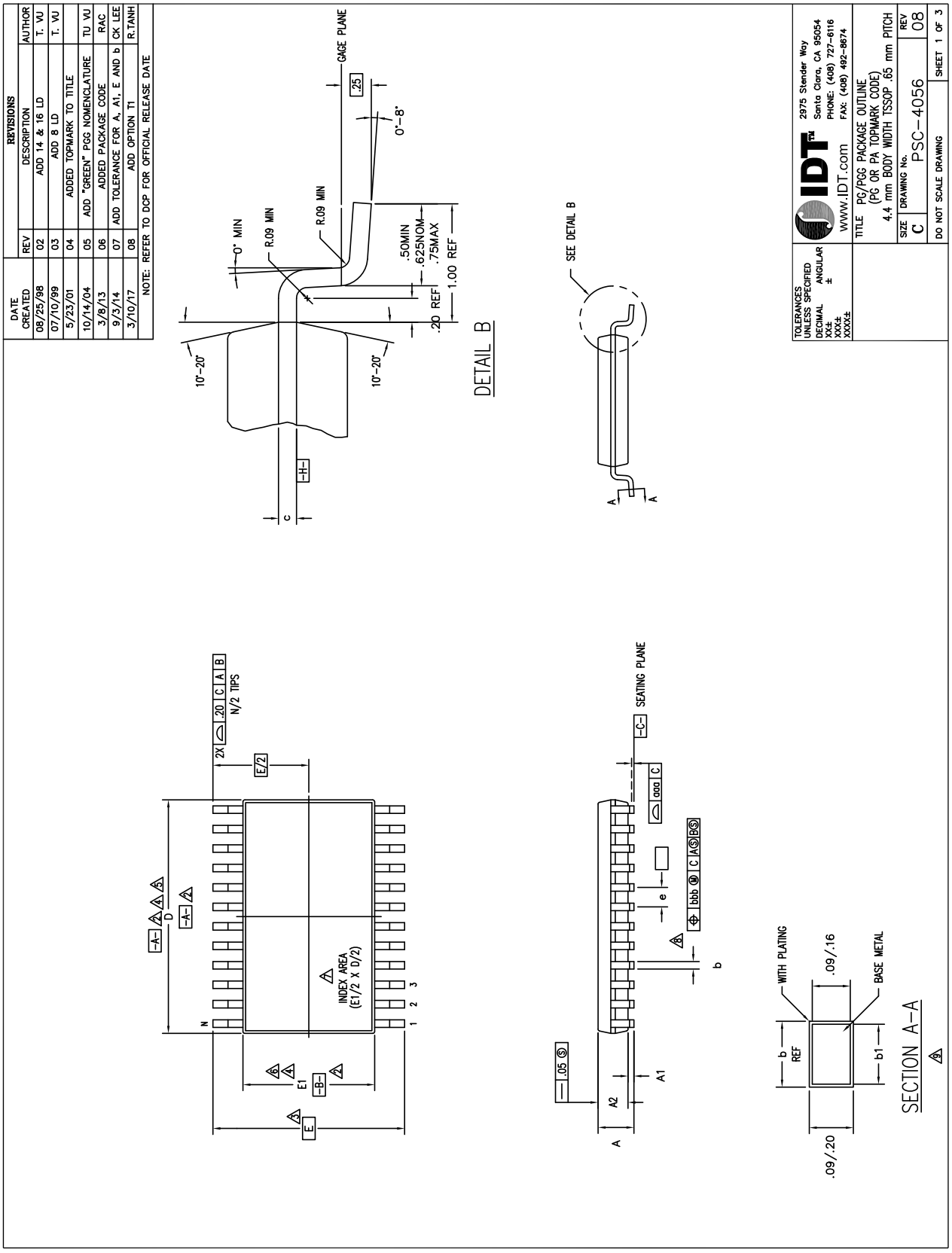
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONING AND TOLERANCING CONFROM TO ANSI Y14.5M–1982.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± ±1° XX± XXX±	IDT™ www.IDT.com 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284–8200 FAX: (408) 284–8591
APPROVALS DATE DRAWN RAC 5/13/08 CHECKED	TITLE NL/NLG 20 LEADS PACKAGE OUTLINE 4.0 x 4.0 mm BODY, EPAD 2.10mm SQ 0.50 mm PITCH VFQFP–N
	SIZE C · DRAWING No. PSC–4170–01 · REV 00
	DO NOT SCALE DRAWING · SHEET 1 OF 2

Package Outline and Dimensions, cont. (4 × 4 mm, 0.50 Pitch 20-VFQFPN),



Package Outline and Dimensions (20-pin TSSOP, 173 mil Body)



Package Outline and Dimensions, cont. (20-pin TSSOP, 173 mil Body)

DATE CREATED	REVISIONS REV	DESCRIPTION	AUTHOR
08/25/98	02	ADD 14 & 16 LD	T. VU
07/10/99	03	ADD 8 LD	T. VU
5/23/01	04	ADDED TOPMARK TO TITLE	
10/14/04	05	ADD "GREEN" PGG NOMENCLATURE	TU VU
3/8/13	06	ADDED PACKAGE CODE	RAC
9/3/14	07	ADD TOLERANCE FOR A, A1, E AND b	CK LEE
3/10/17	08	ADD OPTION T1	R.TANH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

	PG/PGG8				PG/PGG14				PG/PGG16				PG/PGG20				PG/PGG24				PG/PGG28			
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB-1			NOTE	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05	
D	2.90	3.00	3.10	4,5	4.90	5.00	5.10	4,5	4.90	5.00	5.10	4,5	6.40	6.50	6.60	4,5	7.70	7.80	7.90	4,5	9.60	9.70	9.80	4,5
E	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3
E1	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6
e	.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC			
b	.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30	
b1	.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25	
aaa	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
bbb	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
N	8				14				16				20				24				28			

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–153, VARIATION AA, AB–1, AB, AC, AD & AE

	OPTION T1			
	PGG14T1			
SYMBOL	JEDEC VARIATION AB-1			NOTE
	MIN	NOM	MAX	
A	.90	1.10	1.20	
A1	.05	.10	.15	
A2	.80	1.00	1.05	
D	4.90	5.00	5.10	4,5
E	6.20	6.40	6.60	3
E1	4.30	4.40	4.50	4,6
e	.65 BSC			
b	.19	.25	.30	
b1	.19	.22	.25	
c	.09	–	.20	
aaa	–	–	.10	
bbb	–	–	.10	
N	14			

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

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TITLE PG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE C | DRAWING No. PSC-4056 | REV 08

DO NOT SCALE DRAWING | SHEET 2 OF 3

Package Outline and Dimensions, cont. (20-pin TSSOP, 173 mil Body)

DATE CREATED	REV	REVISIONS DESCRIPTION	AUTHOR
08/25/98	02	ADD 14 & 16 LD	T. VU
07/10/99	03	ADD 8 LD	T. VU
5/23/01	04	ADDED TOPMARK TO TITLE	
10/14/04	05	ADD "GREEN" PGG NOMENCLATURE	TU VU
3/8/13	06	ADDED PACKAGE CODE	RAC
9/3/14	07	ADD TOLERANCE FOR A, A1, E AND b	CK LEE
3/10/17	08	ADD OPTION T1	R.TANH

NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

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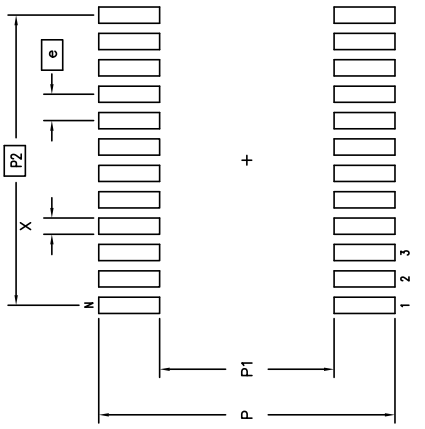
TITLE PG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE C | DRAWING No. PSC-4056 | REV 08

DO NOT SCALE DRAWING | SHEET 3 OF 3

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40
P2	1.95 BSC		3.90 BSC		4.55 BSC		5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	8		14		16		20		24		28	

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V41236PGG	see page 11	Tubes	20-pin TSSOP	0 to +70°C
5V41236PGG8		Tape and Reel	20-pin TSSOP	0 to +70°C
5V41236PGGI		Tubes	20-pin TSSOP	-40 to +85°C
5V41236PGGI8		Tape and Reel	20-pin TSSOP	-40 to +85°C
5V41236NLG	see page 11	Trays	20-pin VFQFPN	0 to +70°C
5V41236NLG8		Tape and Reel	20-pin VFQFPN	0 to +70°C
5V41236NLGI		Trays	20-pin VFQFPN	-40 to +85°C
5V41236NLGI8		Tape and Reel	20-pin VFQFPN	-40 to +85°C

"G" after the two-letter package code are the Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	RDW	09/26/11	Initial release.
B	RDW	11/22/11	1. Changed title to "4 Output PCIe GEN1/2/3 Synthesizer" 2. Updated Differential Phase Jitter table.
C	LPL	02/04/14	Typo in VFQFPN T&R ordering information and VFQFPN device markings.
D	J.C.	06/06/16	1. Updated "Operating Supply Current" parameters/values and Conditions in DC Electrical Characteristics table. 2. Updated RPUP, VIH and VIL conditions.
E	RDW	02/13/17	1. Updated Operating Supply Current [IDD] typical and maximum values. 2. Added typical values to AC Electrical Characteristics CLKOUT (A:D) table. 3. Updated typical values in Differential Phase Jitter table. 4. Updated 20-VFQFPN POD drawing.
F	RDW	04/04/17	1. Update "AC Electrical Characteristics - CLKOUT(A:D)" table values to latest PCIe specifications and characterization data. 2. Updated package outline drawings. 3. Updated legal disclaimer.

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