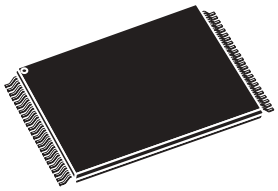
NAND16GW3D2B

16-Gbit, 4320-byte page, 3 V supply, multiplane architecture, multilevel cell NAND flash memory

Features

- High density multilevel cell (MLC) flash memory
  - 16 Gbits of memory array
  - Cost-effective solutions for mass storage applications
- NAND interface
  - x8 bus width
  - Multiplexed address/data
  - Pin-out compatibility for all densities
- Supply voltage
  - V_{DD} = V_{DDQ} = 2.7 to 3.6 V
- Page size: (4096 + 224 spare) bytes
- Block size: (512K + 28K spare) bytes
- Enhanced data throughput by multiplane architecture
  - Array split into two independent planes
  - All operations performed on both planes simultaneously
- Page read/program
  - Random access: 60 µs (max)
  - Page program operation time: 800 µs (typ)
  - Multiplane page program operation time: 800 µs (typ)
- Page serial access (data in/out): 25 ns
- Copy-back program
  - Fast page copy with/without external buffering
  - Multiplane copy back program
- Fast block erase
  - Block erase time: 2.5 ms (typ)
  - Multiplane block erase time: 2.5 ms (typ)
- Throughput improvement with cache program, multiplane cache program, cache read, multiplane cache read
- Cache read: automatic block download without latency time



TSOP48 12 x 20 mm (N)

- PSL (power on selection) for device initialization
- Status register
- Electronic signature
- Chip enable ‘don’t care’
- Security features
  - OTP area
  - Serial number (unique ID) option
- Data protection
  - Hardware program/erase locked during power transitions
- Data integrity
  - 5,000 program/erase cycles (with 12-bit/512-byte ECC)
  - 5 years data retention
- RoHS compliant package

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1 Description

The NAND16GW3D2B device, which provide the most cost-effective solution for the solid state mass storage market, is offered with core power supply (V_{DD}) and input/output power supply (V_{DDQ}) of 3.3 V. The device operates from a 3 V power supply.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

The memory is divided into blocks that can be erased independently. It is possible, therefore, to preserve valid data while old data are erased.

The 16-Gbit device includes 4096 blocks. Each block is composed by 128 pages consisting of two NAND structures of 32 series connected flash cells. Every cell holds two bits.

The memory array is split into 2 planes. This multiplane architecture makes it possible to program 2 pages at a time (one in each plane), to erase 2 blocks at a time (one in each plane), or to read 2 pages at a time (one in each plane) dividing by two the average program, erase, and read times.

The device has the Chip Enable 'don't care' feature, which allows the bus to be shared between more than one memory at the same time, as Chip Enable transition during the latency time do not stop the read operation. Program and erase operations can never be interrupted by Chip Enable transition.

Commands, data and addresses are synchronously introduced using $\overline{E}$, $\overline{W}$, AL and CL input pins. The on-chip program/erase controller automates all read, program and erase operations including pulse repetition, where required, internal verification and margining of data. The modify operations can be locked using the Write Protect input.

The open drain ready/busy output indicates the device's status during each operation. In a system made of multiple memories the ready/busy pins can be connected all together to provide a system's status global indicator.

In addition to the enhanced architecture and interface, the device features the copy back program function from one page to another without the need of moving data to and from the external buffer memory. Since the time-consuming serial access and data input cycles are removed, system performance is significantly increased.

The cache program feature allows data insertion in the cache register while the data register is copied into the flash array. This pipelined program operation improves the program throughput when long files are written inside the memory.

The cache read feature allows to dramatically improve read throughput when consecutive pages have to be streamed out.

To further increase devices' performance, the cache program and cache read features are also supported in multiplane architecture.

Each block can be programmed and erased up to 5,000 cycles by providing 12-bit/512-byte ECC (Error Correction Code) with real time mapping-out algorithm. The spare area must be covered by ECC.

The device comes with two security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently. The access sequence and further details about this feature are subject to an NDA (non disclosure agreement)
- Serial number (unique identifier) option, which enables each device to be uniquely identified. It is subject to an NDA and is, therefore, not described in the datasheet.

For more details about these security features, contact your nearest Numonyx sales office.

The NAND16GW3D2B is available in the TSOP48 12 mm x 20 mm package.

The device is shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

Refer to *Table 1* for a device summary and to *Table 29: Ordering information scheme* for information on how to order these options.

Table 1. Device summary

Root part number	Density	Bus width	Core power supply (V_{DD})	Package
NAND16GW3D2B	16 Gbits	x8	2.7 to 3.6 V	TSOP48 12 mm x 20 mm

Figure 1. Logic block diagram

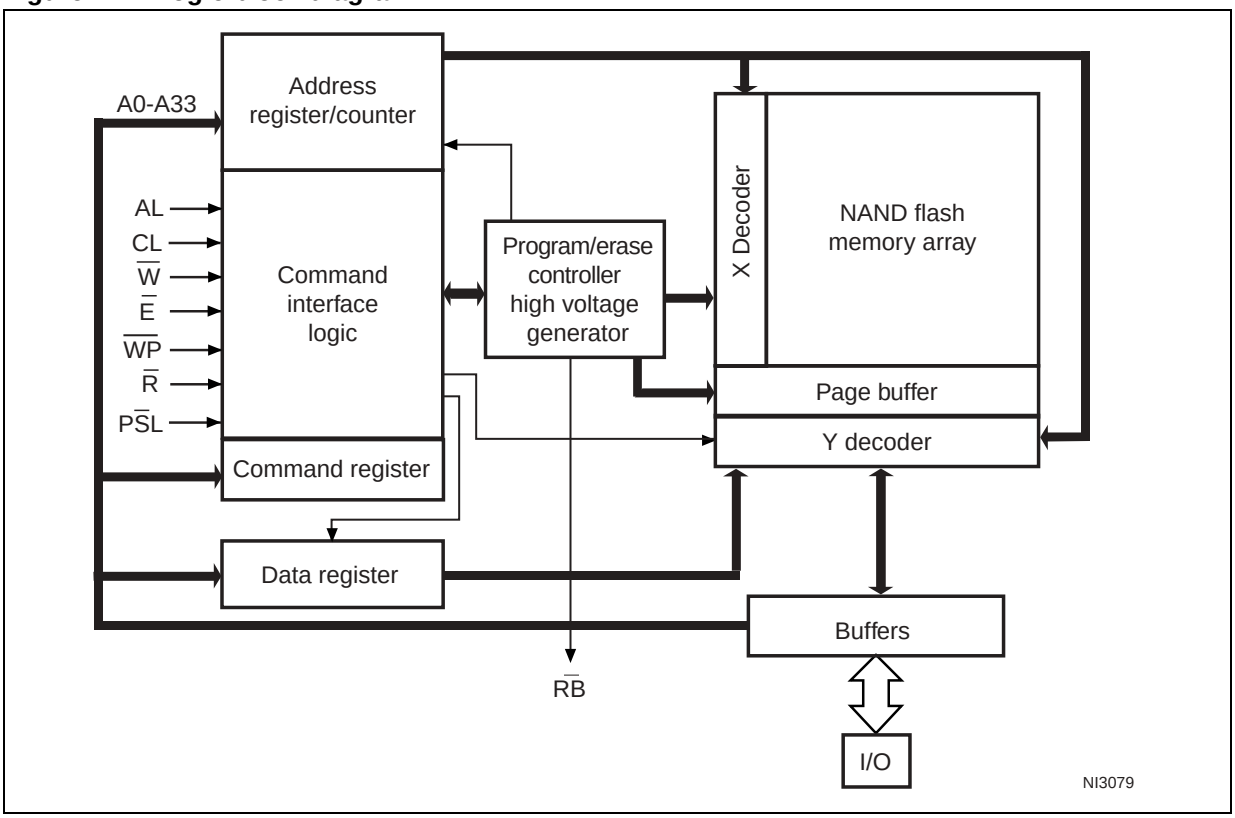


Figure 2. Logic diagram

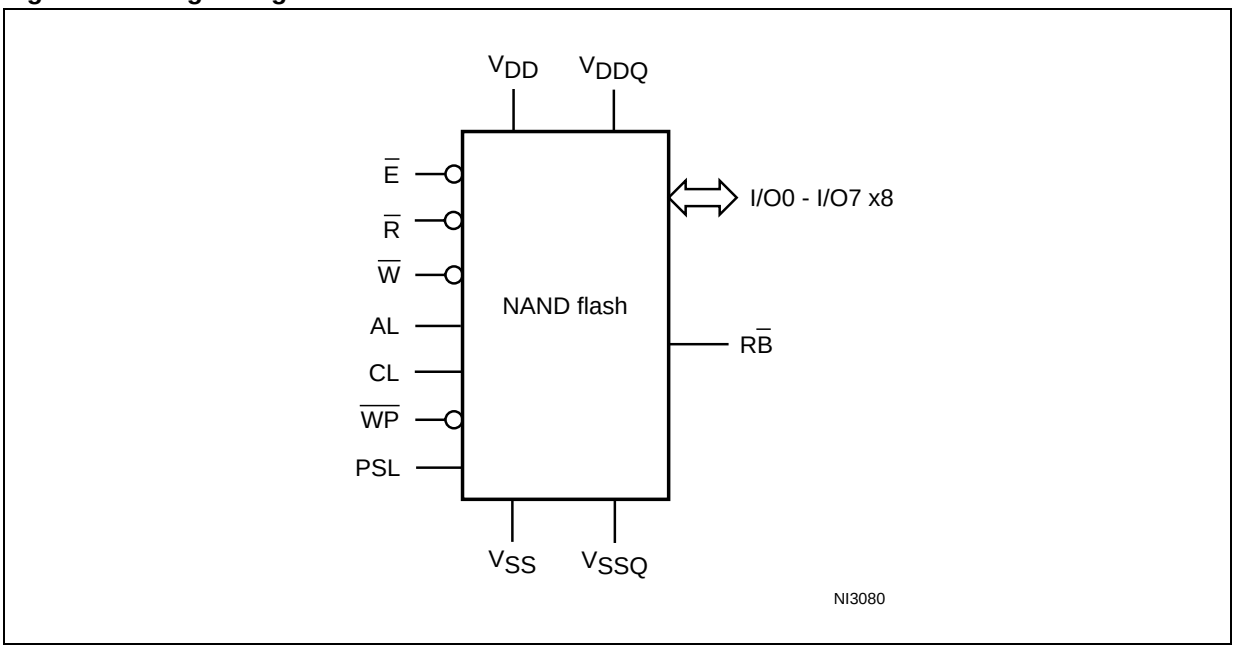
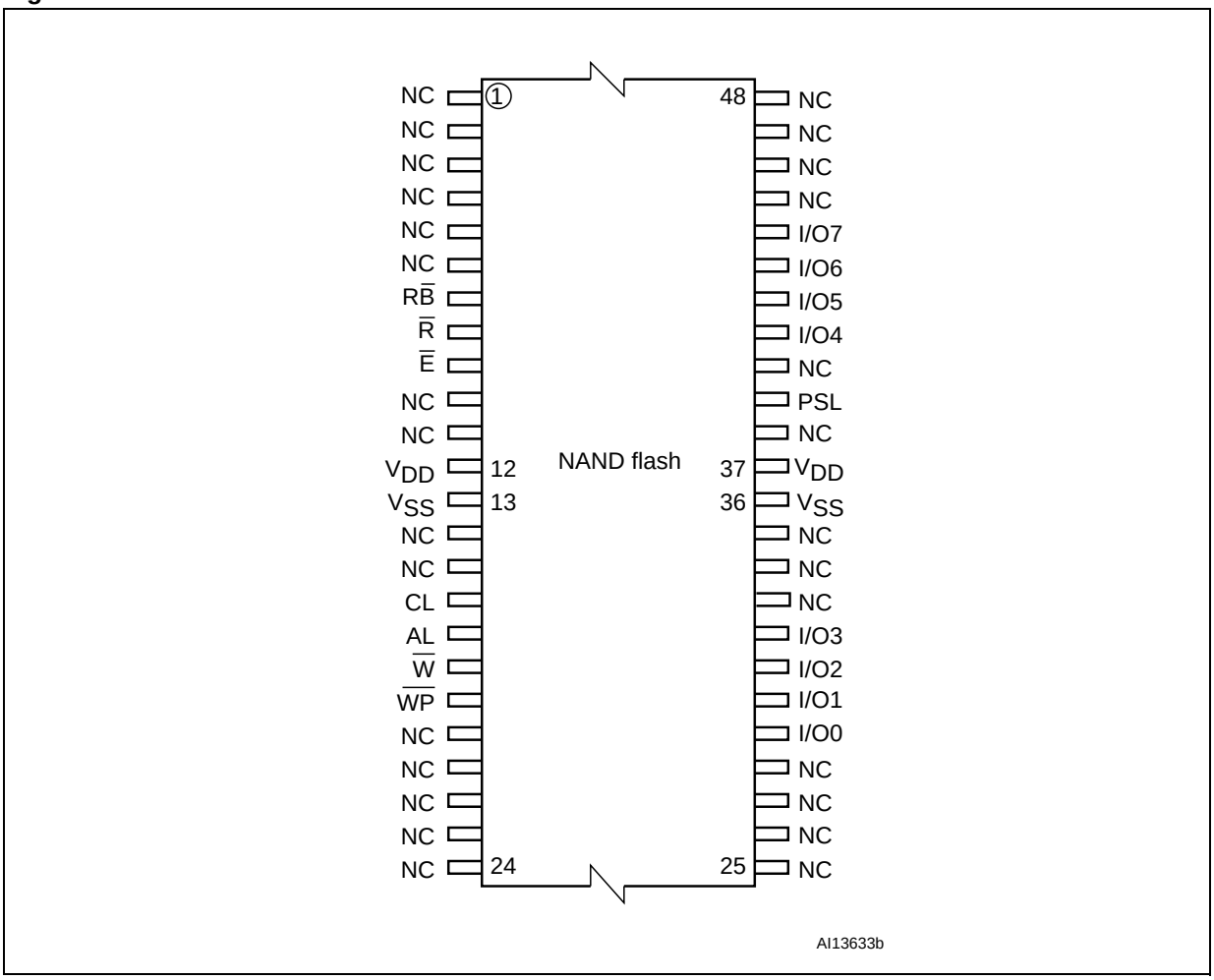


Table 2. Signal names

Signal	Function	Direction
I/O0 - I/O7	Data inputs/outputs	Inputs/outputs
CL	Command Latch Enable	Input
AL	Address Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
PSL	Power on selection	Input
$R\overline{B}$	Ready/Busy (open drain output)	Output
V_{DD}	Power supply	Power supply
V_{DDQ}	Input/output power supply	Power supply
V_{SS}	Ground	Ground
V_{SSQ}	Input/output ground	Ground
NC	No connection	–

Figure 3. TSOP48 connections



2 Memory array organization

The memory array is comprised of NAND structures consisting of 32 cells connected in series.

It is organized in 4096 blocks. Each block contains 128 pages. The array is split into two areas, the main area and the spare area. The main area of the array stores data, whereas the spare area typically stores software flags or bad block identification.

The pages are split into a 4096-byte main area and a spare area of 224 bytes. Refer to *Figure 4: Memory array organization*.

Figure 4. Memory array organization

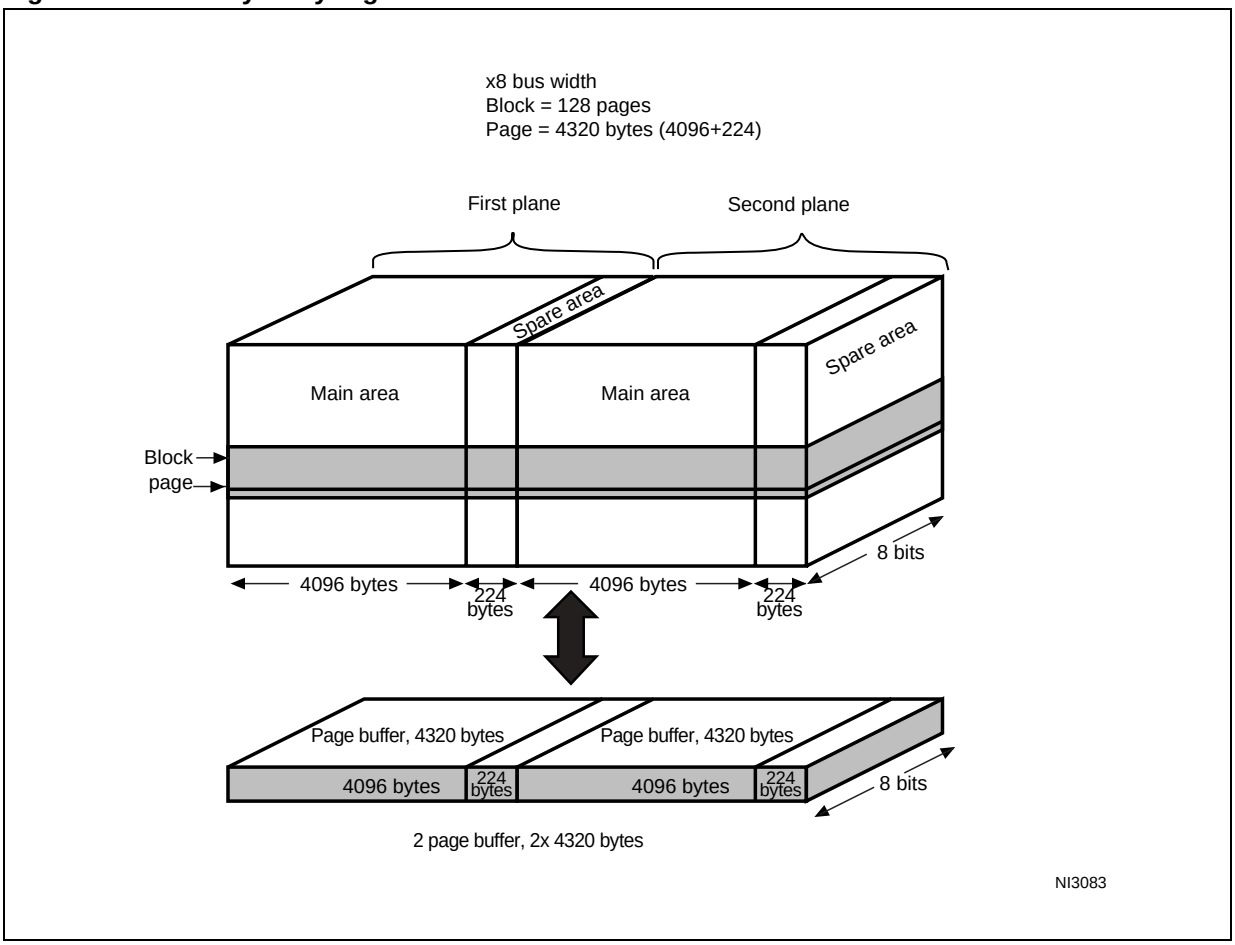


Table 3. Address insertion(1)

Bus cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	A12	A11	A10	A9	A8
3rd	A20	A19	A18	A17	A16	A15	A14	A13
4th	A28	A27	A26	A25	A24	A23	A22	A21
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A31	A30	A29

1. Any additional address input cycles are ignored.

Table 4. Address definitions

Address	Definition
A0 - A12	Column address
A13 - A19	Page address
A20	Plane address
A21 - A31	Block address in each plane

2.1 Bad blocks

The NAND16GW3D2B device may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to *Section 10.1: Bad block management* for more details).

Table 5: Valid blocks shows the minimum number of valid blocks. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management and block replacement (refer to *Section 10: Software algorithms*).

Table 5. Valid blocks

Density of device	Minimum	Maximum
16 Gbits	3996	4096

3 Signals description

See *Figure 1: Logic block diagram*, and *Table 2: Signal names* for a brief overview of the signals connected to this device.

3.1 Data inputs/outputs (I/O0-I/O7)

Inputs/outputs 0 to 7 are used to input the selected command, address or data, output the data during read or program operations. The inputs are latched on the rising edge of Write Enable ($\overline{W}$). I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable ($\overline{W}$).

3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable ($\overline{W}$).

3.4 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.5 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.6 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address, and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-on and power-off a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.7 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-on and power-off.

3.8 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low indicates that one, or more, of the memories is busy.

During power-on and power-off a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the Ready/Busy signal is Low, V_{OL}.

Refer to *Section 13.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.9 Power on selection (PSL)

The power on selection pin is used to select whether the device initialization will occur during the device's power-on or during the first reset.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, write and erase).

3.11 V_{DDQ} supply voltage

V_{DDQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{DD}.

3.12 V_{SS} ground

V_{SS} ground is the reference for the core power supply. It must be connected to the system ground.

3.13 V_{SSQ} ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: 1 V_{DDQ} and V_{DD}, V_{SSQ} and V_{SS} must be respectively shorted together at any time. Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor.

2 All the V_{DD}, V_{DDQ}, V_{SS} and V_{SSQ} pins must be connected to the common power supply outputs.

3 The PCB track widths should be sufficient to carry the required program and erase currents.

4 Bus operations

There are six standard bus operations that control the device. These are command input, address input, data input, data output, write protect and standby. See *Table 6: Bus operations* for a summary.

Typically, glitches of less than 5 ns on Write Enable or Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command input

Command input bus operations give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Moreover, for commands that start a modify operation (write or erase), the Write Protect pin must be High.

Only I/O0 to I/O7 are used to input commands.

See *Figure 37: Command Latch AC waveforms* and *Table 26: AC characteristics for command, address, data input* for details of the timings requirements.

4.2 Address input

Address input bus operations input the memory addresses. Five bus cycles are required to input the addresses. The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Moreover, for commands that start a modify operation (write or erase), the Write Protect pin must be High.

Only I/O0 to I/O7 are used to input addresses.

See *Figure 38: Address Latch AC waveforms* and *Table 26: AC characteristics for command, address, data input* for details of the timings requirements.

4.3 Data input

Data input bus operations input the data to be programmed. Data is only accepted when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low, Read Enable is High and Write Protect is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 39: Data Input Latch AC waveforms* and *Table 26: AC characteristics for command, address, data input* for details of the timing requirements.

4.4 Data output

Data output bus operations read the data in the memory array, the status register, the electronic signature, and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

If the Read Enable pulse frequency is lower than 33 MHz (t_{RLRL} higher than 30 ns), the output data is latched on the rising edge of Read Enable signal (see *Figure 41: Sequential data output after read AC waveforms*).

For higher frequencies (t_{RLRL} lower than 30 ns), the extended data out (EDO) mode must be considered. In this mode, data output is valid on the input/output bus for a time of t_{RLQX} after the falling edge of Read Enable signal (see *Figure 40: Sequential data output after read AC waveforms in EDO mode*).

See figures *40*, *41*, *Figure 42: Read Status Register AC waveforms*, *Figure 5: Page read operation*, *Table 26: AC characteristics for command, address, data input* and *Table 27: AC characteristics for operations,* for details on the timings requirements.

4.5 Write protect

Write protect bus operations protect the memory against program or erase operations. When the Write Protect signal is Low the device does not accept program or erase operations, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-on (refer to *Section 9: Write protect operation* for further details).

4.6 Standby

The memory enters standby mode by holding Chip Enable, $\overline{E}$, High for at least 10 µs. In standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 6. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	PSL(1)
Command input (read mode)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X	0 V/V_{DDQ}/NC
Command input (write mode)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	V_{IH}	0 V/V_{DDQ}/NC
Address input (read mode)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	0 V/V_{DDQ}/NC
Address input (write mode)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	V_{IH}	0 V/V_{DDQ}/NC
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	0 V/V_{DDQ}/NC
Data output	V_{IL}(2)	V_{IL}	V_{IL}	Falling	V_{IH}	X	0 V/V_{DDQ}/NC
During read (busy)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	0 V/V_{DDQ}/NC
During program (busy)	X	X	X	X	X	V_{IH}	0 V/V_{DDQ}/NC
During erase (busy)	X	X	X	X	X	V_{IH}	0 V/V_{DDQ}/NC
Write protect	X	X	X	X	X	V_{IL}	0 V/V_{DDQ}/NC
Standby	V_{IH}	X	X	X	X	0 V/V_{DDQ}	0 V/V_{DDQ}/NC

1. PSL must be tied to either 0 V or V_{DDQ}, or left unconnected (NC)
2. As the devices are Chip Enable don't care, Chip Enable High during the latency time does not stop read operations.

5 Command set

All bus write operations to the memory are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is High. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 7: Command set*.

Table 7. Command set

Function	1st cycle	2nd cycle	3rd cycle	4th cycle	Acceptable command during busy
Page Read	00h	30h			
Single Plane Cache Read (start)					
Multiplane Page Read	60h	60h	30h		
Multiplane Cache Read (start)	60h	60h	33h		
Single/Multiplane Cache Read	31h				
Single/Multiplane Cache Read (end)	3Fh				
Read for Copy Back	00h	35h			
Read ID	90h				
Page Program (start)	80h	10h			
Cache Program (end)					
Multiplane Page Program	80h	11h	81h	10h	
Multiplane Cache Program (end)					
Cache Program (start)	80h	15h			
Multiplane Cache Program (start)	80h	11h	81h	15h	
Copy Back Program	85h	10h			
Multiplane Copy Back Program	85h	11h	81h	10h	
Multiplane Copy Back Read	60h	60h	35h		
Block Erase	60h	D0h			
Multiplane Block Erase	60h	60h	D0h		
Read Status Register	70h				Yes
Multiplane Read Status Register	F1h				Yes
Random Data Input	85h				
Random Data Output	05h	E0h			
Multiplane Random Data Output	00h	05h	E0h		
Reset	FFh				Yes

6 Device operations

6.1 Single plane operations

6.1.1 Page read

The page read operation is started by issuing the Page Read command (00h) followed by five address input cycles, and then by a Confirm command (30h). Consecutive read operations require the Page Read command to be issued to read from the second page onwards.

Once a Read command is issued, two types of read operations are available: random read and sequential page read. The random read mode is enabled when the page address is changed, in all the other cases the sequential page read is enabled.

After the first random read access, the 4320 bytes of data in the selected page are transferred to the data registers in a time of t_{WHBH} (refer to *Table 27: AC characteristics for operations* for value). The system controller detects the completion of the data transfer by either analyzing the output of the Ready/Busy signal, or issuing the Read Status Register commands (70h or F1h) or monitoring IO6 (Ready/Busy) through the Read Enable toggling. In this latter case, the device will output the Read Status until the command 00h is issued.

Once the transfer is complete, the data can then be read out sequentially (from the selected column address to the last column address) by pulsing the Read Enable signal (see *Figure 5: Page read operation*) every t_{RLRL} (25 ns).

The device can output random data in a page, instead of the consecutive sequential data, by issuing a Random Data Output command. The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command. The Random Data Output command can be issued as many times as required within a page.

Note: At power-on the device defaults to page read only if PSL is tied to V_{SS}/V_{SSQ} or left floating. For further information refer to Section 8: Power-on sequence and PSL handling.

Figure 5. Page read operation

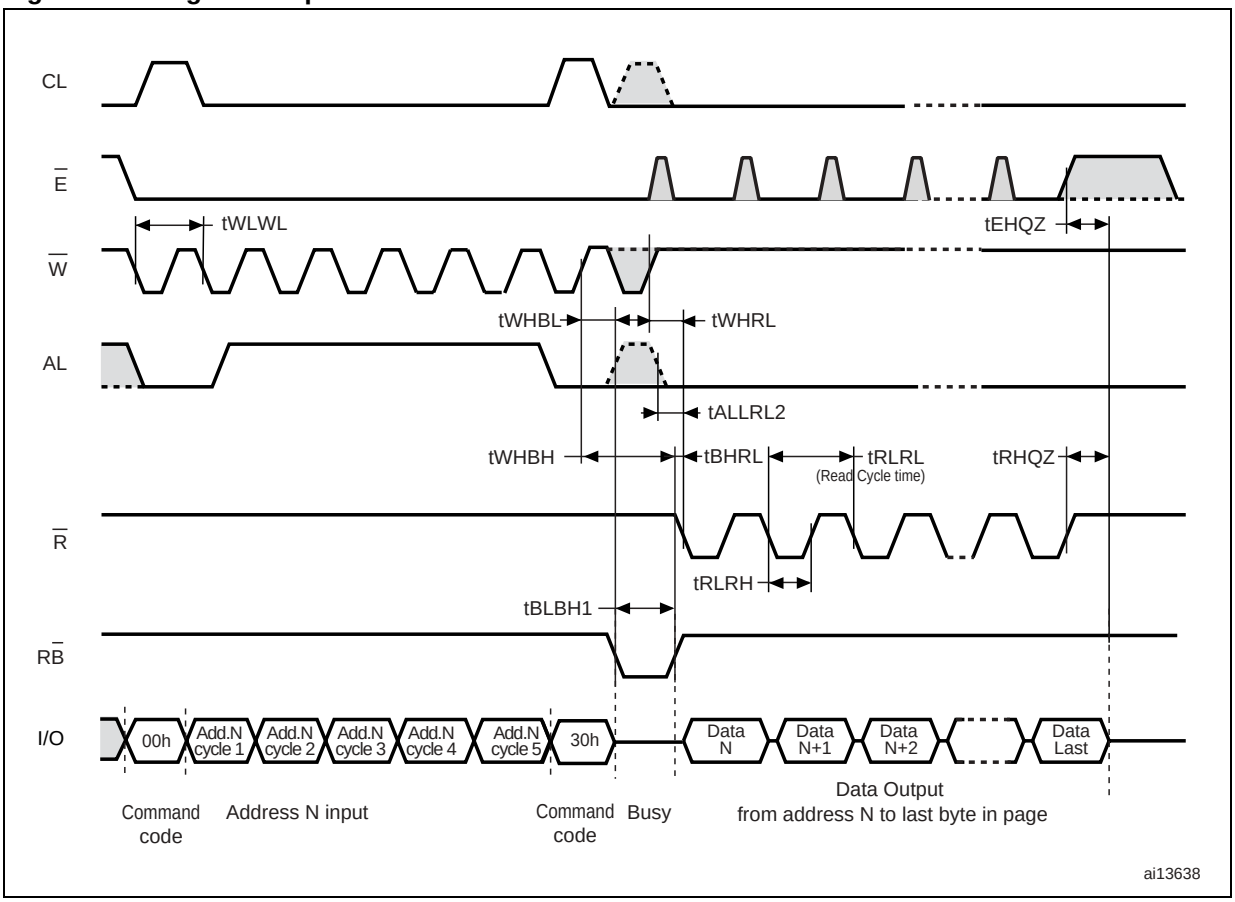
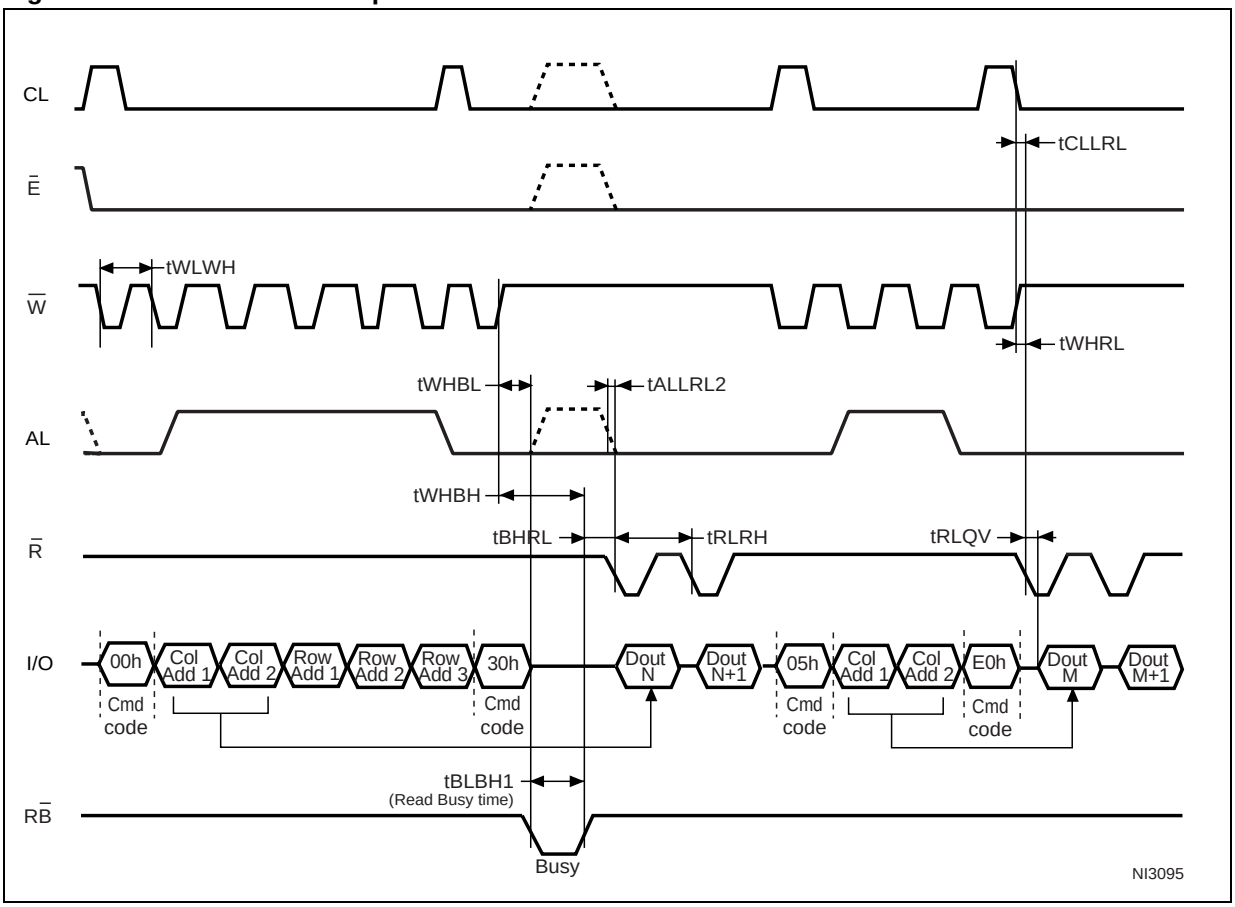


Figure 6. Random data output



6.1.2 Page program

The page program operation is the standard operation to program data to the memory array. Within a given block, the pages must be programmed sequentially. Only one partial page program operation is allowed on the same page (see *Table 20: Busy times*).

A page program cycle consists of a serial data loading period, in which up to 4320 bytes of data can be loaded into the data register, followed by a non-volatile programming period where loaded data is programmed in the memory array. The serial data loading period starts by issuing the Serial Data Input command (80h), followed by five cycle address inputs and serial data.

The Page Program Confirm command (10h) starts the programming process (provided that the serial data is already entered). The internal write state controller automatically executes the algorithms and timings needed to program and verify, thus leaving the system controller free for other tasks. Once the program process starts, the Read Status Register command can be entered to read the status register.

The system controller detects the completion of a program cycle by either analyzing the output of the Ready/Busy signal, or of the Status Register bit I/O6 (ready/busy bit).

During the page program operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored. When the page program is complete, The write status bit I/O0 (pass/fail bit) can be checked. During page program operations the

status register only flags errors for bits set to ‘1’ that have not been successfully programmed to ‘0’.

The device remains in read status register mode until another valid command is written to the command register. *Figure 6.1.3: Block erase* details the command sequence.

If the program operation is interrupted by either a power-off or a reset operation, the block data is no longer valid, as the program algorithm was not executed entirely.

Moreover, when a program operation is abnormally aborted (such as during a power-off), the page data under program data as well as the paired page data may be damaged (refer to *Table 8: Paired page address information*).

The device supports random data input within a page. The column address of next data can be changed to the address which follows Random Data Input command (85h). The Random Data Input command can be issued as many times as required within a page.

Figure 7. Page program operation

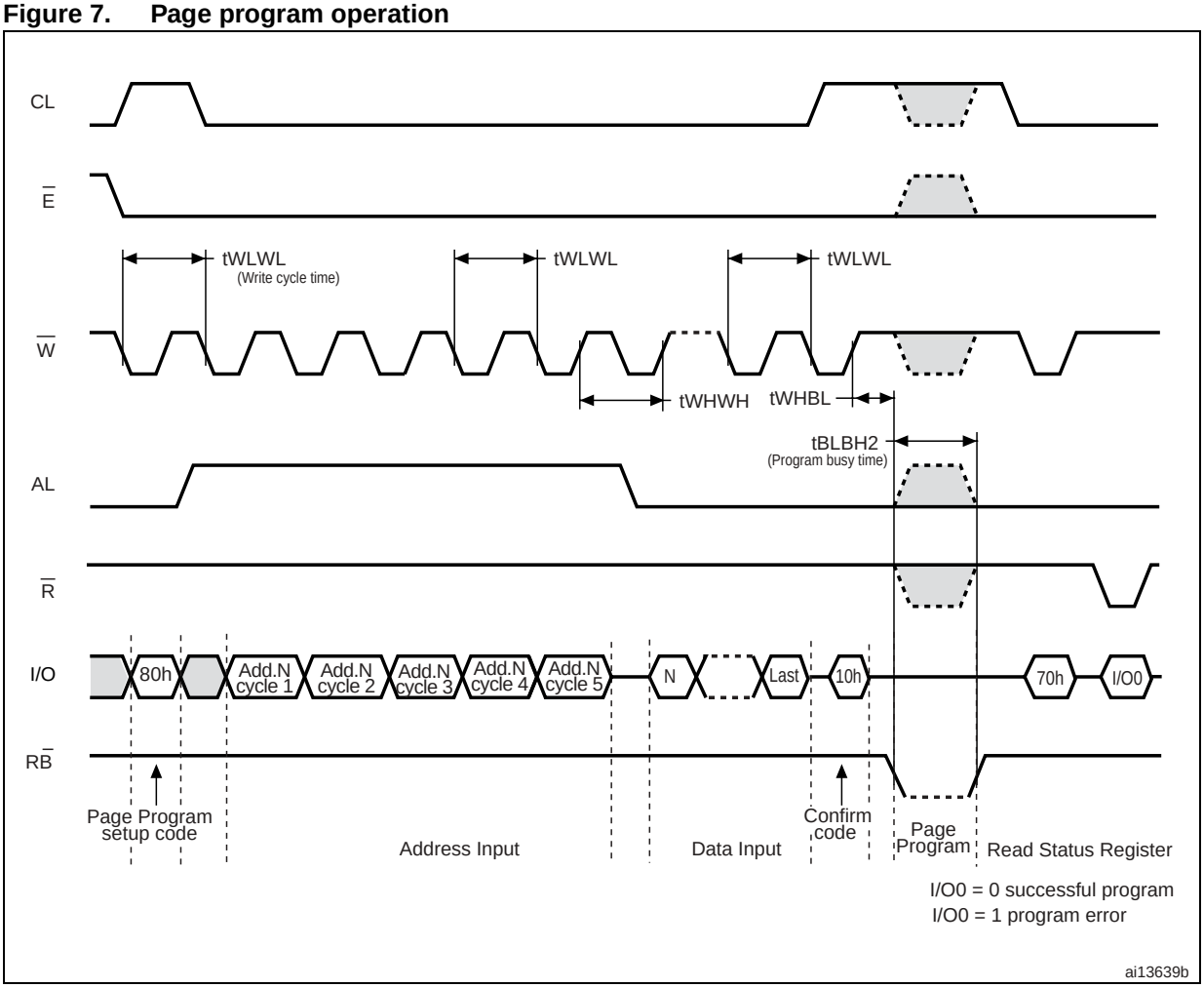


Table 8. Paired page address information

Paired page address		Paired page address	
00h	04h	01h	05h
02h	08h	03h	09h
06h	0Ch	07h	0Dh
0Ah	10h	0Bh	11h
0Eh	14h	0Fh	15h
12h	18h	13h	19h
16h	1Ch	17h	1Dh
1Ah	20h	1Bh	21h
1Eh	24h	1Fh	25h
22h	28h	23h	29h
26h	2Ch	27h	2Dh
2Ah	30h	2Bh	31h
2Eh	34h	2Fh	35h
32h	38h	33h	39h
36h	3Ch	37h	3Dh
3Ah	40h	3Bh	41h
3Eh	44h	3Fh	45h
42h	48h	43h	49h
46h	4Ch	47h	4Dh
4Ah	50h	4Bh	51h
4Eh	54h	4Fh	55h
52h	58h	53h	59h
56h	5Ch	57h	5Dh
5Ah	60h	5Bh	61h
5Eh	64h	5Fh	65h
62h	68h	63h	69h
66h	6Ch	67h	6Dh
6Ah	70h	6Bh	71h
6Eh	74h	6Fh	75h
72h	78h	73h	79h
76h	7Ch	77h	7Dh
7Ah	7Eh	7Bh	7Fh

6.1.3 Block erase

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 8: Block erase operation*):

1. One bus cycle is required to setup the Block Erase command (60h).
2. Three bus cycles are then required to load the address of the block to be erased. Refer to *Table 4: Address definitions* for the block addresses of each device. Only addresses A20 to A31 are valid while the addresses A13 to A19 are ignored
3. One bus cycle is required to issue the Block Erase Confirm command (D0h) to start the P/E/R controller.

The erase operation is initiated on the rising edge of Write Enable, $\overline{W}$, after the Block Erase Confirm command is issued. The P/E/R controller handles block erase and implements the verify process.

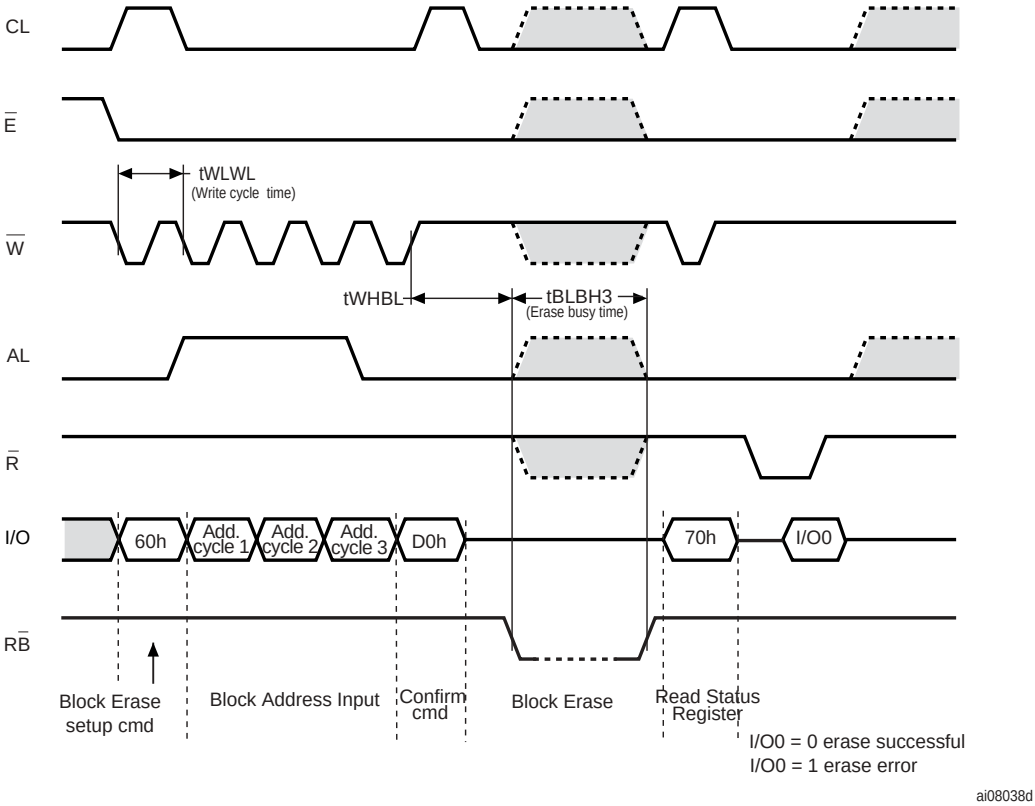
During the block erase operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored.

The system controller detects the completion of a erase operation by either analyzing the output of the Ready/Busy signal, or the Status Register bit I/O6 (ready/busy bit).

If the operation completes successfully, the write status bit I/O0 is ‘0’, otherwise it is set to ‘1’ (refer to *Section 6.3: Reset*).

If the erase operation is interrupted by either a power-off or a reset operation, the block data is no longer valid, as the erase algorithm was not executed entirely.

Figure 8. Block erase operation



6.1.4 Copy back program

The copy-back program with read for copy-back operation allows to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored.

Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is evident when a portion of a block is updated and the rest of the block also needs to be copied to the newly-assigned free block.

The copy-back operation is a sequential execution of a read for copy-back and a copy back program followed by the destination page address. A read operation with a 35h command and the address of the source page moves the entire 4320 bytes into the internal data buffer.

When the device returns to the ready state ($R\overline{B}$ High), optional readout of data is allowed by pulsing $\overline{R}$ to check ECC (see *Figure 10: Copy back program operation (with readout of data)*).

The next bus write cycle of the command is given to input the target page address. If there is not a bit error data do not need to be reloaded. The next bus write cycle of the command is given to input the target address (85h).

Once the copy back program process starts, the Read Status Register command (70h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the Ready/Busy output, or the status bit (I/O6) of the status

register (commands 70h or F1h). When the copy back program is complete, the write status bit (I/O0) can be checked. The command register remains in read status command mode until another valid command is written to the command register. During the copy back program, data modification is allowed by using the Random Data Input command (85h) as shown in *Figure 11: Copy back program operation with random data input*.

The copy back program operation is only allowed within the same memory plane.

Figure 9. Copy back program operation (without readout of data)

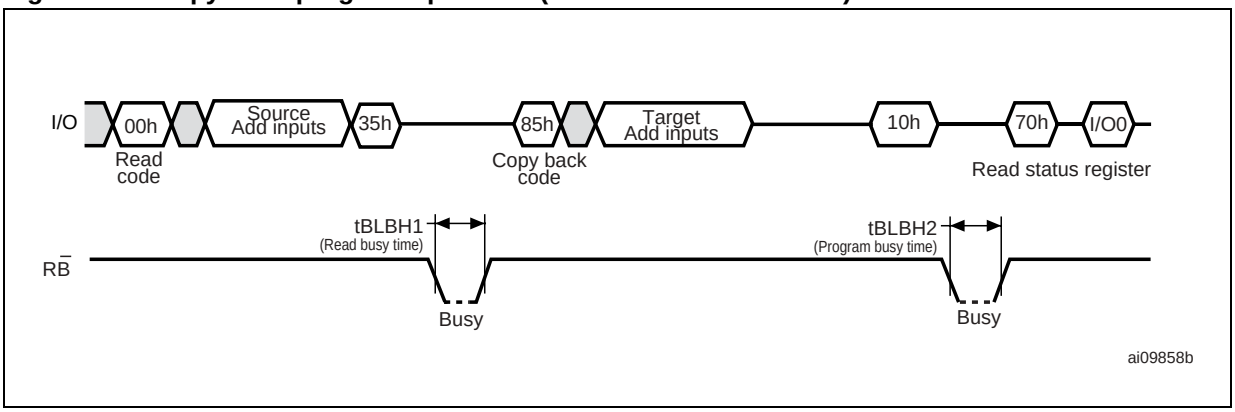


Figure 10. Copy back program operation (with readout of data)

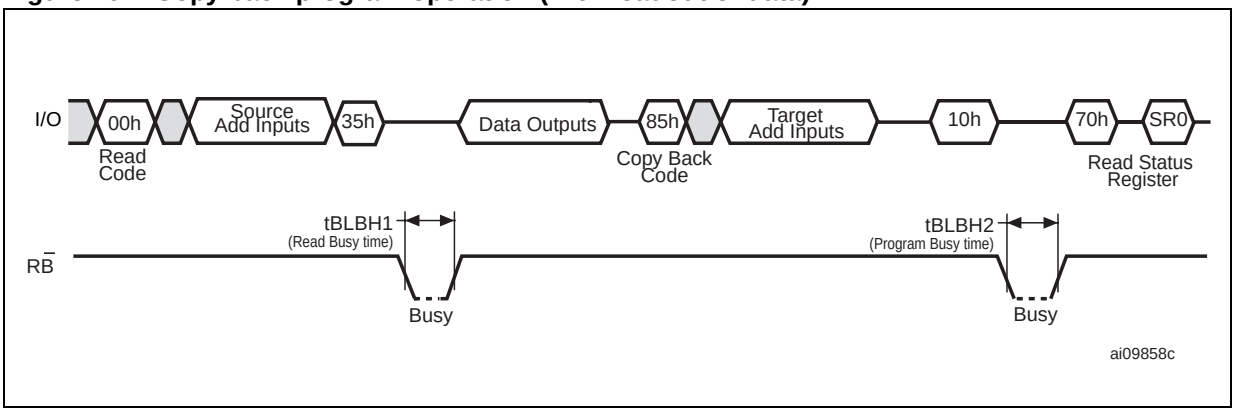
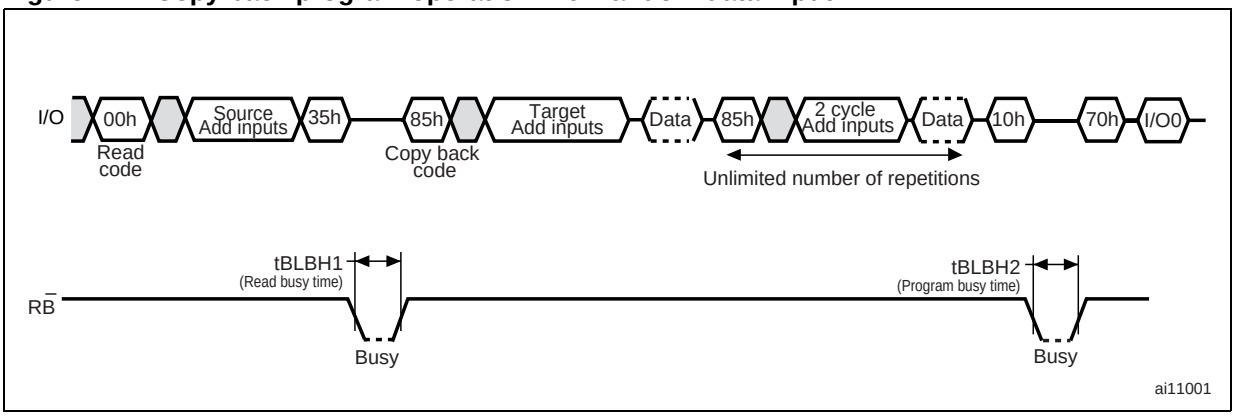


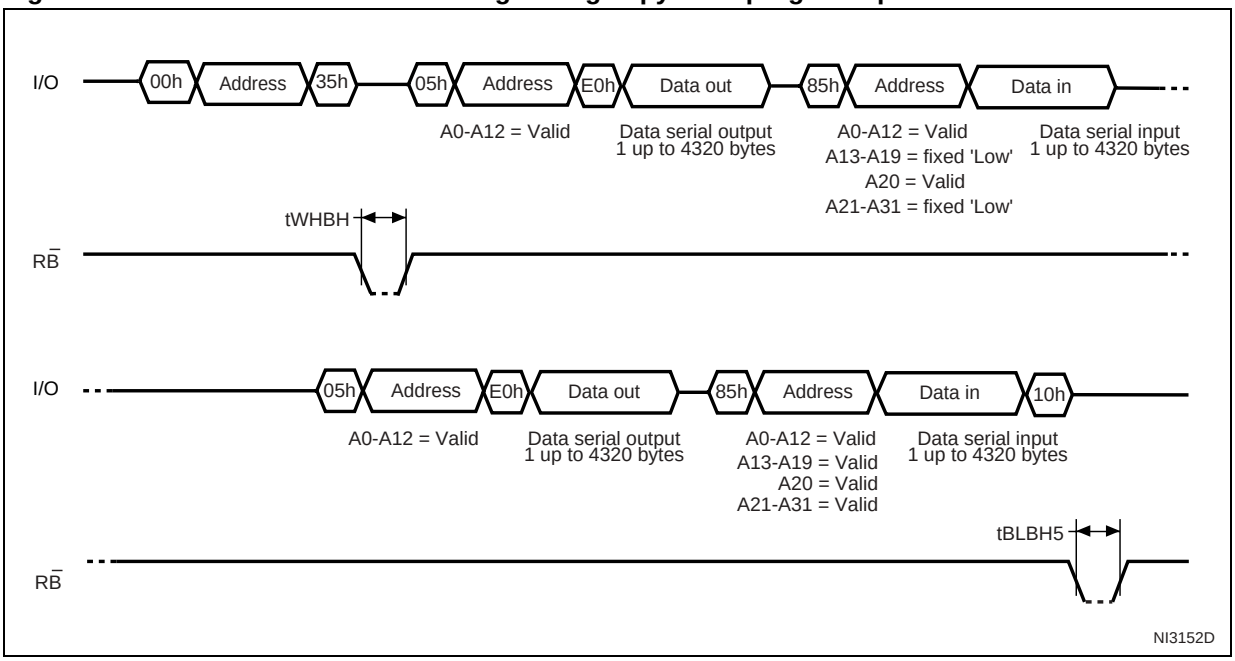
Figure 11. Copy back program operation with random data input



6.1.5 Copy-back program with data out/data in interleaving

The NAND16GW3D2B device allows interleaving of data out and data in during copy back through an extended usage of random data out (05h-E0h) and copy back program setup (85h) commands. Refer to *Figure 12* for the sequence.

Figure 12. Data in/data out interleaving during copy back program operation



6.1.6 Cache read

The cache read operation is an extension of the page read, which is an operation available only within a block. Since the device has one cache register, serial data output can be executed while data in the memory is read into data register.

The cache read operation starts with the page read sequence (00h-30h).

Once the random access to the first page is complete (Ready/Busy signal goes High), the Cache Read command (31h) is latched into the command register. At this time, data of the first page is transferred from the data register to the cache register, while device goes busy for a short time (t_{BLBH6}).

At the end of this phase cache register data can be output by toggling the Read Enable signal while the next page is read from the memory array into data register.

Subsequent pages are read by issuing additional 31h command sequences.

If the serial data output time of one page exceeds random access time (t_{WHBH}), the random access time of the next page is hidden by data downloading of the previous page.

On the other hand, if 31h is issued prior to complete the random access to the next page, the device will stay busy as long as needed to complete random access to this page, transfer its contents into the cache register, and trigger the random access to the following page.

To terminate the cache read operation, the 3Fh command must be issued. This command transfer data from data register to the cache register without issuing next page read.

During the cache read operation, all commands are forbidden except 31h, 3Fh, Read Status Register or Reset (FFh).

To carry out other operations the cache read operation must be ended by issuing the Cache Read End command (3Fh) or by resetting the device with a Reset command (FFh).

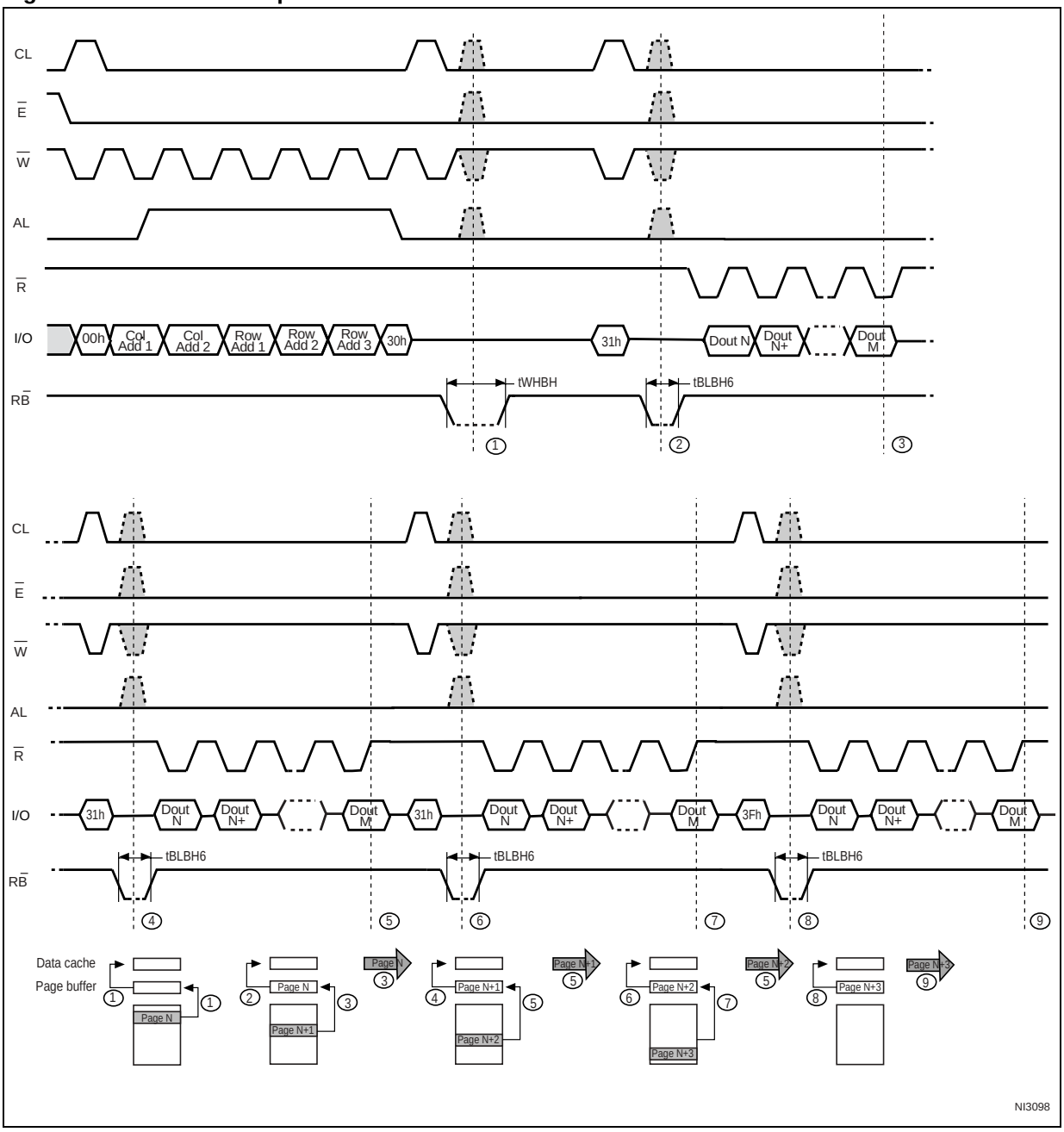
Note: 31h and 3Fh commands reset the column counter, thus when Read Enable ($\overline{R}$) is toggled to output the data of a given page, the first output data is related to the first byte of the page (column address 00h). Random Data Output command can be used to switch the column address.

The Read Status Register command (70h) can be issued to check the status of the different registers, and the ready/busy status of cache read operations. In particular:

1. The cache busy status bit I/O6 indicates when the cache register is ready to output new data
2. The status bit I/O5 is used to determine when the cell reading of the current data register contents is complete

Refer to *Table 12: Multiplane read status register bits (cached operations)* and *Figure 13: Cache read operation* for more details.

Figure 13. Cache read operation



6.1.7 Cache program

The cache program operation is an extension of the standard page program, which is an operation executed with two 4,320-byte registers, data and the cache register.

The cache program operation allows data insertion in one page while program of another page is under execution.

The cache program operation is available only within a block.

Once the Serial Data Input command (80h) is loaded to the command register, followed by 5 address cycles, a full or partial page of data is latched into the cache register.

When the Cache Write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in busy state for a short time (t_{BLBH7}). After all data of the cache register is transferred into the data register, the device returns to ready state, and allows loading next data into the cache register through another cache program command sequence (80h-15h).

The busy time following the first sequence (80h – 15h) equals the time needed to transfer the data of the cache register to the data register. Cell programming of this data and loading of the next data into the cache register is consequently processed through a pipeline model.

In case of any subsequent sequence (80h-15h), the transfer from cache register to data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (t_{BLBH7}).

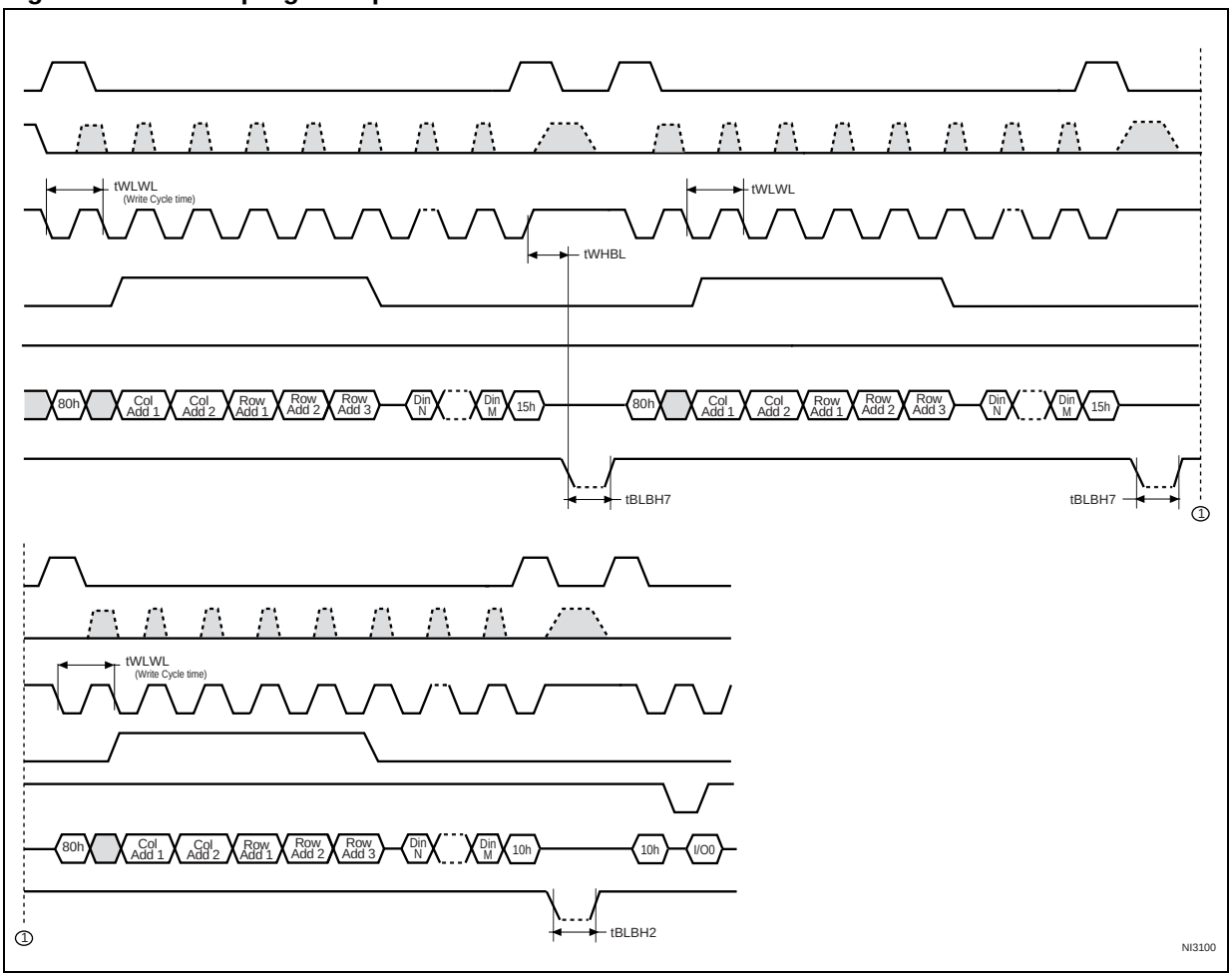
The Read Status Register command (70h) can be issued to check the status of the different registers, and the pass/fail status of the cached program operations. In particular:

1. The cache busy status bit I/O6 indicates when the cache register is ready to accept new data
2. The status bit I/O5 indicates when the cell programming of the current data register contents is complete
3. The cache program error bit I/O1 is used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O6 status bit changing to ‘1’.
4. The error bit I/O0 is used to identify if any error has been detected by the program/erase controller while programming page N. The latter can be polled upon I/O5 status bit changing to ‘1’. I/O1 can be read together with I/O0.

If the system monitors the progress of the operation only with the Ready/Busy signal, the last page of the target program sequence must be programmed with the Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation.

Refer to *Table 12: Multiplane read status register bits (cached operations)* and *Figure 14: Cache program operation* for more details.

Figure 14. Cache program operation



6.2 Multiplane operations

6.2.1 Multiplane page read

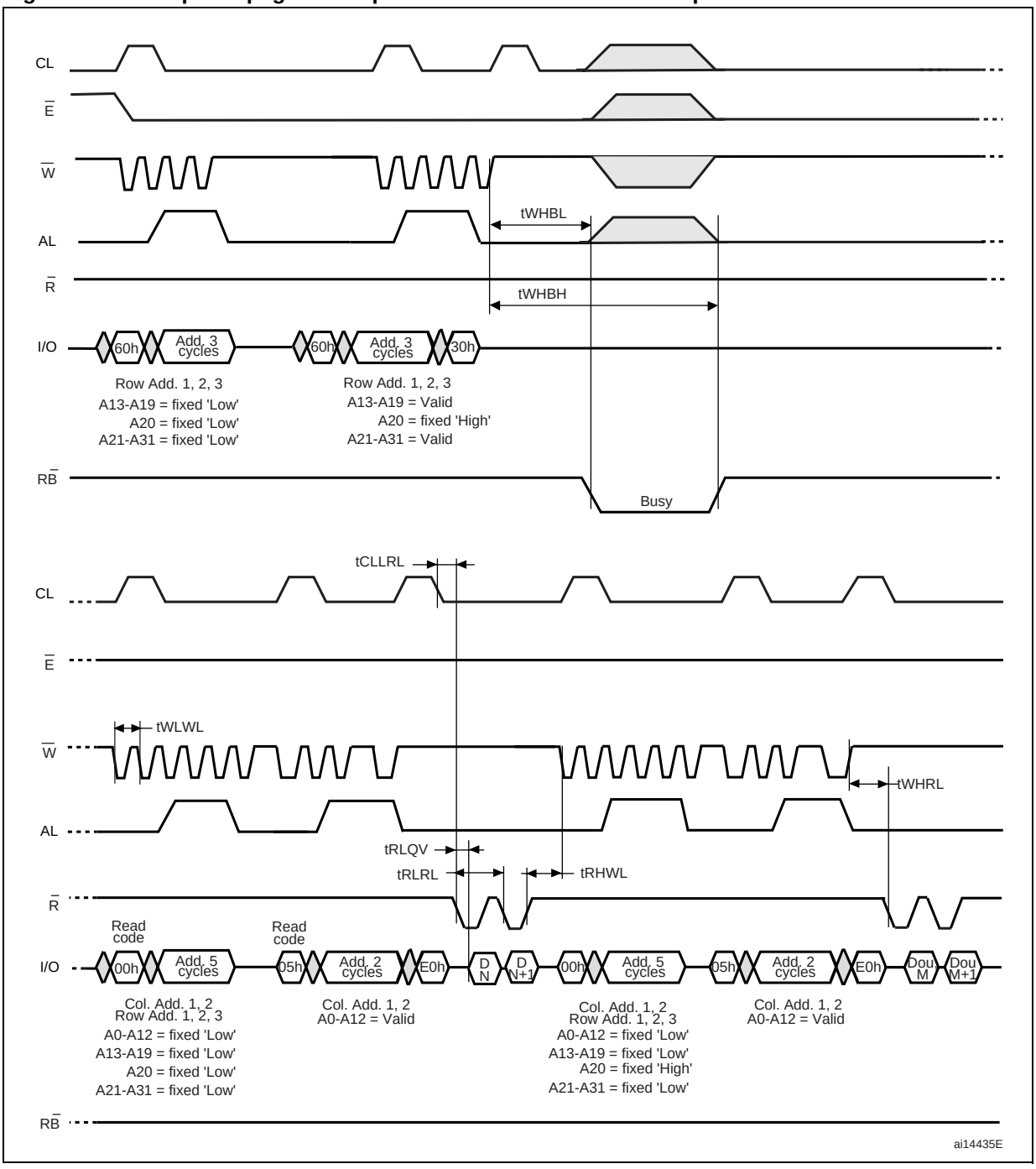
The multiplane page read operation is an extension of a page read operation for a single plane. Since the device is equipped with two memory planes, a random read operation of two pages (one for each plane) is enabled by activating two sets of 4320-byte page registers (one for each plane). The multiplane page read operation is initiated by repeating twice the command 60h followed by three address cycles, and then by a Read Confirm command (30h). In this case only the same page of the same block can be selected from each plane, as shown in *Figure 15: Multiplane page read operation with random data output*.

After the Read Confirm command (30h) the 8640 bytes of data within the selected two pages are transferred to the data registers in a time of t_{WHBH}. The system controller detects the completion of data transfer by either analyzing the output of the Ready/Busy signal, or issuing the Read Status Register commands (70h or F1h) or monitoring IO6 (Ready/Busy) through the Read Enable toggling. In this latter case, the device will output the Read Status until the command 00h is issued.

Once the data is loaded into the data registers, the data of first plane can be read by issuing the command 00h with five address cycles (A20 = Low), followed by the command 05h with two column addresses an then by the command E0h. The data of the second plane can be read using the same command sequence as above, except for A20 = High in the five address cycles.

The multiplane page read operation is also allowed in blocks that have not been programmed with a multiplane page program operation.

Figure 15. Multiplane page read operation with random data output



6.2.2 Multiplane page program

The NAND16GW3D2B device supports multiplane page program, that allows the programming of two pages in parallel, one in each plane.

A multiplane page program operation consists of two steps:

1. Loading of up to two pages of data (8640 bytes) into the data register. The related command sequence is described below:
   - One clock cycle to set up the Serial Data Input command (80h)
   - Five bus write cycles to input the first page address and data. The address of the first page must be within the first plane (A20 = Low)
   - One bus write cycle to issue the dummy page program confirm command (11h). After this the device is busy for a time of t_{BLBH5}
   - When the device returns to the ready state (ready/busy high), a multiplane page program setup code (81h) must be issued, followed by the second page address (5 write cycles) and its serial data input. The address of the second page must be within the second plane (A20 = High), and A19 to A13 must be the address bits loaded during the first address insertion
2. Parallel programming of the two pages of data from the data buffer into the appropriate memory pages. It is started by issuing a Program Confirm command (10h).

Once the multiplane page program operation has started, the status register can be read using the Read Status Register commands (70h or F1h). If the 70h command is used, the status register provides a global information about the operation in both planes (I/O6 = ready/busy, I/O0 = pass/fail). If the F1h is used, the status register provides information about the operation in each plane (I/O0 = global pass/fail, I/O1 = first plane pass/fail; I/O2 = second plane pass/fail).

Only Reset (FFh) or Status Register commands (70h, F1h) can be issued during the busy time t_{BLBH5}.

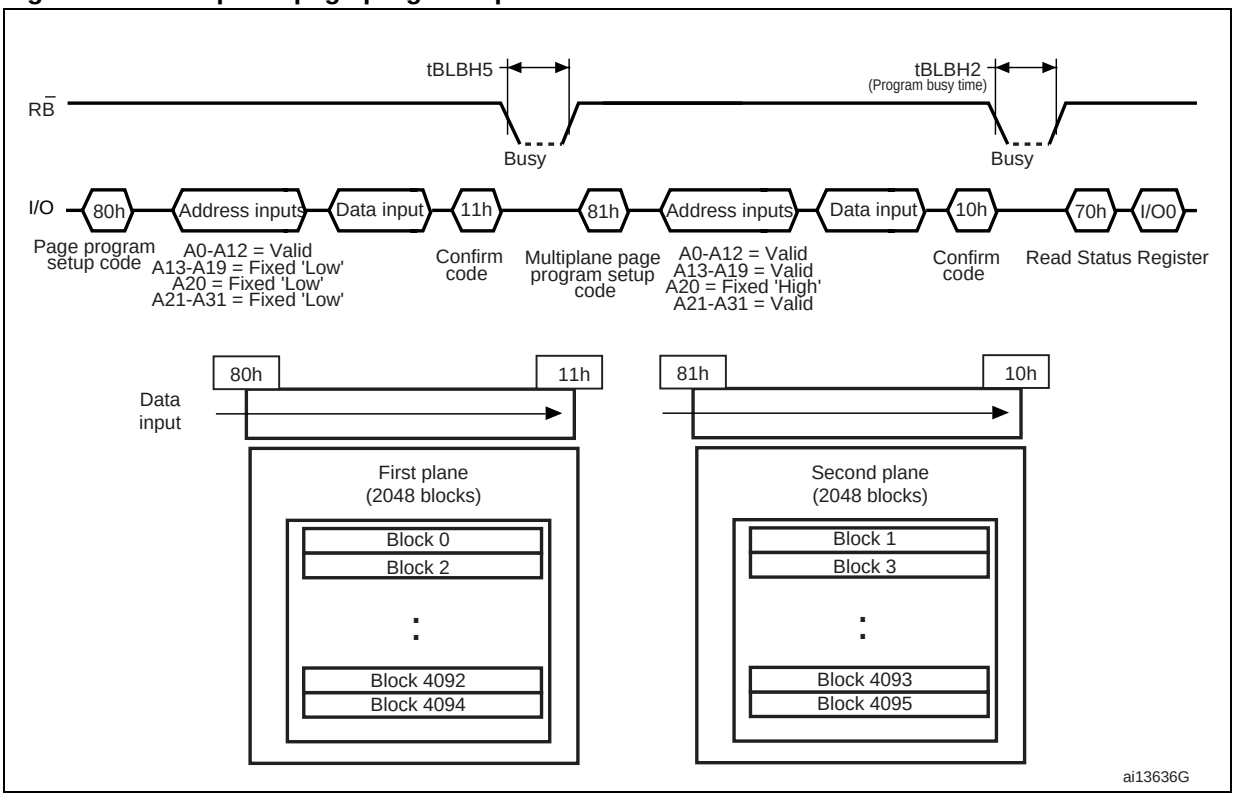
If the multiplane program operation is interrupted by either a power-off or a reset operation, data in the selected pages as well as data in the respective paired pages (refer to *Table 8: Paired page address information*) is no longer valid, as the program algorithm was not executed entirely.

The multiplane page program sequence is shown in *Figure 16: Multiplane page program operation*.

The device supports random data input during both data loading phases, according to the command sequence described in *Section 6.1.2: Page program*.

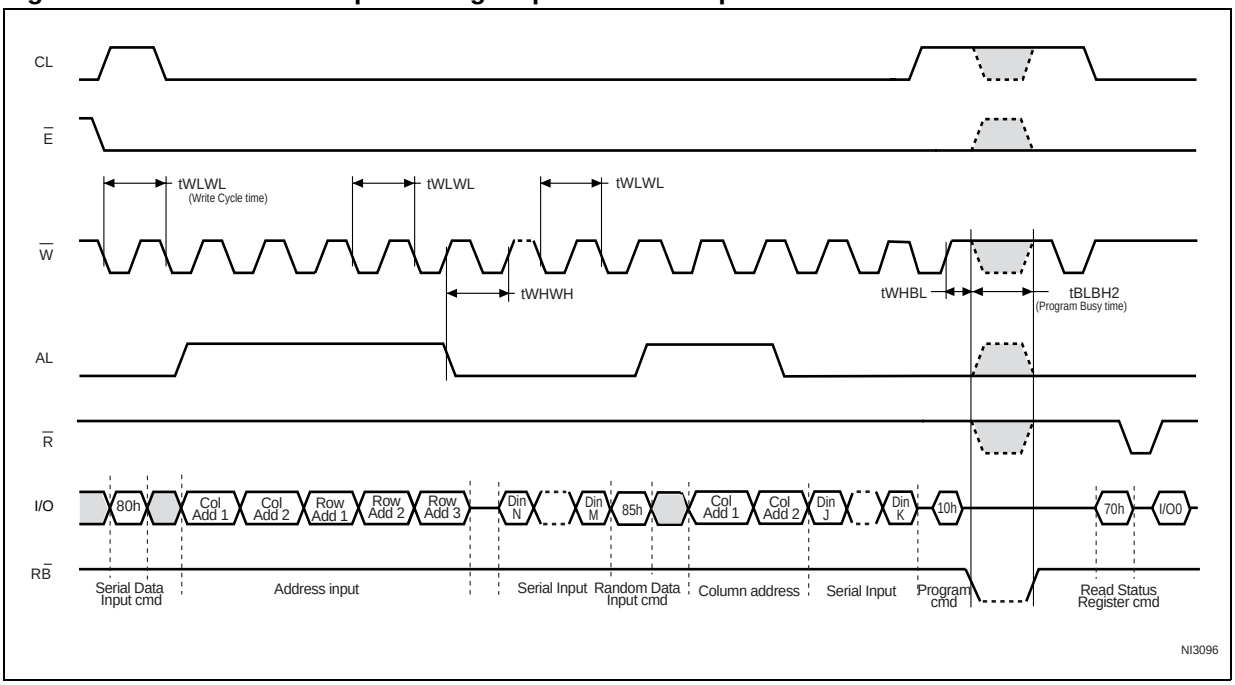
Address limitation applies to multiplane page program operations: page and block address for the pages in the two planes must be the same, as described in *Figure 16: Multiplane page program operation*.

Figure 16. Multiplane page program operation



1. No command between 11h and 81h is permitted except 70h and FFh.

Figure 17. Random data input during sequential data input



6.2.3 Multiplane erase

The multiplane erase operation allows to erase two blocks in parallel, one in each plane (refer to *Figure 18: Multiplane erase operation* for details of the sequence).

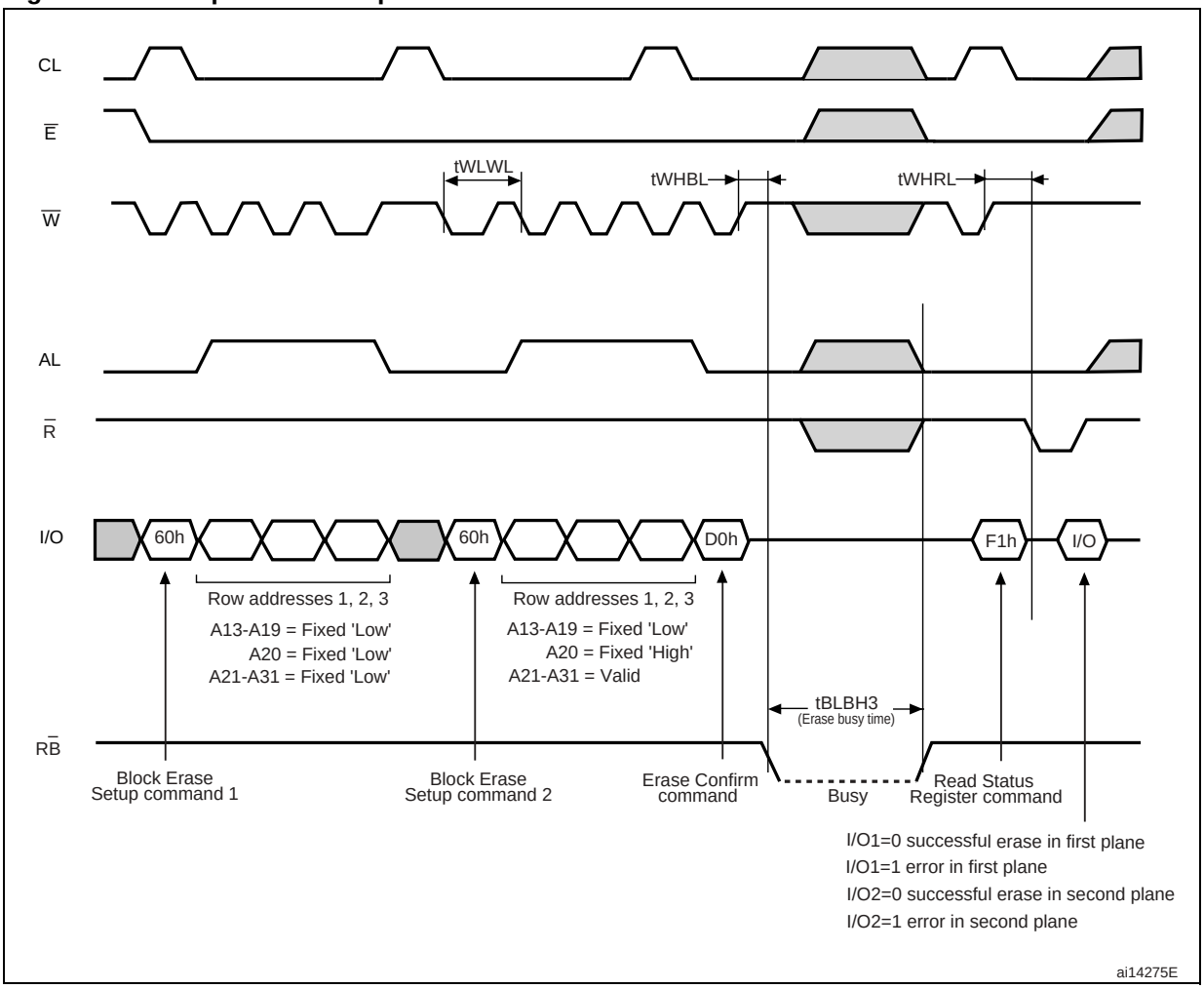
The Block Erase Setup command (60h) must be issued two times, each time followed by the 1st and 2nd block address cycles (3 cycles for each time). As for block erase operation, the Erase Confirm command (D0h) starts this operation. No dummy busy time is required between the first and second block address cycles insertion.

Address limitation applies to multiplane erase: block address for the two planes must be the same.

The multiplane erase operation status can be checked by the Ready/Busy signal or by using the Read Status Register commands (70h or F1h). If the 70h command is used, the status register provides a global information about the operation in both planes (I/O6 = ready/busy, I/O0 = pass/fail). If the F1h is used, the status register provides information about the operation in each plane (I/O0 = global pass/fail, I/O1 = first plane pass/fail; I/O2 = second plane pass/fail).

If the multiplane erase operation is interrupted by either a power-off or a reset operation, data in the selected blocks is no longer valid, as the erase algorithm was not executed entirely.

Figure 18. Multiplane erase operation



6.2.4 Multiplane copy back program

The multiplane copy back program is an extension of the copy back program for a single plane with 4,320 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 4,320 byte page registers enables a simultaneous programming of two pages. The operation consists of two steps:

1. The multiplane read for copy back, where the selection of the source pages occurs by issuing:
   a) the command 60h followed by three address cycles of the source page in the first block (A20 = Low)
   b) the command 60h followed by three address cycles of the source page in the second block (A20 = High)

   Page and block addresses in the two planes must be the same.
   After the Read Confirm command (35h) the 8,640 bytes of data within the selected two pages are transferred to the data registers in a time of t_{WHBH}.

   The system controller detects the completion of this data transfer by either checking the Ready/Busy signal, or issuing the Read Status Register commands (70h or F1h), or monitoring I\O6 (ready/busy) through the Read Enable toggling.

   In the latter case, the device will output the read status until another valid command is written to the command register. Once the data is loaded into the data registers, the data output of the first plane can be read out by issuing the command 00h followed by five address cycles (with A20 = Low), the command 05h with two column address, and then the command E0h. The data output of the second plane can be read out using the identical command sequence (this time with A20 = High). Data do not need to be reloaded if there is not a bit error.
2. The multiplane copy back program. The operation starts by issuing the Page Copy Data Input command (85h) followed by five cycle address cycles for the destination page in the first plane. The address for this page must be within the1st plane (A20 = Low). The device supports random data input exactly as the page program operation. The dummy Page Program Confirm command (11h) stops the 1st page data input and the device becomes busy for a short time (t_{BLBH5}).
   Once the device becomes ready again, 81h command must be issued, followed by the 2nd page address (5 cycles). Address for this page must be within the 2nd plane (A 20 = 1). Again, random data input is allowed during this phase. The Program Confirm command (10h) starts the parallel programming of both pages.

The multiplane copy back program operation status can be checked by the Ready/Busy signal or by using the Read Status Register commands (70h or F1h). If the 70h command is used, the status register provides a global information about the operation in both planes (I/O6 = ready/busy, I/O0 = pass/fail). If the F1h is used, the status register provides information about the operation in each plane (I/O0 = global pass/fail, I/O1 = first plane pass/fail; I/O2 = second plane pass/fail).

Any command between 11h and 81h is prohibited except 70h, F1h and FFh.

Status register commands can be issued during t_{BLBH5} (refer to *Section 6.3: Reset* for further information).

If the multiplane copy back program operation is interrupted by either a power-off or a reset operation, data in the selected pages as well as data in the respective paired pages is no longer valid, as the program algorithm was not executed entirely.

Figure 19: Multiplane copy back program operation shows the details of the command sequence for the multiplane copy back program operation when controllers handle 8 Kbytes of data. In this case, the multiplane copy back program sequence 85h is issued after random data output of the source pages is complete.

Figure 19. Multiplane copy back program operation

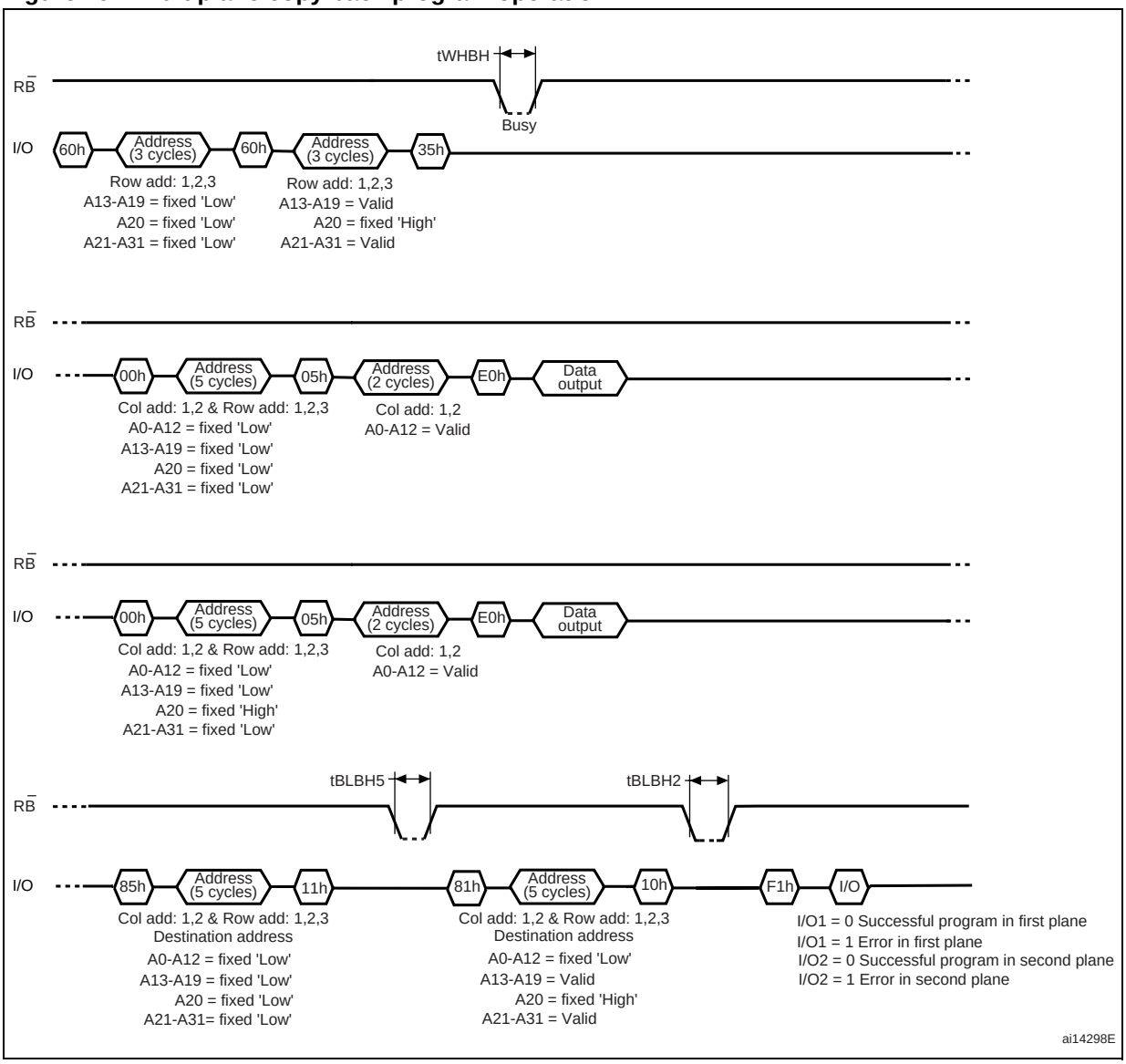


Figure 20. Multiplane copy back program operation with random data input

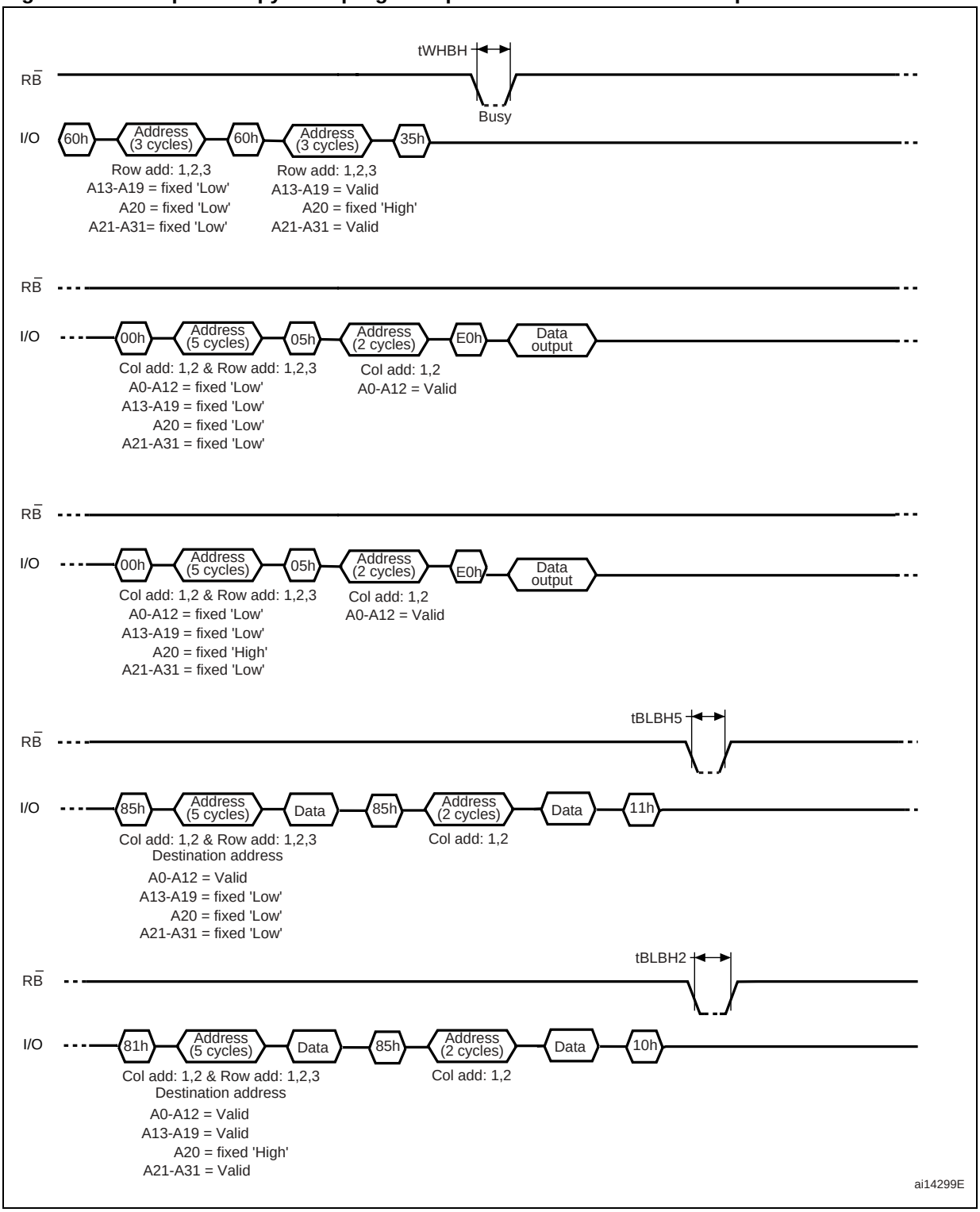
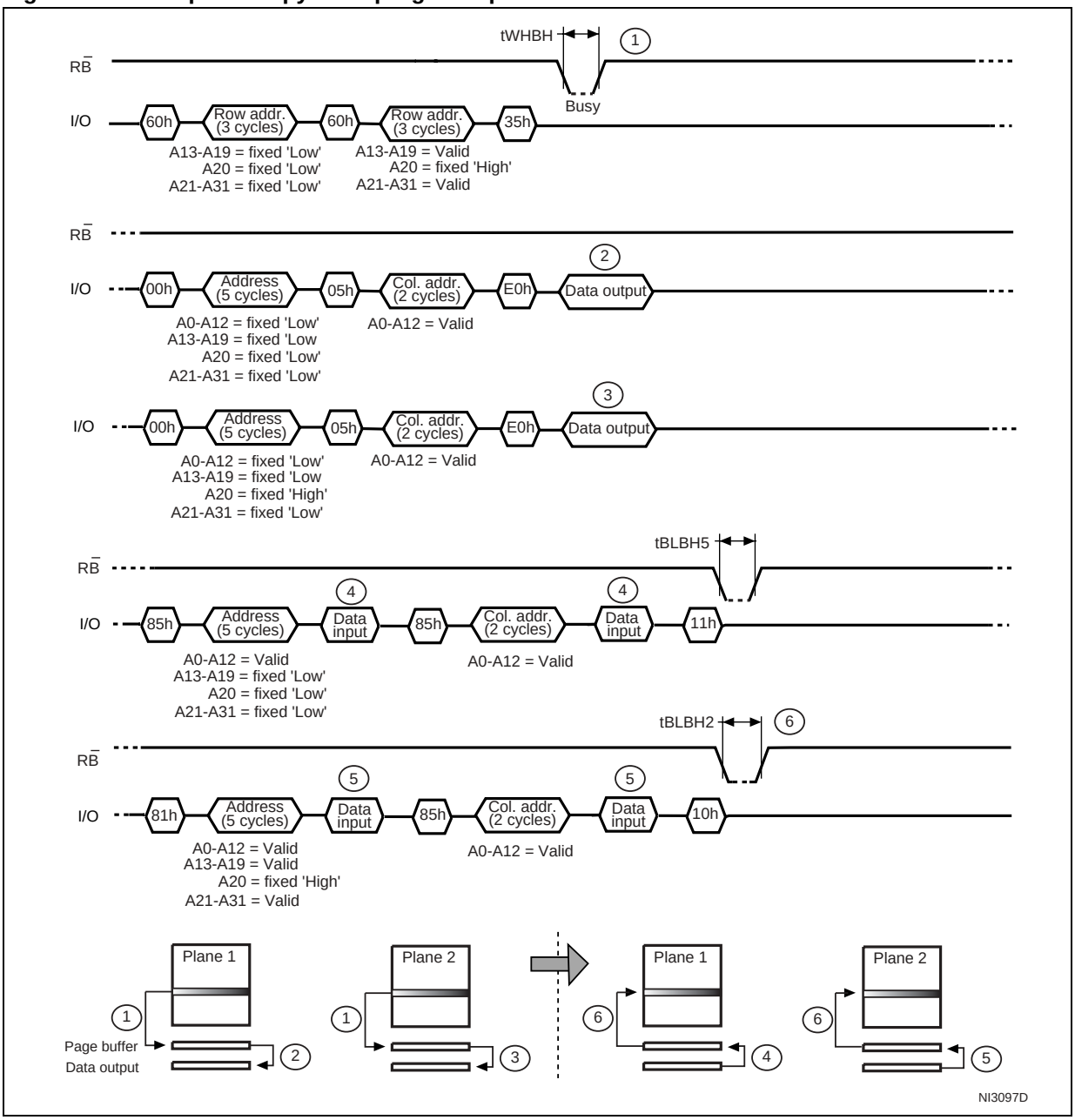


Figure 21. Multiplane copy back program operation

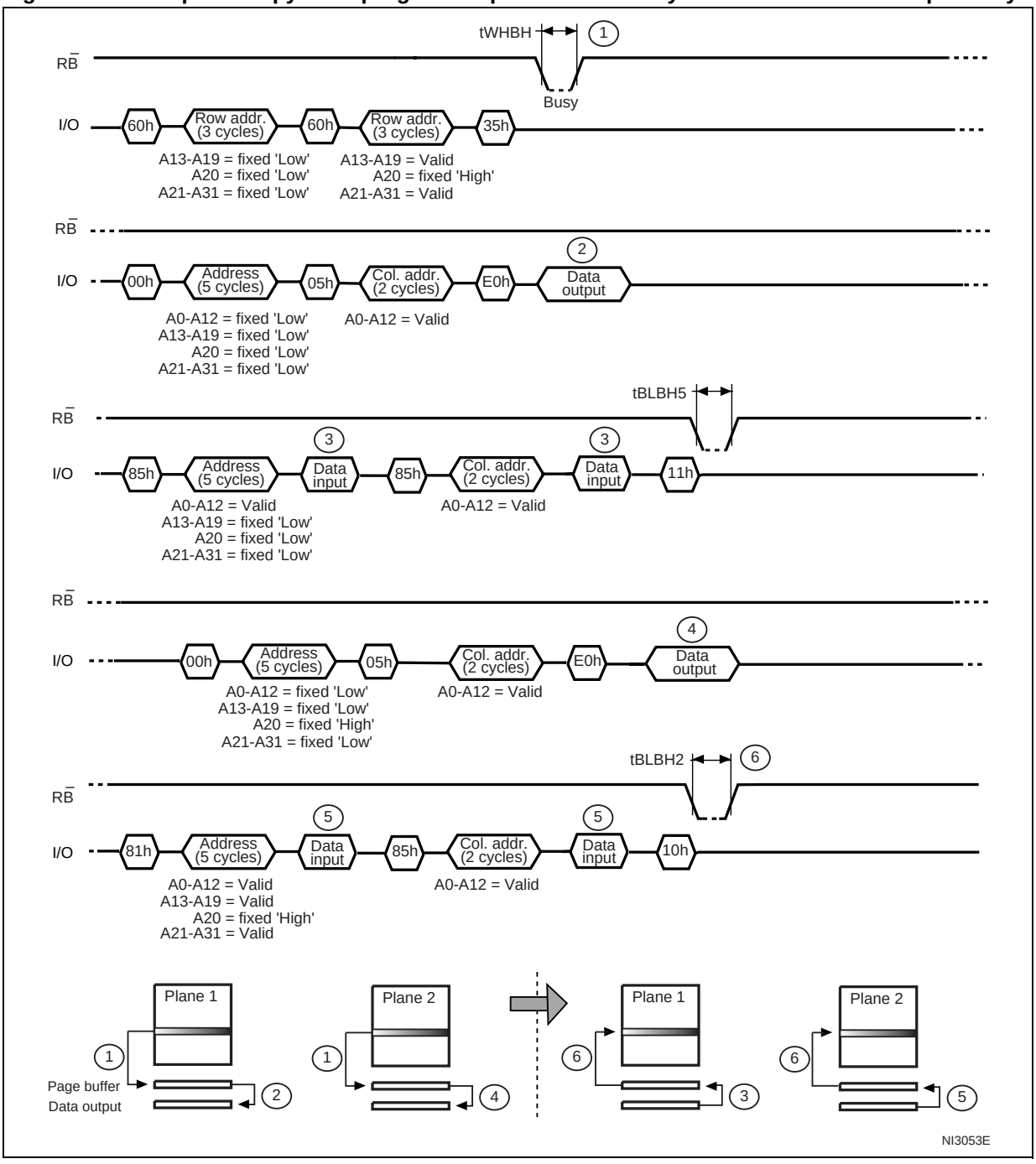


6.2.5 Multiplane copy back program with 4-Kbyte host data buffer compatibility

The devices are made of 4-Kbyte pages and can support two-plane program operation. The internal RAM requirement for a controller is 8 Kbytes, but for controllers which support a RAM of less than 8 Kbytes, the sequence shown in *Figure 22* can be used for two-plane copy back program operation.

In this case the random data input in each plane is started right after finishing the random data output of that plane.

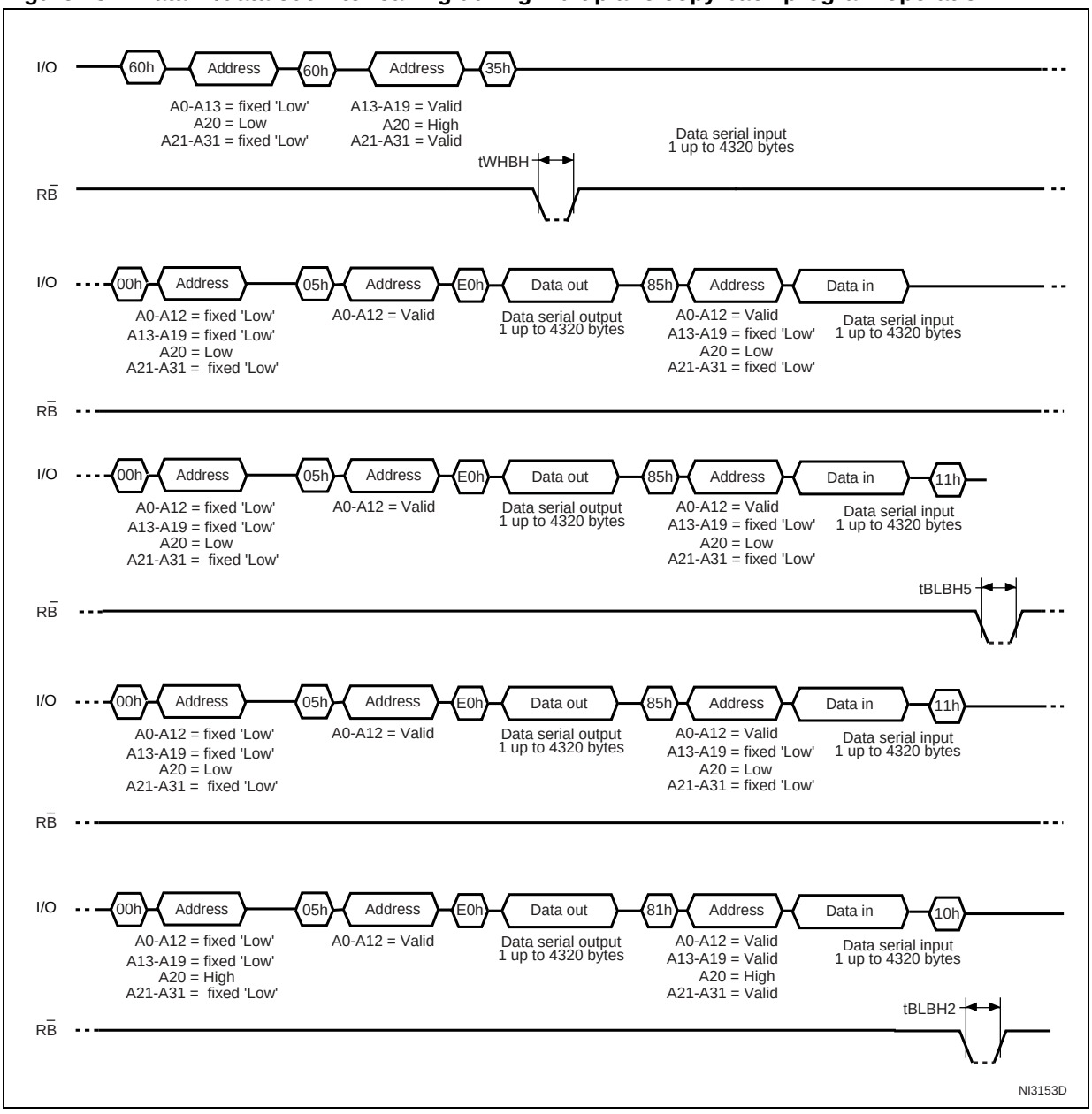
Figure 22. Multiplane copy back program sequence with 4-Kbyte host data buffer compatibility



6.2.6 Multiplane copy back program with data out/data in interleaving

The interleaving of data out and data in is also allowed during multiplane copy back program operations. *Figure 23* shows the sequence:

Figure 23. Data in/data out interleaving during multiplane copy back program operation



6.2.7 Multiplane cache read

The multiplane cache read operation is an extension of the cache read operation, and is available only within two paired blocks belonging to the two planes. Since the device has one cache register in each plane, serial data output from the cache registers of the two planes can be executed while data in the memory is read into the data registers.

The multiplane cache read operation is initiated by the following sequence:

1. 60h command followed by three address cycles of the page of the first plane
2. 60h command followed by three address cycles of the corresponding page of the second plane
3. 33h confirm command.

Once the random access to the first page is complete (Ready/Busy signal goes High), the Multiplane Cache Read command (31h) is latched into the command register. At this time, data of the first page is transferred from the data register to the cache register, while device goes busy for a short time (t_{BLBH5}).

At the end of this phase cache register data of the first page can be output by issuing the following sequence:

1. 00h command followed by the five address cycles related to the first page
2. 05h command followed by two address cycles related to the column address to start the read out
3. E0h command, followed by Read Enable toggling.

The cache register data of the second page can be output by issuing the same sequence:

1. 00h command followed by the five address cycles related to the second page
2. 05h command followed by two address cycles related to the column address to start the read out
3. E0h command, followed by Read Enable toggling.

Subsequent pages are read from the memory array into the data registers by issuing additional 31h command sequences.

If the serial data output time of the two pages exceeds random access time (t_{WHBH}), the random access time of the next pages is hidden by data downloading of the previous pages.

On the other hand, if 31h is issued prior to complete the random access to the next pages, the device will stay busy as long as needed to complete random access to these pages, transfer their contents into the cache register, and trigger the random access to the following pages.

To terminate the multiplane cache read operation, 3Fh command must be issued. This command transfer data from data registers to the cache registers without issuing next page read.

During the multiplane cache read operation, all commands are forbidden except 31h, 3Fh, Read Status Register or Reset (FFh).

To carry out other operations the multiplane cache read operation must be ended by issuing the Multiplane Cache Read End command (3Fh) or by resetting the device with a Reset command (FFh).

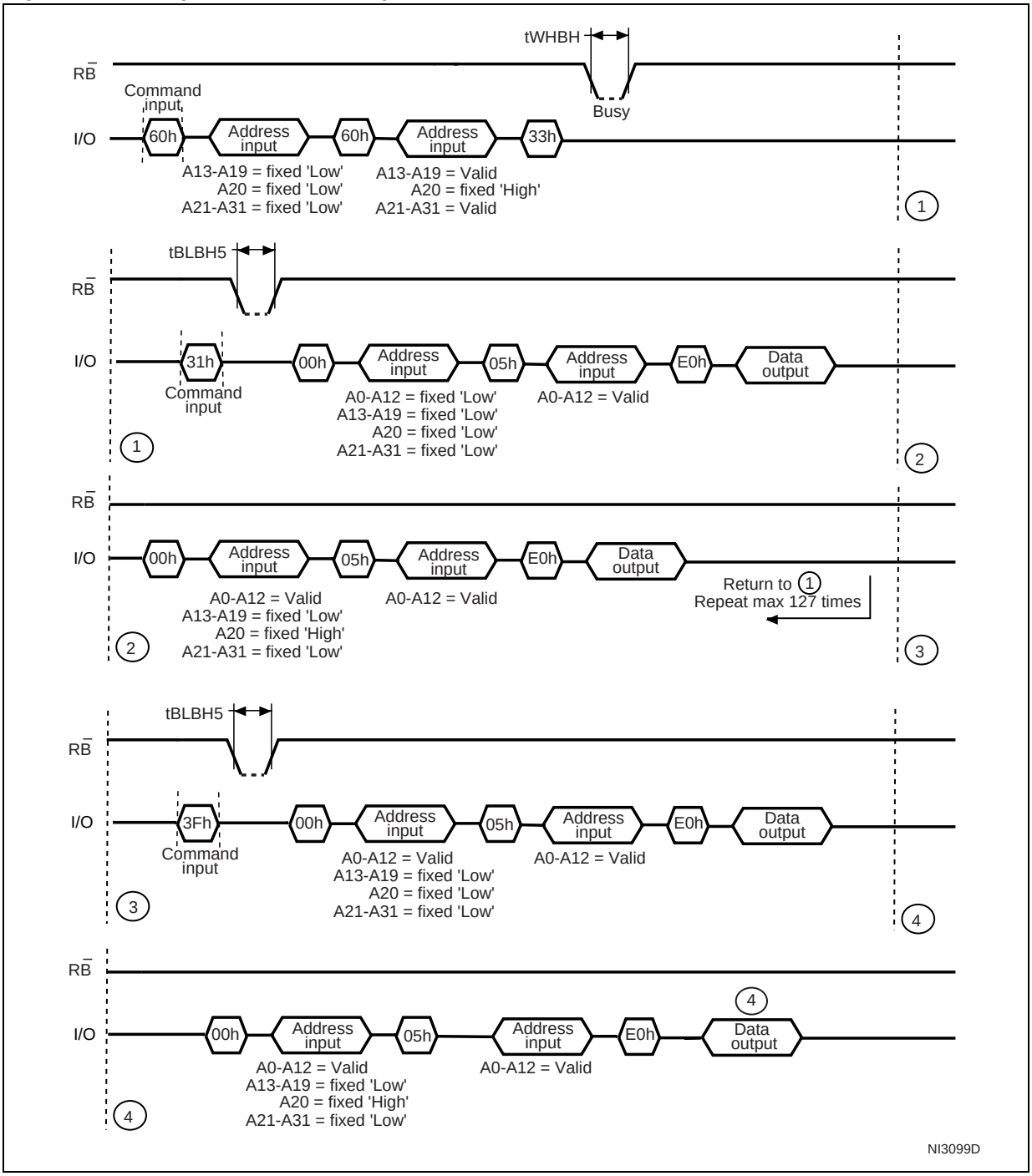
The operation status can be checked with the Ready/Busy pin or with the read status register commands (70h or F1h). In particular:

1. The cache busy status bit I/O6 indicates when both the cache register are ready to output new data
2. The status bit I/O5 indicates when the cell reading of the current data registers is complete

Refer to *Table 11: Multiplane read status register bits (non cached operations)* and *Table 12: Multiplane read status register bits (cached operations)* for more details.

Figure 24: Multiplane cache read operation shows the command sequence for the multiplane cache read operation.

Figure 24. Multiplane cache read operation



6.2.8 Multiplane cache program

The device supports multiplane cache program, which enables high program throughput by programming two pages in parallel while exploiting data and cache registers of both planes to implement cache.

The command sequence can be summarized as follows:

1. The Serial Data Input command (80h) is followed by five cycle address inputs and then by the serial data for the first page. Address for this page must be within the first plane (A20 = Low). The data of the first page other than those to be programmed do not need to be loaded. The device supports random data input exactly like the page program operation
2. The dummy Page Program Confirm command (11h) stops first page data input and the device becomes busy for a short time (t_{BLBH5}).
3. Once the device returns to the ready state again, the 81h command must be issued, followed by the second page address (5 cycles) and its serial data input. Address for this page must be within the second plane (A20 = High). The data of the second page other than those to be programmed do not need to be loaded.
4. Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in busy state for a short time (t_{BLBH7}). After all data of the cache registers are transferred into the data registers, the device returns to ready state, and allows loading the next data into the cache register through another cache program command sequence.

The sequence (80h-...- 11h...-...81h...-...15h) can be repeated at any time. The time t_{BLBH5}, in which the device is busy, allows to complete cell programming of current data registers contents, and to transfer data from cache registers. The sequence to end the multiplane cache program operation is (80h-...- 11h...-...81h...-...10h).

Figure 25: Multiplane cache program operation shows the command sequence for the multiplane cache program operation.

The multiplane cache program operation is available only within two paired blocks belonging to the two planes.

Any command between 11h and 81h is prohibited except 70h, F1h and FFh

The multiplane cache program operation status can be checked by the Ready/Busy signal or by using the Read Status Register commands (70h or F1h). If the 70h command is used, the status register provides a global information about the operation in both planes. In particular:

1. I/O6 indicates when both cache registers are ready to accept new data.
2. I/O5 indicates when the cell programming of the current data registers is complete.
3. I/O1 identifies if the previous pages (pages N-1) in both planes have been successfully programmed or not. The latter can be polled upon I/O6 status bit changing to ‘1’.
4. I/O0 identifies if any error has been detected by the program/erase controller while programming the two pages N. The latter can be polled upon I/O5 status bit changing to ‘1’.

Refer to *Table 12: Multiplane read status register bits (cached operations)* for more details.

If the F1h command is used, the status register provides information about the operation in each of the two planes. In particular:

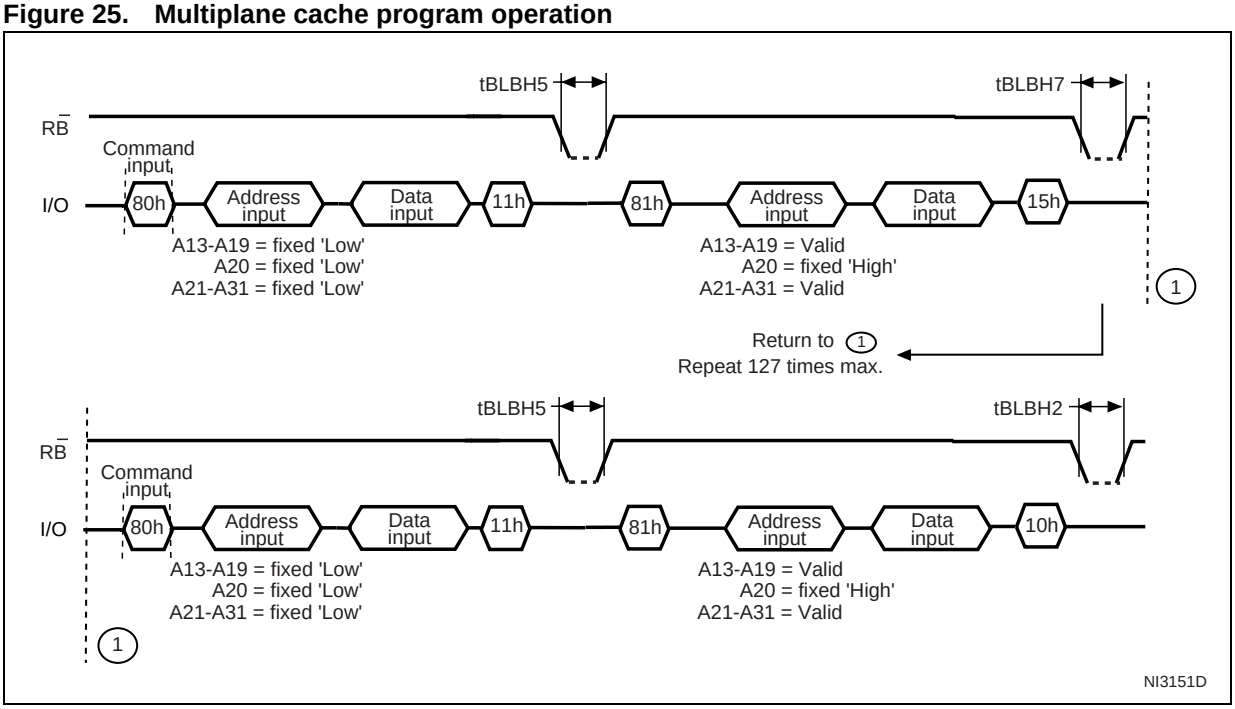
1. I/O6 indicates when both cache registers are ready to accept new data.
2. I/O5 indicates when the cell programming of the current data registers is complete.
3. I/O0 identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O5 status bit changing to ‘1’.
4. I/O1 is the pass/fail flag for current page (N) programming in the first plane. I/O1 can be polled upon I/O5 status bit changing to ‘1’.
5. I/O2 is the pass/fail flag for current page (N) programming in the second plane. I/O2 can be polled upon I/O5 status bit changing to ‘1’.
6. I/O3 is the pass/fail flag for the previous page (N-1) programming in the first plane. I/O3 can be polled upon I/O6 status bit changing to ‘1’.
7. I/O4 is the pass/fail flag for the previous page (N-1) programming in the second plane. I/O4 can be polled upon I/O6 status bit changing to ‘1’.

If the system monitors the progress of the operation only with the Ready/Busy signal, the last pages of the target program sequence must be programmed with a Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O5 must be polled to find out if the last programming is finished before starting any other operation.

If the multiplane cache program operation is interrupted by either a power-off or a reset operation, data in the selected pages is no longer valid, as the program algorithm was not executed entirely.

Refer to *Table 12: Multiplane read status register bits (cached operations)* and to *Section 6.3: Reset* for further information.

Figure 25. Multiplane cache program operation



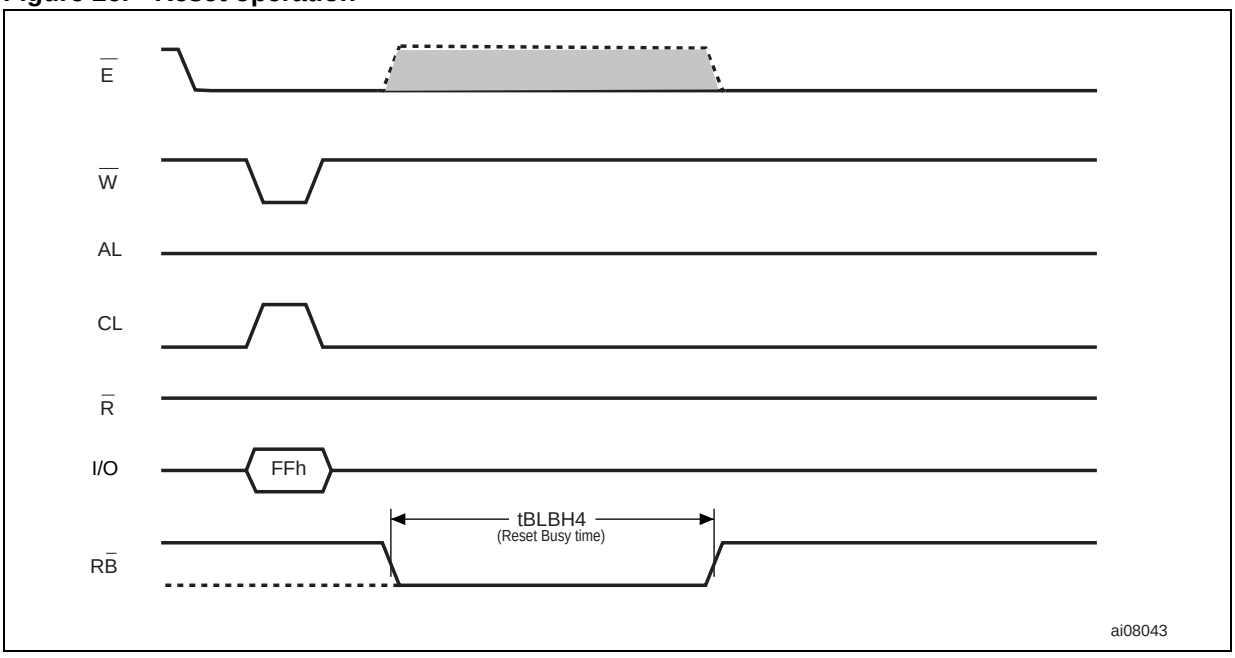
6.3 Reset

The Reset command reset the command interface and status register. If the Reset command is issued during any operation, the operation is aborted. If it is a program or erase operation that is being aborted, the contents of the memory locations being modified are no longer valid as the data is partially programmed or erased. When a reset command is issued during a program operation in busy state, the data in the paired page could become invalid.

If the device is being reset, a new Reset command is not accepted. On the other hand, if the device has completed a reset operation, then a new Reset command is accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued (see *Figure 26: Reset operation*). The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued. Refer to *Table 27: AC characteristics for operations* for the values.

Figure 26. Reset operation



6.4 Read status register

The device contains a status register that provides information on the current or previous read, program or erase operation. The various bits in the status register convey information and errors on the operation.

The status register is read by issuing the Read Status Register command (70h) or the Multiplane Read Status Register command (F1h). The status register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable, or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the status register.

After the Read Status Register command has been issued, the device remains in read status register mode until another command is issued. Therefore, if a Read Status Register command is issued during a random read cycle a new Read command (00h) must be issued to continue with a page read operation.

If the Read Status Register command (70h) is used to check the operation status, the status register provides a global information about the operation in the device. In particular, during a multiplane operation, each status register bit provides a combined information (OR or AND) of the events occurring in the two planes. *Table 9* summarizes the logic function of each status register bit in a multiplane operation.

Table 9. Logic function of read status register bits

Status register bit	Logic combination between planes
I/O0	OR
I/O1	OR
I/O5	AND
I/O6	AND

Table 10 summarizes the meaning of status register bits during standard operations.

Table 10. Read status register bits(1)

I/O	Page read	Page program	Block erase	Cache read	Cache program	Reset	Definition (70h)
0	NA	Pass/fail	Pass/fail	NA	Pass/fail	NA	N page Pass: ‘0’, Fail: ‘1’
1	NA	NA	NA	NA	Pass/fail	NA	N-1 page Pass: ‘0’, Fail: ‘1’
2	NA	NA	NA	NA	NA	NA	–
3	NA	NA	NA	NA	NA	NA	–
4	NA	NA	NA	NA	NA	NA	–
5	Ready/ busy	Ready/busy	Ready/busy	Ready/busy	Ready/busy	Ready/busy	Ready/Busy Busy: ‘0’; Ready:’1’
6	Ready/ busy	Ready/busy	Ready/busy	Ready/busy	Ready/busy	Ready/busy	Data Cache Ready/Busy Busy: ‘0’, Ready: ‘1’
7	Write protect	Write protect	Write protect	Write protect	Write protect	Write protect	Protected: ‘0’ Not protected: ‘1’

1. I/Os defined as NA are recommended to be masked out when read status register is being executed.

If the Multiplane Read Status Register command (F1h) is used to check the operation status, the status register allows to check the outcome of the multiplane operation in each of the two planes.

Table 11 summarizes the meaning of status register bits during multiplane read, multiplane program, multiplane erase operations (non cached operations), while *Table 12* refers to multiplane cache read and multiplane cache program operations (cached operations).

Table 11. Multiplane read status register bits (non cached operations)(1)

I/O	Multiplane read	Multiplane program	Multiplane erase	Definition (F1h)
0	NA	Pass/fail	Pass/fail	Pass: ‘0’, Fail: ‘1’
1	NA	Pass/fail	Pass/fail	First plane Pass: ‘0’, Fail: ‘1’
2	NA	Pass/fail	Pass/fail	Second plane Pass: ‘0’, Fail: ‘1’
3	NA	NA	NA	–
4	NA	NA	NA	–
5	Ready/busy	Ready/busy	Ready/busy	Ready/Busy Busy: ‘0’; Ready:’1’
6	Ready/busy	Ready/busy	Ready/busy	Data Cache Ready/Busy Busy: ‘0’, Ready: ‘1’
7	Write protect	Write protect	Write protect	Protected: ‘0’ Not protected: ‘1’

1. I/Os defined as NA are recommended to be masked out when read status register is being executed.

Table 12. Multiplane read status register bits (cached operations)(1)

I/O	Multiplane cache read	Multiplane cache program	Definition (F1h)
0	NA	Pass/fail	Pass: ‘0’, Fail: ‘1’
1	NA	Pass/fail	N page/First plane Pass: ‘0’, Fail: ‘1’
2	NA	Pass/fail	N page/Second plane Pass: ‘0’, Fail: ‘1’
3	NA	Pass/fail	N-1 page/First plane Pass: ‘0’, Fail: ‘1’
4	NA	Pass/fail	N-1 page/Second plane Pass: ‘0’, Fail: ‘1’
5	Ready/busy	Ready/busy	Ready/Busy Busy: ‘0’; Ready:’1’
6	Ready/busy	Ready/busy	Data Cache Ready/Busy Busy: ‘0’, Ready: ‘1’
7	Write protect	Write protect	Protected: ‘0’ Not protected: ‘1’

1. I/Os defined as NA are recommended to be masked out when read status register is being executed.

6.5 Read electronic signature

The device contains product identification codes. The following three steps are required to read these codes:

1. One bus write cycle to issue the Read Electronic Signature command (90h)
2. One bus write cycle to input the address (00h)
3. Six bus read cycles to sequentially output the data: manufacturer code, device identifier, and 3rd, 4th, 5th, 6th byte (as shown in *Table 14: Electronic signature*).

Table 13. Device identifier codes

Device identifier cycle	Description
1st	Manufacturer code
2nd	Device identifier
3rd	Internal chip number, cell type, number of simultaneously programmed pages, interleaved program, write cache.
4th	Page size, block size, spare size organization
5th	Plane number, ECC level
6th	Technology (Design rule), EDO, interface

Table 14. Electronic signature

Root part number	Byte/word 1	Byte/word 2	Byte 3 *Table 15*	Byte 4 *Table 16*	Byte 5 *Table 17*	Byte 6 *Table 18*
	Manufacturer code	Device code				
NAND16GW3D2B	20h	D5h	94h	25h	44h	41h

Table 15. Electronic signature byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Internal chip number	0 0 0 1 1 0 1 1	1 2 4 Reserved
I/O3-I/O2	Cell type	0 0 0 1 1 0 1 1	2-level cell 4-level cell 8-level cell 16-level cell
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 4 8
I/O6	Interleaved programming between multiple dice	0 1	Not supported Supported
I/O7	Write cache	0 1	Not supported Supported

Table 16. Electronic signature byte 4

I/O	Definition	Value	Description
I/O1-I/O0	Page size (without spare area)	0 0 0 1 1 0 1 1	2 Kbytes 4 Kbytes 8 Kbytes Reserved
I/O7-I/O5-I/O4	Block size (without spare area)	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	128 Kbytes 256 Kbytes 512 Kbytes 768 Kbytes 1 Mbyte Reserved Reserved Reserved
I/O6-I/O3-I/O2	Spare area size	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	128 bytes 224 bytes Reserved Reserved Reserved Reserved Reserved Reserved

Table 17. Electronic signature byte 5

I/O	Definition	Value	Description
I/O1 - I/O0	Reserved	0 0 0	
I/O3 - I/O2	Plane number	0 0 0 1 1 0 1 1	1 plane 2 planes 4 planes 8 planes
I/O6 - I/O5 - I/O4	ECC level	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1 bit/512 bytes 2 bit/512 bytes 4 bit/512 bytes 8 bit/512 bytes 12 bit/512 bytes 15 bit/512 bytes Reserved Reserved
I/O7	Reserved	0	

Table 18. Electronic signature byte 6

I/O	Definition	Value	Description
I/O2 - I/O1 - I/O0	NAND technology	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	48 nm 41 nm Reserved Reserved Reserved Reserved Reserved Reserved
I/O5 - I/O4 - I/O3	Reserved	0 0 0	
I/O6	EDO support	0 1	Not support Support
I/O7	NAND interface	0 1	SDR DDR

7 Data protection and power-on/power-off sequence

The device has hardware features to protect against spurious program and erase operations during power transitions. An internal voltage detector disables all functions whenever the power supply, V_{DD}, is below the threshold $V_{DD} = V_{DDQ} < 2$ V.

V_{DD} and V_{DDQ} as well as V_{SS} and V_{SSQ} are shorted together at any time (see the power-on/power-off sequence in *Figure 27*).

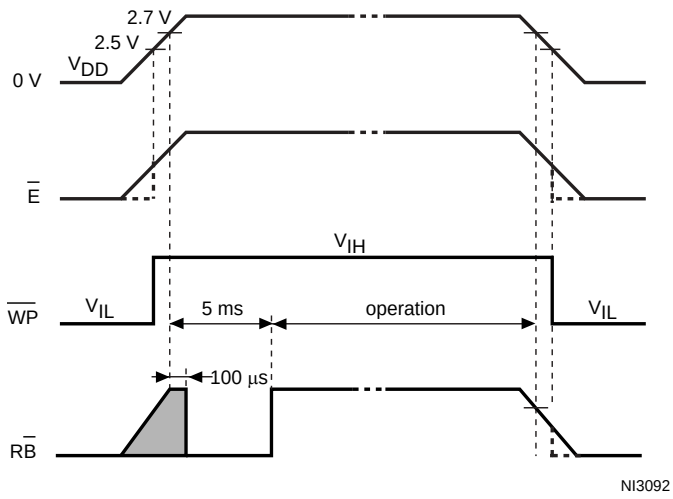
The Ready/Busy signal is valid within 100 µs since the power supplies have reached the minimum values and returns to one within a maximum of 5 ms (see *Table 25: DC characteristics*).

During the busy time at power-on, the device can accept only Read Status Register commands (70h or F1h), while at the end of the busy time, the device is ready to accept any other command sequences.

It is recommended to keep $\overline{WP}$ at V_{IL} during power-on and power-off or whenever $V_{DD} = V_{DDQ} < 2.5$ V, as shown in *Figure 27*.

The $\overline{WP}$ pin should be kept Low (V_{IL}) to guarantee hardware protection during power transitions, as shown in *Figure 27*.

Figure 27. Data protection



8 Power-on sequence and PSL handling

The power-on sequence can be executed in two different ways:

- keeping PSL tied to ground or floating
- keeping PSL tied to power supply.

If PSL is tied to ground, V_{SS}, (or V_{SSQ}) or not connected, the device executes an automatic self initialization during power-on. During this initialization process, the device consumes a current I_{CC0} (30 mA maximum) and keeps the Ready/Busy signal Low for a maximum time of 5 ms. The Ready/Busy signal is valid within 100 µs since the power supplies have reached the minimum values and returns to one within a maximum of 5 ms (see *Table 25: DC characteristics*). During the busy time, the device can accept only Read Status Register commands (70h or F1h), while at the end of the busy time, it defaults into read setup. This means that if the user decides to issue a Page Read command, the 00h command can be skipped (see *Figure 28: Power-on sequence with PSL tied to ground or floating*).

If PSL is tied to V_{DD} (or V_{DDQ}), the device does not complete the self initialization during power-on and does not consume I_{CC0}. The initialization process is executed once a Reset (FFh) command is issued after power-on, and the latter sequence causes the I_{CC0} current consumption. Device operation is guaranteed only after the initialization process is complete, therefore the FFh command must be issued at the end of power-on prior to issuing any command to the device. During this initialization process the device does not accept any command different from Read Status Register (70h or F1h). At the end of the busy time, the device does not default into ‘read setup’. This means that if the user decides to issue a page read, the command 00h must be issued (see *Figure 29: Power-on sequence with PSL tied to power supply*).

Figure 28. Power-on sequence with PSL tied to ground or floating

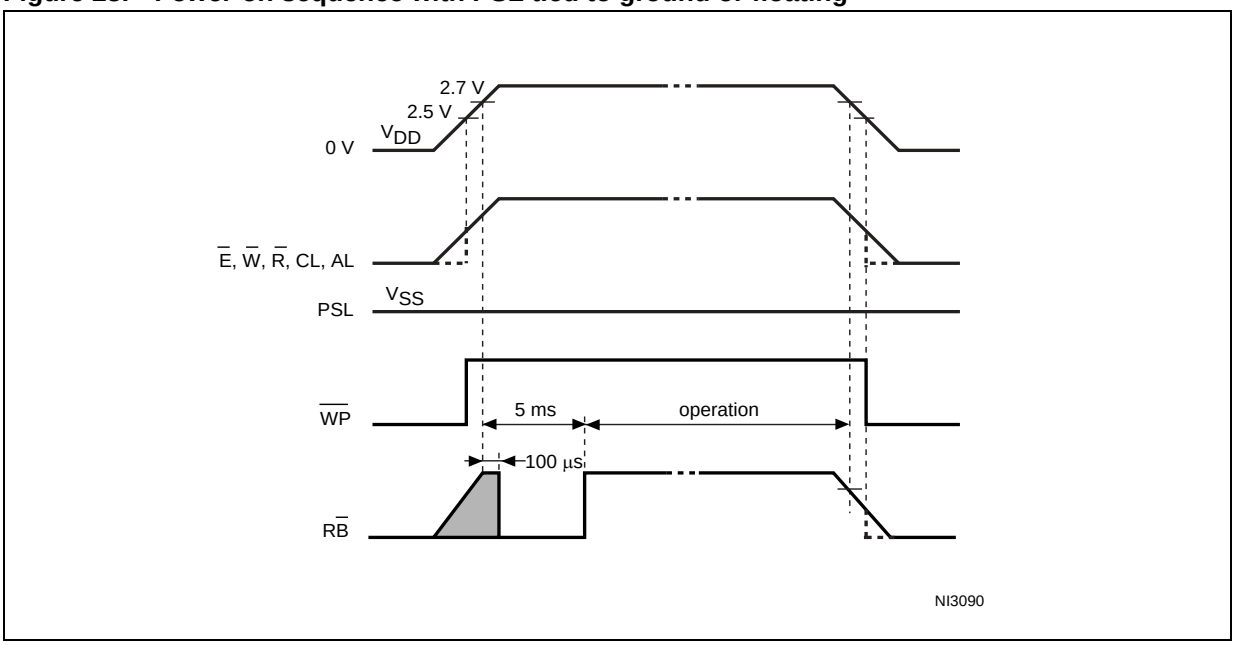
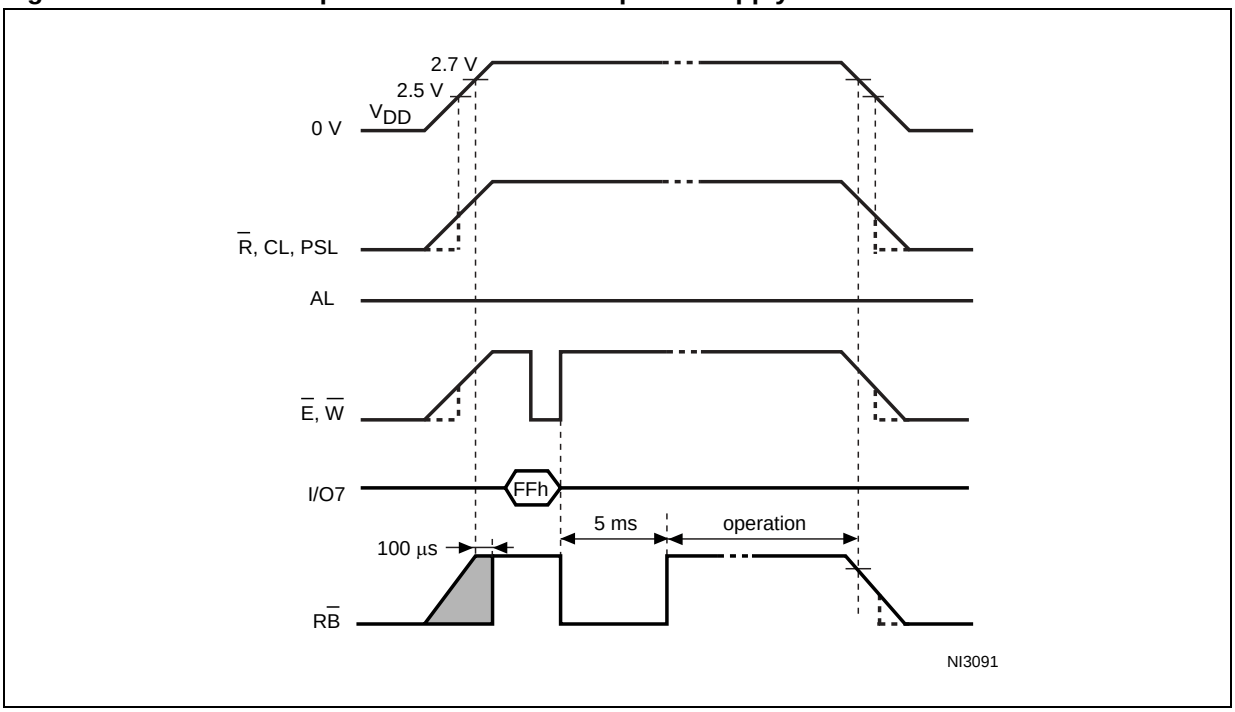


Figure 29. Power-on sequence with PSL tied to power supply



9 Write protect operation

Erase and program operations are automatically reset when $\overline{WP}$ goes Low during busy time and is kept Low for a time t_{VLWH}. Once a program or erase operation is aborted by $\overline{WP}$ driven Low, the contents of the memory locations being modified are no longer valid as the data is partially programmed or erased.

Erase and program operations are enabled and disabled by setting $\overline{WP}$ to High or Low, respectively, prior to issuing the set-up commands (80h or 60h), as shown in *Figure 30*, *Figure 31*, *Figure 32*, and *Figure 33*.

Figure 30. Program enable waveform

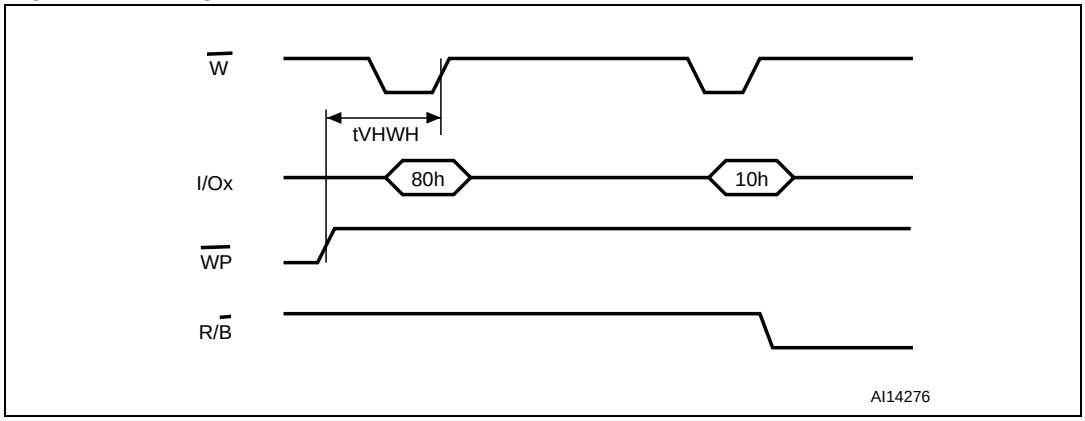


Figure 31. Program disable waveform

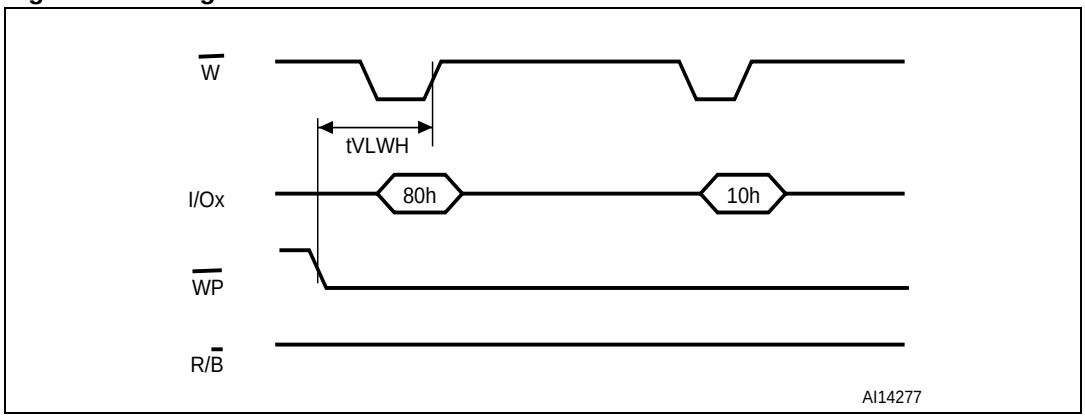


Figure 32. Erase enable waveform

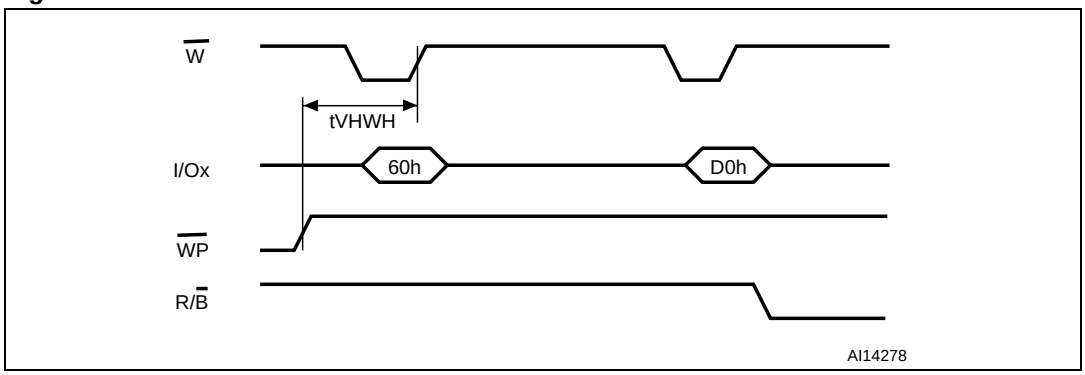
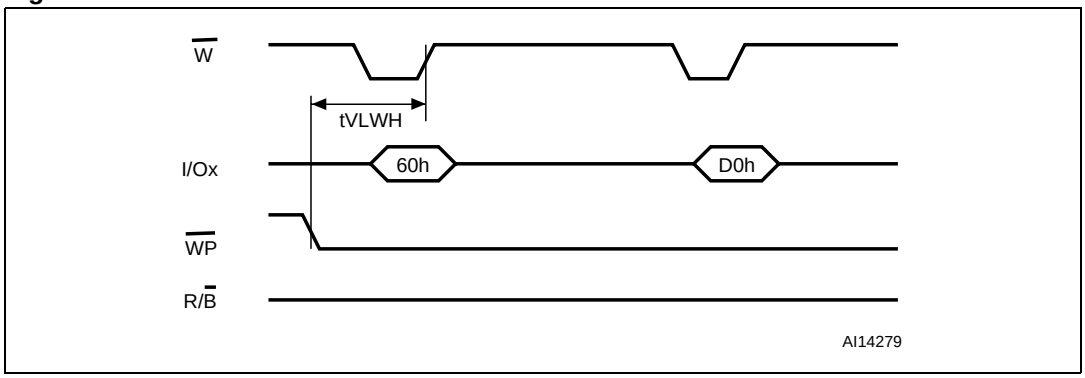
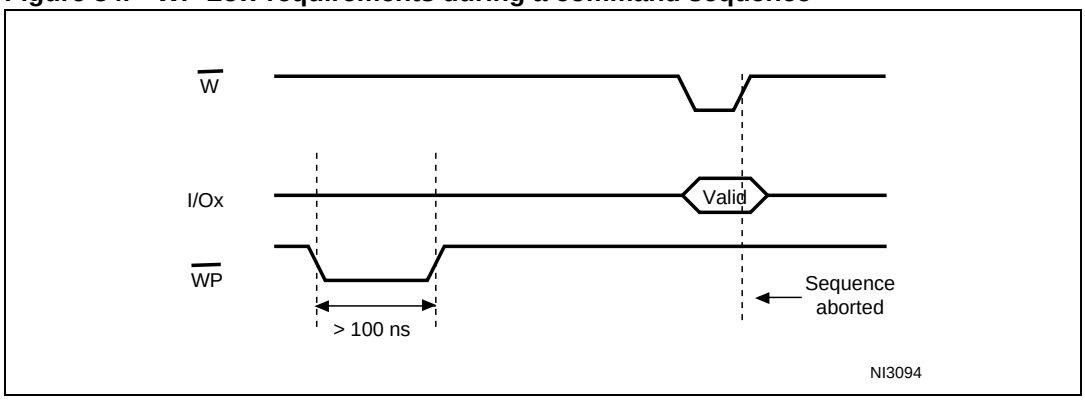


Figure 33. Erase disable waveform



Switching $\overline{WP}$ to V_{IL} during any cycle (command, address or data) of a program or erase command sequence means aborting that command sequence. As specified in *Figure 34*, $\overline{WP}$ Low for more than 100 ns can cause the abort of the command sequence at the first valid $\overline{W}$ pulse (command, address or data).

Figure 34. WP Low requirements during a command sequence



10 Software algorithms

This section provides information on the software algorithms that Numonyx recommends implementing to manage the bad blocks and extend the lifetime of the NAND device.

NAND flash memories are programmed and erased by Fowler-Nordheim tunneling using high voltage. Exposing the device to high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 20: Busy times* for value). To extend the number of program and erase cycles and to increase data retention, it is recommended to implement garbage collection and wear-leveling while the implementation of error correction code algorithms is mandatory.

To help integrate a NAND memory into an application, Numonyx can provide a full range of software solutions: file system, sector manager, drivers, and code management.

Contact the nearest Numonyx sales office or visit www.numonyx.com for more details.

10.1 Bad block management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A bad block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The bad block information is written prior to shipping. Any block, where the 1st byte in the spare area of the last page, does not contain FFh, is a bad block.

The bad block information must be read before any erase is attempted as the bad block Information may be erased. For the system to be able to recognize the bad blocks based on the original information it is recommended to create a bad block table following the flowchart shown in *Figure 35: Bad block management flowchart.*

10.2 NAND flash memory failure modes

The NAND16GW3D2B device may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the devices.

To implement a highly reliable system, all the possible failure modes must be considered:

- Program/erase failure

  in this case, the block has to be replaced by copying the data to a valid block. These additional bad blocks can be identified as attempts to program or erase them and give errors in the status register.

  Because the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back

Program command can be used to copy the data to a valid block. See *Figure 17: Random data input during sequential data input* for more details.

- Read failure

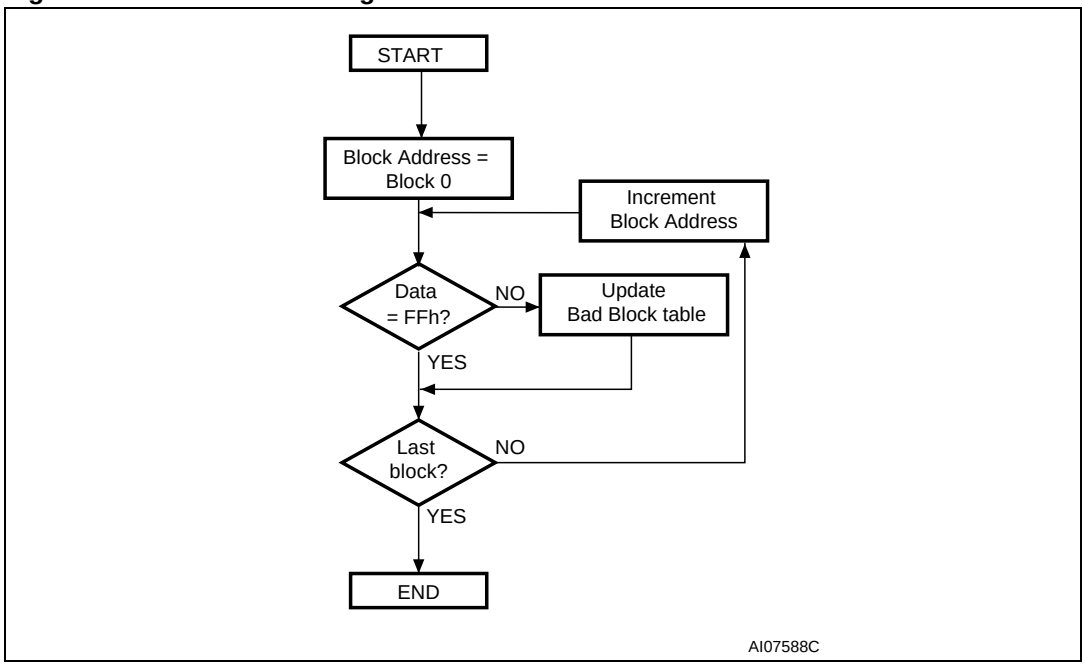
  in this case, ECC correction must be implemented. To efficiently use the memory space, it is recommended to recover single-bit errors in read by ECC, without replacing the whole block.

Refer to *Table 19* for the procedure to follow if an error occurs during an operation.

Table 19. Block failure

Operation	Procedure
Erase	Block replacement
Program	Block replacement or ECC (with 12 bits/512 bytes)
Read	ECC (with 12 bits/512 bytes)

Figure 35. Bad block management flowchart

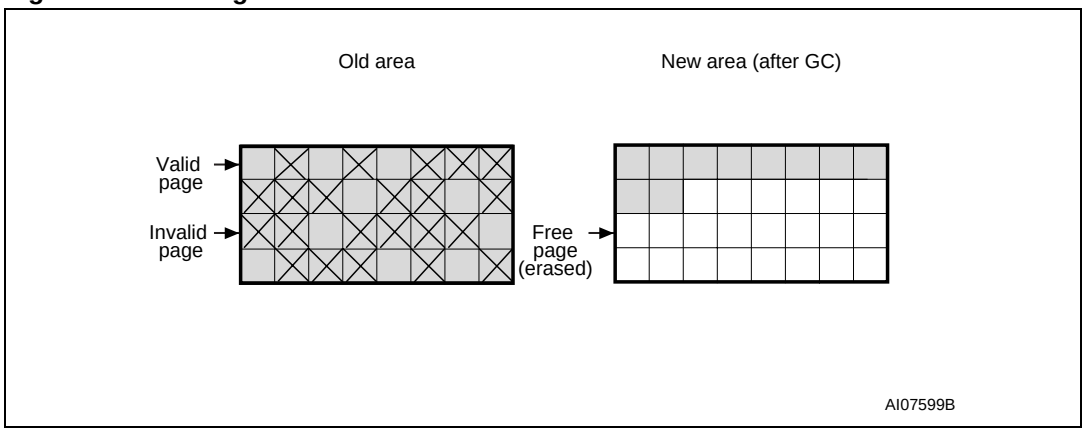


10.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page and mark the previous page as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations, it is recommended to implement a garbage collection algorithm. In a garbage collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 36*).

Figure 36. Garbage collection



10.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a wear-leveling algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a wear-leveling algorithm, not all blocks get used at the same rate. The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each block.

There are two wear-leveling levels:

1. First level wear-leveling, where new data is programmed to the free blocks that have had the fewest write cycles
2. Second level wear-leveling, where long-lived data is copied to another block so that the original block can be used for more frequently changed data.

The second level wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

10.5 Hardware simulation models

10.5.1 Behavioral simulation models

Denali software corporation models are platform-independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND flash devices, and, therefore, allow software to be developed before hardware.

10.5.2 IBIS simulations models

I/O buffer information specification (IBIS) models describe the behavior of the I/O buffers and electrical characteristics of flash devices.

These models provide information such as AC characteristics, rise/fall times, and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

11 Busy times and endurance cycles

Table 20 shows the busy times for 16-Gbit devices while *Table 21* summarizes the number of program/erase cycles per block.

Table 20. Busy times

Parameters	Symbol	Alt. symbol	Max	Unit
Page read, multiplane page read, read for copy back, multiplane read for copy back time (read busy time)	t_{BLBH1}	t_R	60	µs
Page program time (program busy time)	t_{BLBH2}	t_{PROG}	2,000	µs
Cache program time (busy time for cache program operations)	t_{BLBH7}	t_{CBSYW}	2,000	µs
Multiplane program, multiplane cache program, multiplane copy back program time (dummy busy time for multiplane operations)	t_{BLBH5}	t_{DBSY}	1	µs
Cache read, multiplane cache read time (busy time for cache read operations)	t_{BLBH6}	t_{CBSYR}	65	µs
Block erase, multiplane block erase busy time	t_{BLBH3}	t_{BERS}	10	ms
Reset busy time during ready	t_{BLBH4}	t_{RST}	5	µs
Reset busy time during read			5	µs
Reset busy time during program			10	µs
Reset busy time during erase			500	µs

Table 21. Endurance cycles

Parameters	Min	Typ	Max	Unit
Number of partial program cycles (NOP) within the same page (main array or spare array)	–	–	1	cycle
Program/erase cycles (with 12-bit/512-byte ECC)	5,000	–	–	cycles
Data retention	5	–	–	years

12 Maximum ratings

Stressing the device above the ratings listed in *Table 22: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 22. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature (commercial temperature range)	0	70	°C
	Ambient operating temperature (extended temperature range)	– 25	85	°C
	Ambient operating temperature (industrial temperature range)	– 40	85	°C
T_{BIAS}	Temperature under bias	– 50	125	°C
T_{STG}	Storage temperature	– 65	150	°C
V_{IO}(1)	Input or output voltage	– 0.6	4.6	V
V_{DD}	Supply voltage	– 0.6	4.6	V

1. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins.

13 DC and AC parameters

This section summarizes the operating and measurement conditions as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristics tables are derived from tests performed under the measurement conditions summarized in *Table 23: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 23. Operating and AC measurement conditions

Parameter		Min	Max	Unit
Core and input/output supply voltage	V_{DD}	2.7	3.6	V
	V_{DDQ}	2.7	3.6	
Load capacitance (C_L) (1 TTL GATE and C_L)	1.7-1.95 V 2.7-3.6V	50		pF
Input pulses voltages		0	V_{DD}	V
Input and output timing ref. voltages		$V_{DD}/2$		V
Input rise and fall times		5		ns

Table 24. Capacitance(1)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		10	pF
$C_{I/O}$	Input/output capacitance	V_{IL} = 0 V		10	pF

1. T_A = 25 °C, f = 1 MHz.

Table 25. DC characteristics (1)(2)(3)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD0}	Power-on reset current		PSL = GND or NC	–	15	30	mA
			PSL = V_{DD}, FFh command input after power-on	–	15	30	mA
I_{DD1}	Operating current	Read	t_{RLRL} = 25 ns $\overline{E}$ = V_{IL}, I_{OUT} = 0 mA	–	15	30	mA
I_{DD2}		Program	–	–	15	30	mA
I_{DD3}		Erase	–	–	15	30	mA
I_{DD4}	Standby current (TTL)(4)		E = V_{IH}, $\overline{WP}$ = 0/V_{DD}			1	mA
I_{DD5}	Standby current (CMOS)(4)		$\overline{E}$ = V_{DD}-0.2, $\overline{WP}$ = 0/V_{DD} PSL = 0 V/V_{DD}/NC	–	10	50	µA
I_{LI}	Input leakage current		V_{IN} = 0 to 3.6 V	–	–	±10	µA
I_{LO}	Output leakage current		V_{OUT} = 0 to 3.6 V	–	–	±10	µA
V_{IH}	Input high voltage		–	0.8 x V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–	-0.3	–	0.2 x V_{DD}	V
V_{OH}	Output high voltage level		I_{OH} = -400 µA	2.4	–	–	V
V_{OL}	Output low voltage level		I_{OL} = 2.1 mA	–	–	0.4	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.4 V	8	10	–	mA

1. All V_{DDQ} and V_{DD} pins, and all V_{SS} and V_{SSQ} pins are shorted together.
2. Values listed in this table refer to the entire voltage range V_{DD} = V_{DDQ} = 2.7 to 3.6 V and to a single device. For stacked devices, the standby and leakage currents are the sum of the standby and leakage currents of all the chips, while the active power consumption depends on the number of chips concurrently executing different operations.
3. All measurements have been performed with a 0.1 µF capacitor connected between the V_{DD} supply voltage pin and the V_{SS} ground pin.
4. Standby current measurements are performed after the device has completed the initialization process at power-on (see *Section 8: Power-on sequence and PSL handling*).

Table 26. AC characteristics for command, address, data input

Symbol	Alt. symbol	Parameter			$V_{DD}=V_{DDQ}=3.3$ V	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable High	AL setup time	Min	12	ns
t_{ALHWH}		Address Latch High to Write Enable High				
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable High	CL setup time	Min	12	ns
t_{CLLWH}		Command Latch Low to Write Enable High				
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data setup time	Min	12	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable High	$\overline{E}$ setup time	Min	20	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL hold time	Min	5	ns
t_{WHALL}		Write Enable High to Address Latch Low				
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	5	ns
t_{WHCLL}		Write Enable High to Command Latch Low				
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data hold time	Min	5	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ hold time	Min	5	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High hold time	Min	10	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ pulse width	Min	12	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write cycle time	Min	25	ns
t_{RHWL}	t_{RHW}	Read Enable High to Write Enable Low		Min	100	ns

Table 27. AC characteristics for operations

Symbol	Alt. symbol	Parameter			$V_{DD}=V_{DDQ}=3.3$ V	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read electronic signature	Min	10	ns
t_{ALLRL2}			Read cycle	Min	10	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	ns
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	30	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	25	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High hold time	Min	10	ns
t_{EHQX}	t_{COH}	Chip Enable High to Output Hold		Min	15	ns
t_{RHQX}	t_{RHOH}	Read Enable High to Output Hold		Min	15	ns
t_{RLQX}	t_{RLOH}	Read Enable Low to Output Hold (EDO mode)		Min	5	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z		Max	100	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable pulse width	Min	12	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read cycle time	Min	25	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable access time	Max	20	ns
			Read ES access time(1)			
t_{WHBH}	t_{R}	Write Enable High to Ready/Busy High	Read busy time	Max	60	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	80	ns
t_{RHWL}	t_{RHW}	Read Enable High to Write Enable Low		Min	100	ns
t_{WHWH}(2)	t_{ADL}	Last Address Latched on Data Loading time during program operations		Min	70	ns
t_{VHWH}	t_{WW}	Write protection time(3)		Min	100	ns
t_{VLWH}				Min	100	ns

1. ES = electronic signature.
2. t_{WHWH} is the delay from Write Enable rising edge during the final address cycle to Write Enable rising edge during the first data cycle.
3. $\overline{WP}$ High to $\overline{W}$ High during program/erase enable operations or $\overline{WP}$ Low to $\overline{W}$ High during program/erase disable operations.

Figure 37. Command Latch AC waveforms

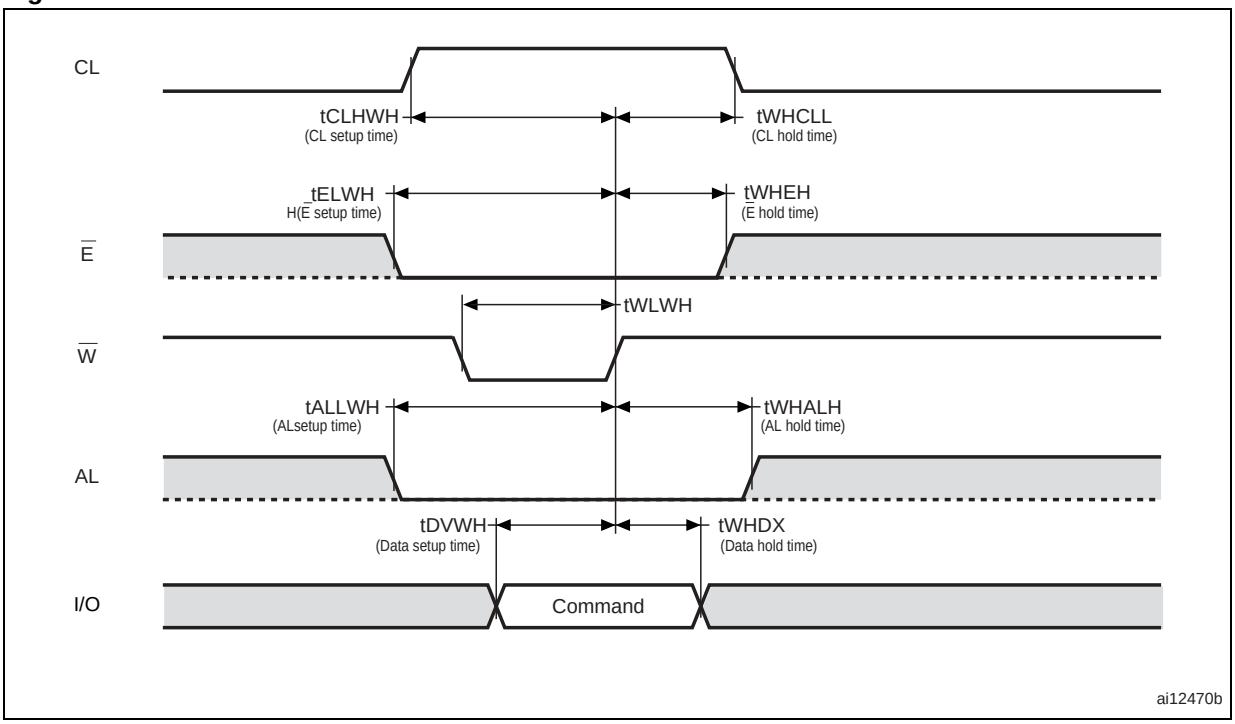


Figure 38. Address Latch AC waveforms

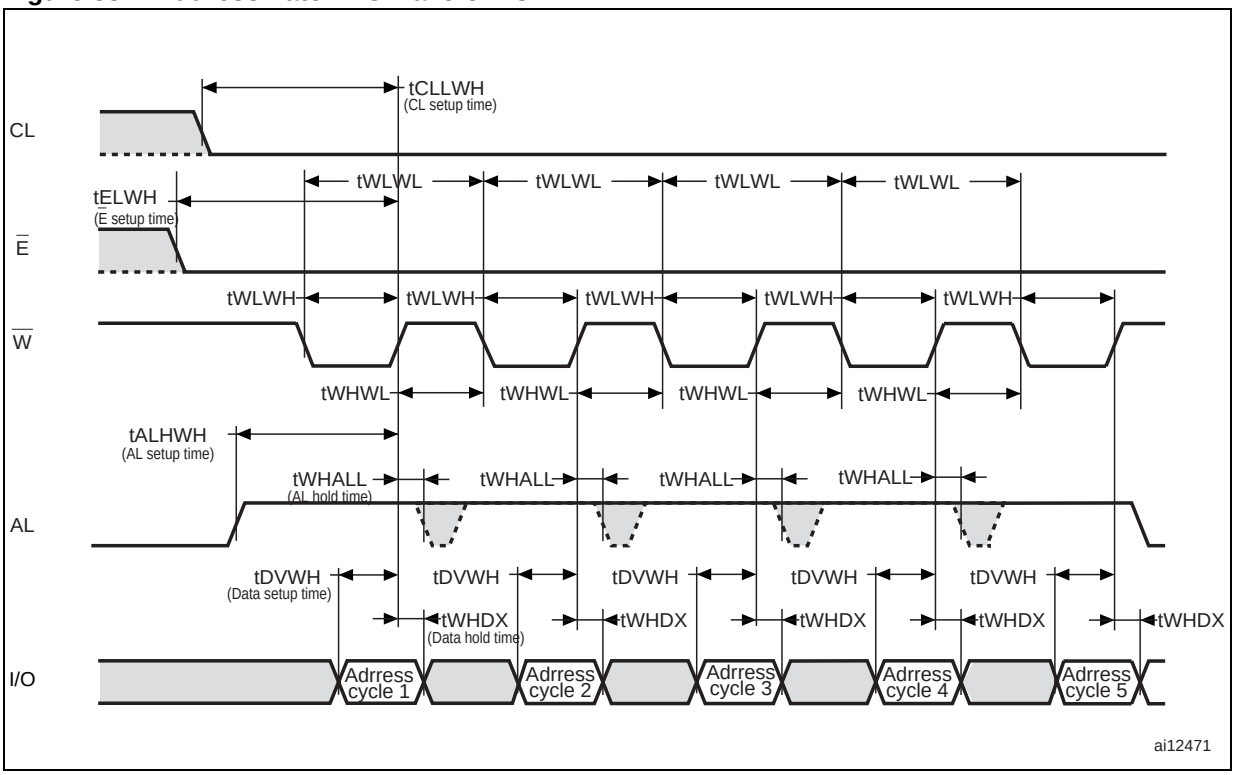


Figure 39. Data Input Latch AC waveforms

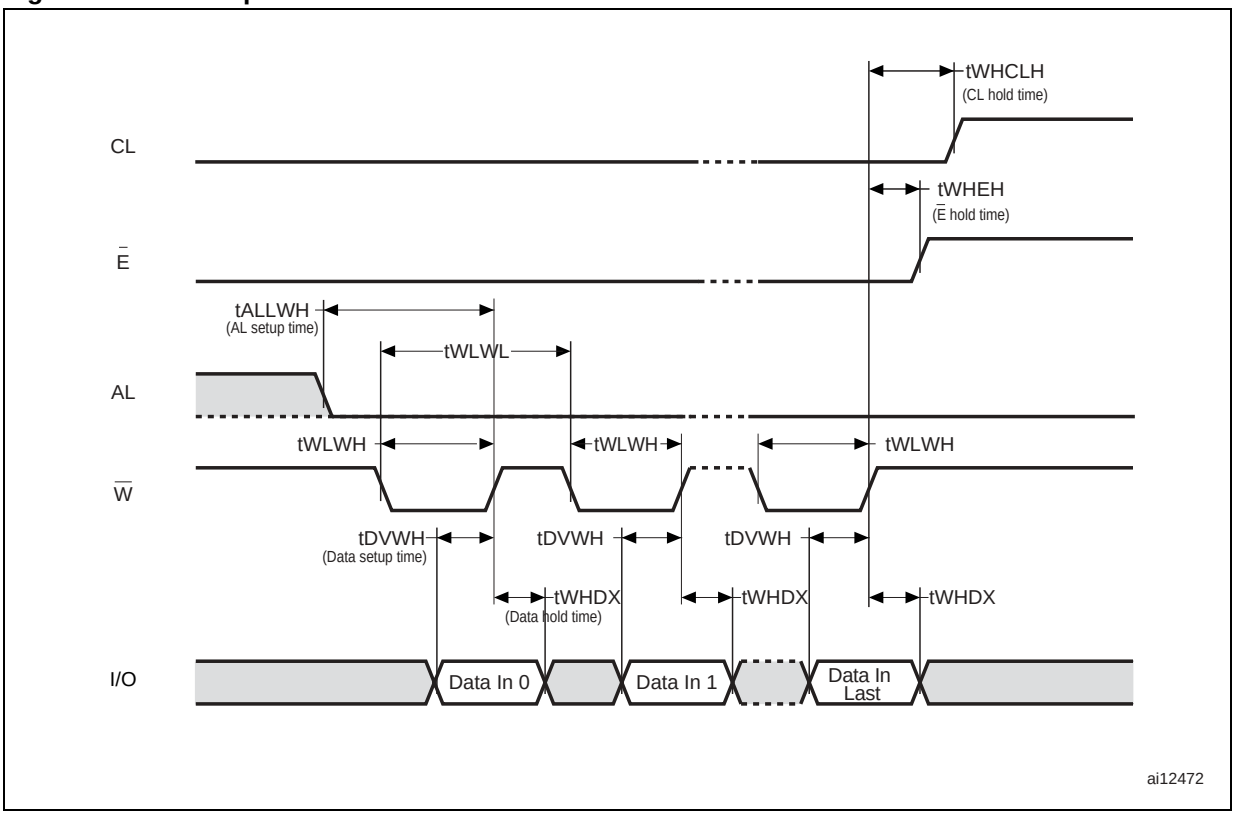
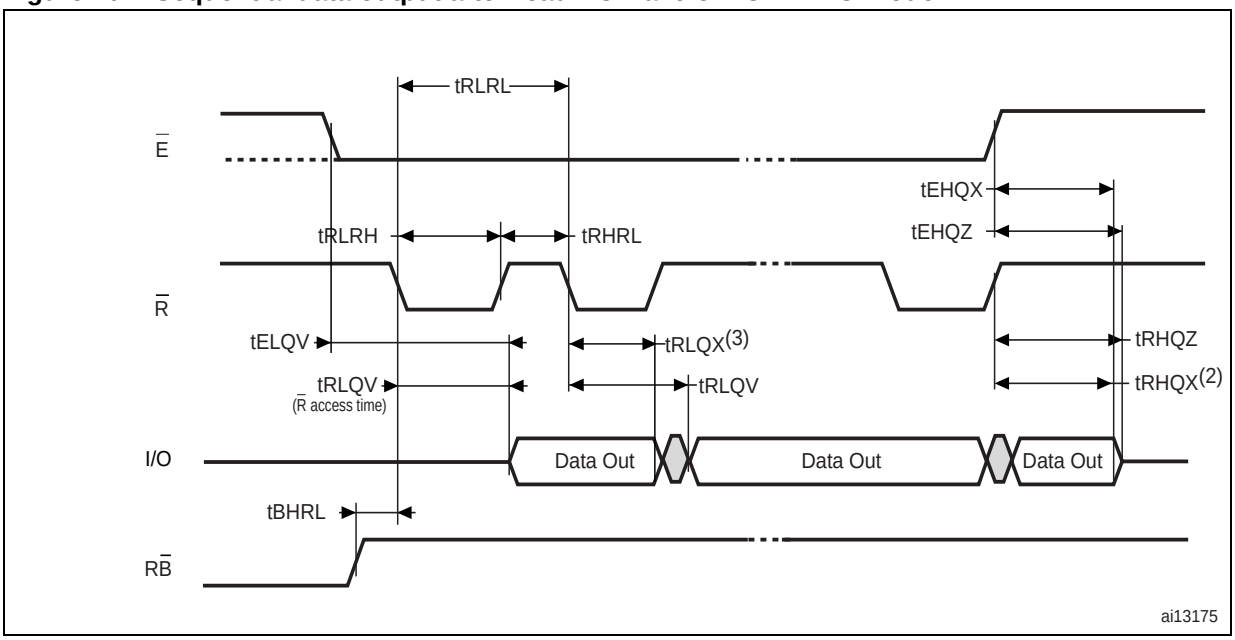
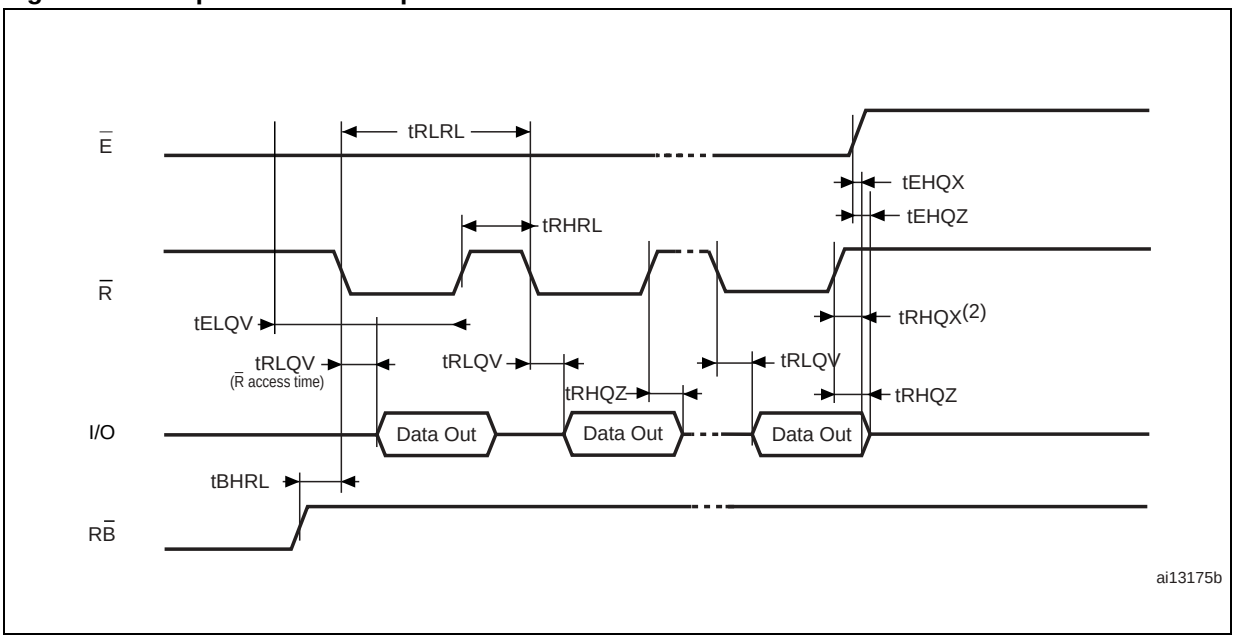


Figure 40. Sequential data output after read AC waveforms in EDO mode



1. This diagram refers to EDO mode, CL and AL Low, V_{IL}, and $\overline{W}$ High, V_{IH}.
2. t_{RHQX} is applicable for frequencies lower than 33 MHz (for instance, t_{RLRL} lower than 30 ns).
3. t_{RLQX} is applicable for frequencies higher than 33 MHz (for instance, t_{RLRL} lower than 30 ns). It is possible to read data on the next Read Enable Low, but just for a time t_{RLQX}.

Figure 41. Sequential data output after read AC waveforms



1. This diagram refers to CL and AL Low, V_{IL}, and $\overline{W}$ High, V_{IH}.
2. t_{RHQX} is applicable for frequencies lower than 33 MHz (for instance, t_{RLRL} lower than 30 ns).

Figure 42. Read Status Register AC waveforms

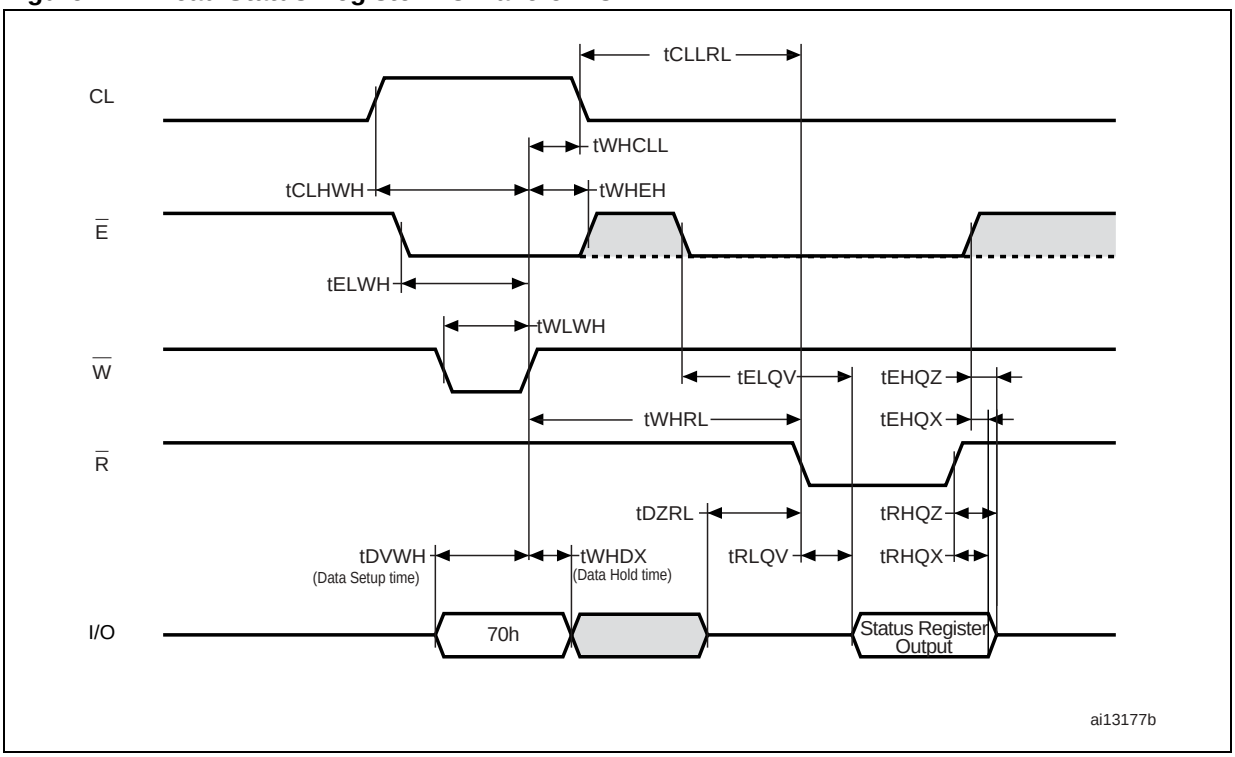
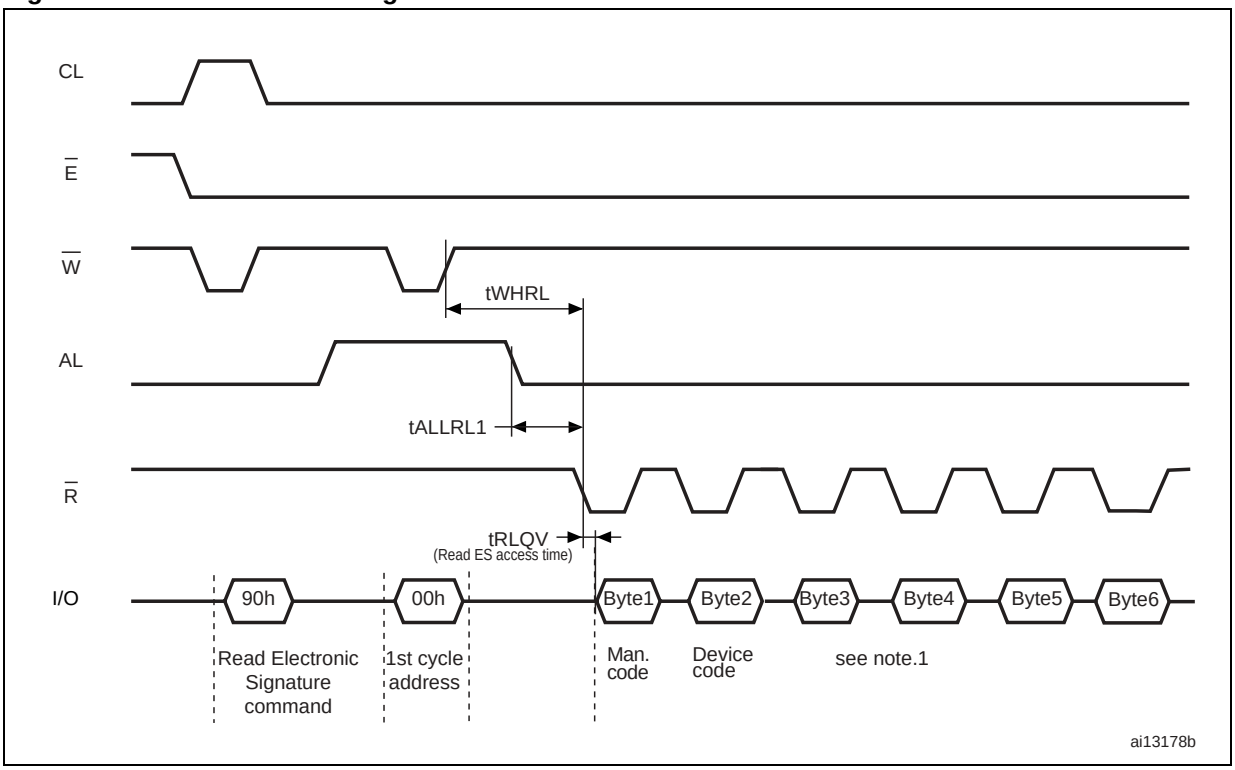


Figure 43. Read electronic signature AC waveforms



1. Refer to *Table 14* for the values of the manufacturer and device codes, and to *Table 15*, *Table 16*, *Table 17*, and *Table 18* for the information contained in byte 3, byte 4, byte 5, and byte 6.

13.1 Ready/Busy signal electrical characteristics

The Ready/Busy signal indicates the status of the device operation. The Ready/Busy signal is Low, when a reset, program, erase or random read operation is in progress while it is High when these operations are completed.

Figure 44, *Figure 45*, and *Figure 46* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 44. Ready/Busy AC waveform

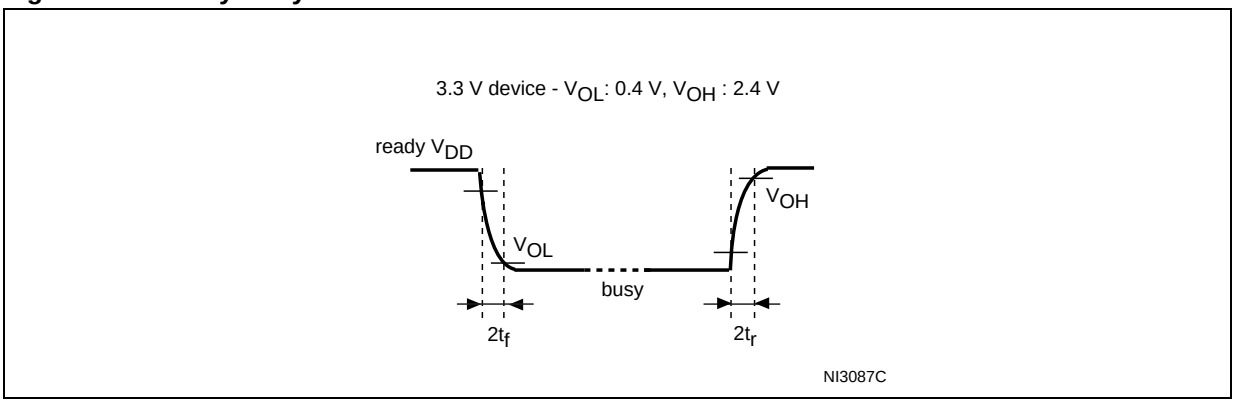


Figure 45. Ready/Busy load circuit

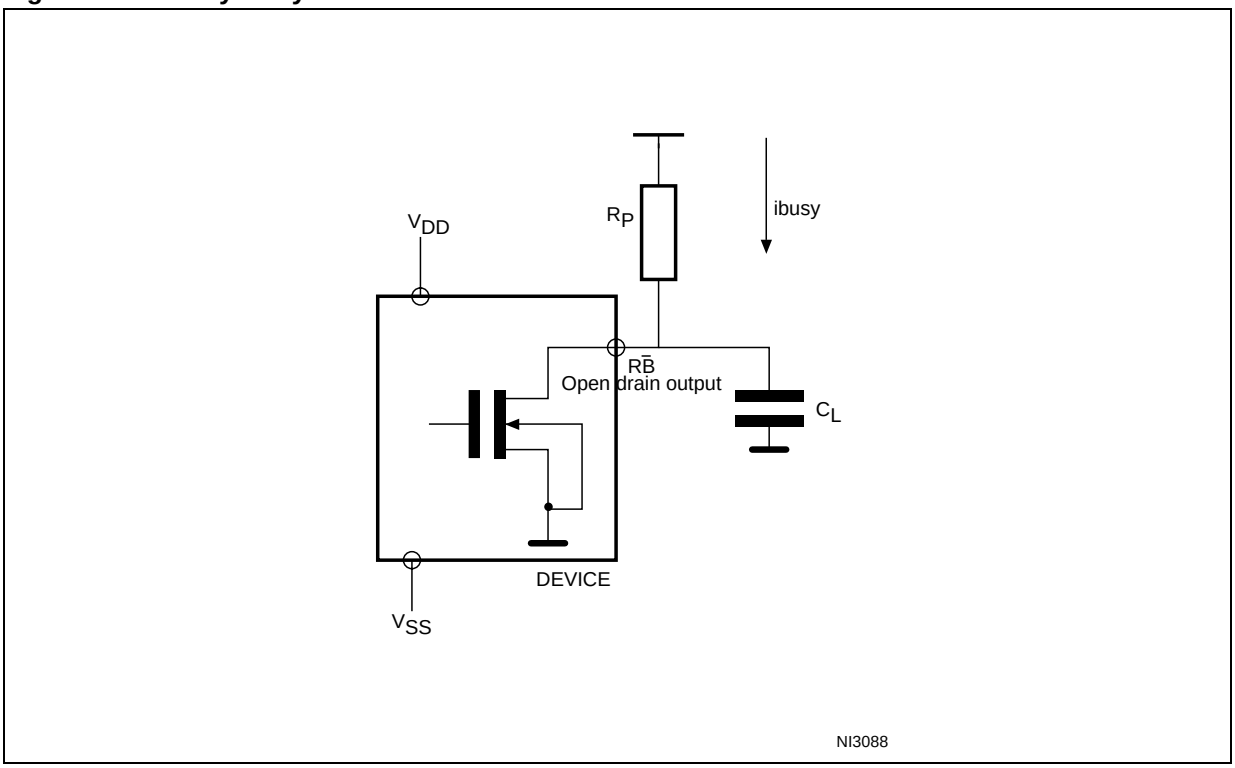
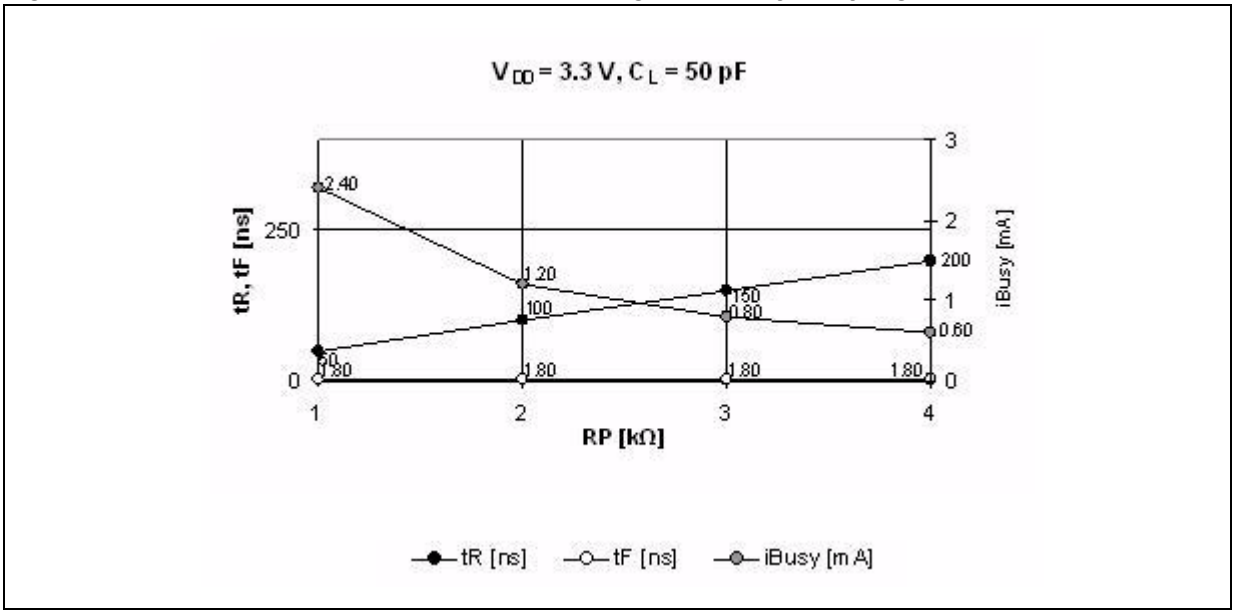


Figure 46. Resistor value versus waveform timings for Ready/Busy signal



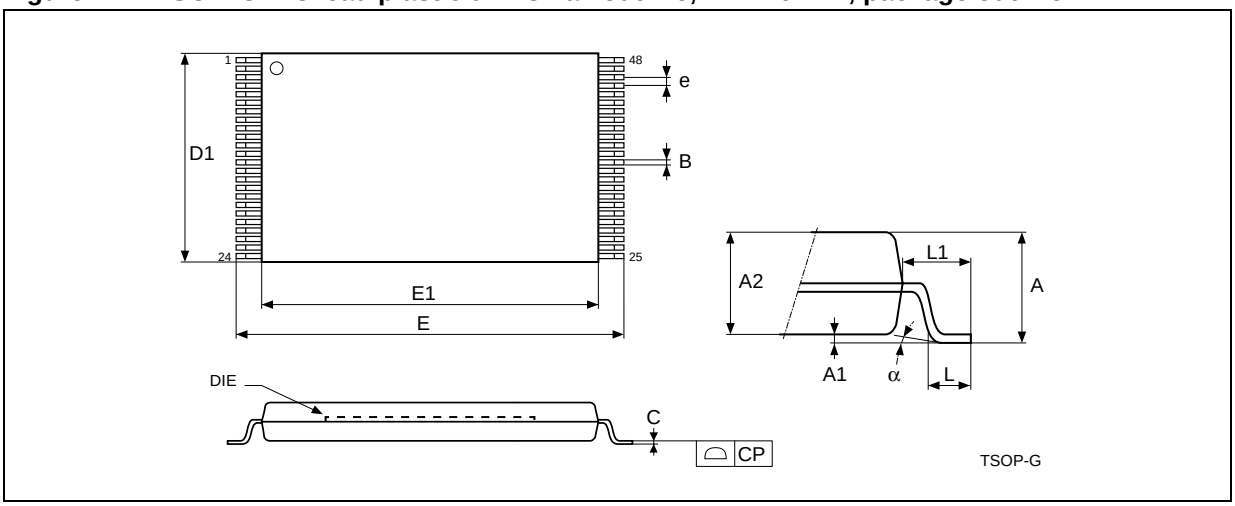
1. T = 25 °C.

14 Package mechanical

To meet environmental requirements, Numonyx offers these devices in RoHS compliant packages, which have a lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

RoHS compliant specifications are available at www.numonyx.com.

Figure 47. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline



1. Drawing is not to scale.

Table 28. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.08			0.003
D1	12.00	11.90	12.10	0.472	0.468	0.476
E	20.00	19.80	20.20	0.787	0.779	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	
L	0.60	0.50	0.70	0.024	0.020	0.028
L1	0.80			0.031		
a	3°	0°	5°	3°	0°	5°

15 Ordering information

Table 29. Ordering information scheme

Example: NAND16G W 3 D 2 B N 6 E

Device type

NAND flash memory

Density

16G = 16 Gbits

Operating voltage

W = V_{DD} = V_{DDQ} = 2.7 to 3.6 V

Bus width

3 = x8

Family identifier

D = 4 Kbyte-page MLC

Device options

2 = Chip Enable ‘don't care’ enabled

Product version

B = second version

Package

N = TSOP48 12 x 20 mm

Temperature range

6 = –40 to 85 °C

Option

E = RoHS compliant package, standard packing

F = RoHS compliant package, tape and reel packing

Note: Devices are shipped from the factory with the memory content bits, in valid blocks, erased to ‘1’.

For further information on any aspect of this device, please contact your nearest Numonyx sales office.

16 Revision history

Table 30. Document revision history

Date	Revision	Changes
17-Dec-2008	1	Initial release.
24-Sep-2009	2	Modified datasheet's name from NANDxxGx3D2B to NAND16GW3D2B. Document status promoted from 'preliminary data' to full datasheet. Removed all the references to 32-Gbit, 64-Gbit devices and hybrid version throughout the document. Added note in *Section 6.1.6: Cache read*. Modified: maximum value of t_{EHQZ} in *Table 27: AC characteristics for operations*, *Section 8: Power-on sequence and PSL handling*, *Figure 44: Ready/Busy AC waveform* and *Figure 46: Resistor value versus waveform timings for Ready/Busy signal*.

Please Read Carefully: