PIC18F86J72/87J72

PIC18F86J72/87J72 Silicon Errata and Data Sheet Clarification

The PIC18F86J72/87J72 devices that you have received conform functionally to the current Device Data Sheet (DS39979**A**) except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F86J72/87J72 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1, A3**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVID:REVID values for the various PIC18F86J72/87J72 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A1	A3
PIC18F87J72	503Xh	1h	3h
PIC18F86J72	502Xh		

Note 1: The Device IDs (DEVID and REVID) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:REVID".

2: Refer to the *"PIC18F6XJXX/8XJXX Family Flash Microcontroller Programming Specification"* (DS39644) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A1	A3	
MSSP	I^2C™ Slave	1.	If the SSPBUF register is not read within a window after the SSPIF interrupt, the module may not receive the correct data.	X	X	
EUSART	Enable/ Disable	2.	If interrupts are enabled, disabling and re-enabling the module requires a 2 TCY delay.	X	X	
RTCC	INTRC Clock	3.	The INTRC clock is not automatically enabled when it is selected.	X		
RTCC	Port Override	4.	The RTCC output does not override the associated TRIS bit.	X		
MSSP	I^2C Mode	5.	If a Stop condition occurs in the middle of an address or data reception, there will be issues with the SCL clock stream and RCEN bit.	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1, A3**).

1. Module: MSSP (I^2C™ Slave)

In extremely rare cases when configured for I^2C™ slave reception, the MSSP module may not receive the correct data. This occurs only if the Serial Receive/Transmit Buffer register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF bit is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A1	A3						
X	X						

2. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (SPEN bit (RCSTAx<7>) = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2 TCY delay after re-enabling the EUSART.

1. Disable receive interrupts (RCxIE bit (PIE1<5>) = 0).
2. Disable the EUSART (RCSTAx<7> = 0).
3. Re-enable the EUSART (RCSTAx<7> = 1).
4. Re-enable receive interrupts (PIE1<5> = 1). (This is the first TCY delay.)
5. Execute a NOP instruction. (This is the second TCY delay.)

Affected Silicon Revisions

A1	A3						
X	X						

3. Module: Real-Time Clock and Calendar (RTCC)

The INTRC is not automatically enabled as the clock source for the RTCC module when the INTRC clock is selected (CONFIG3L<1> = 0) and the RTCC module is enabled (RTCCFG<7> = 1).

Work around

In order to enable the INTRC, at least one of the following has to be enabled:

1. Watchdog Timer Enable bit (WDTEN, CONFIG1L<0>).
2. Two-Speed Start-up Enable bit (IESO, CONFIG2L<7>).
3. Fail-Safe Clock Monitor Enable bit (FCMEN, CONFIG2L<6>).

Affected Silicon Revisions

A1	A3						
X							

4. Module: Real-Time Clock and Calendar (RTCC)

When the RTCC output is enabled (RTCOE = 1), the RTCC module does not override the input state of RG4.

Work around

Clear the port direction bit associated with the RG4 pin (TRISG<4>) when the RTCC output to RG4 is desired.

Affected Silicon Revisions

A1	A3						
X							

5. Module: MSSP (I^2C™ Mode)

In Master I^2C Receive mode, if a Stop condition occurs in the middle of an address or data reception, the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. When a Start condition occurs after the improper Stop condition, nine additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches that may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and subsequently stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPCON1.

Affected Silicon Revisions

A1	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39979**A**).

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with PIC18FJ Microcontrollers

Section 2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

The on-chip voltage regulator enable pin, ENVREG, must always be connected directly to either a supply voltage or to ground. Tying ENVREG to VDD enables the regulator, while tying it to ground disables the regulator. Refer to **Section 26.3 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

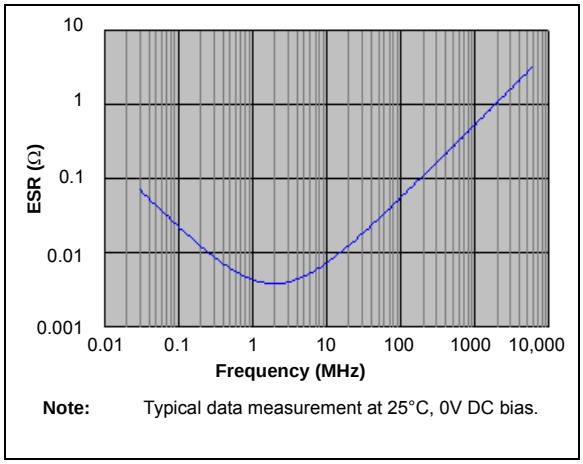
Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 29.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

Note that the "LF" versions of some low pin count PIC18FJ parts (e.g., the PIC18LF45J10) do not have the ENVREG pin. These devices are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to +125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to +85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

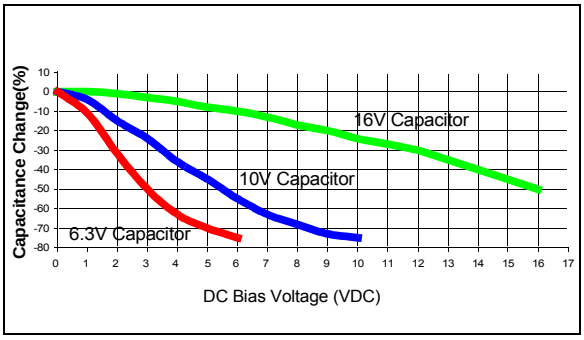
Typical low-cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R) or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum V_{DDCORE} voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2. Module: VBOR Specification

Changes have been made to the VBOR specification, Parameter Number D005 in Table 29.1, as shown in bold text in the updated table below.

29.1 DC Characteristics: Supply Voltage PIC18F86J72/87J72 (Industrial)

PIC18F86J72/87J72 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D001	VDD	Supply Voltage	VDDCORE 2.0	— —	3.6 3.6	V V	ENVREG tied to VSS ENVREG tied to VDD
D001B	VDDCORE	External Supply for Microcontroller Core	2.0	—	2.70	V	ENVREG tied to VSS
D001C	AVDD	Analog Supply Voltage	VDD – 0.3	—	VDD + 0.3	V	
D001D	AVSS	Analog Ground Potential	VSS – 0.3	—	VSS + 0.3	V	
D002	VDR	RAM Data Retention Voltage(1)	1.5	—	—	V	
D003	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	—	—	0.7	V	See Section 5.3 “Power-on Reset (POR)” for details
D004	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	See Section 5.3 “Power-on Reset (POR)” for details
D005	VBOR	Brown-out Reset Voltage	**1.75(2)**	2.0	**2.4**	V	

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: When the BOR is enabled, the part will continue to operate until the BOR occurs. This is valid, although VDD may be below the minimum VDD voltage.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2010)

Initial release of this errata. Includes silicon issues 1 (MSSP – I^2C Slave), 2 (EUSART), 3 (RTCC), 4 (RTCC) and 5 (MSSP – I^2C Mode).

Rev B Document 9/2010

Added data sheet clarification issue 1 (Guidelines For Getting Started with PIC18FJ Microcontrollers).

Rev C Document 9/2011

Updated data sheet clarification issue 2 (V_{BOR} Specification).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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