PCE85133AUG

Universal 80 × 4 LCD driver for low multiplex rates

Rev. 2 — 22 July 2015 Product data sheet

1. General description

The PCE85133AUG is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 80 segments. The PCE85133AUG is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing and by display memory switching (static and duplex drive modes).

For a selection of NXP LCD segment drivers, see Table 23 on page 42.

2. Features and benefits

- Single-chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$, or $\frac{1}{3}$
- Frame frequency: 150 Hz
- Internal LCD bias generation with voltage-follower buffers
- 80 segment drives:
  - Up to 40 7-segment alphanumeric characters
  - Up to 20 14-segment alphanumeric characters
  - Any graphics of up to 320 segments/elements
- 80 × 4 RAM for display data storage
- Display memory bank switching in static and duplex drive modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 5.5 V for high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- No external components needed
- Compatible with Chip-On-Glass (COG) technology

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 18.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCE85133AUG	bare die	110 bumps	PCE85133AUG

3.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCE85133AUG/DA	PCE85133AUG/DAZ	935306039033	chip with hard bumps in tray[1]	1

[1] Bump hardness see Table 20.

4. Block diagram

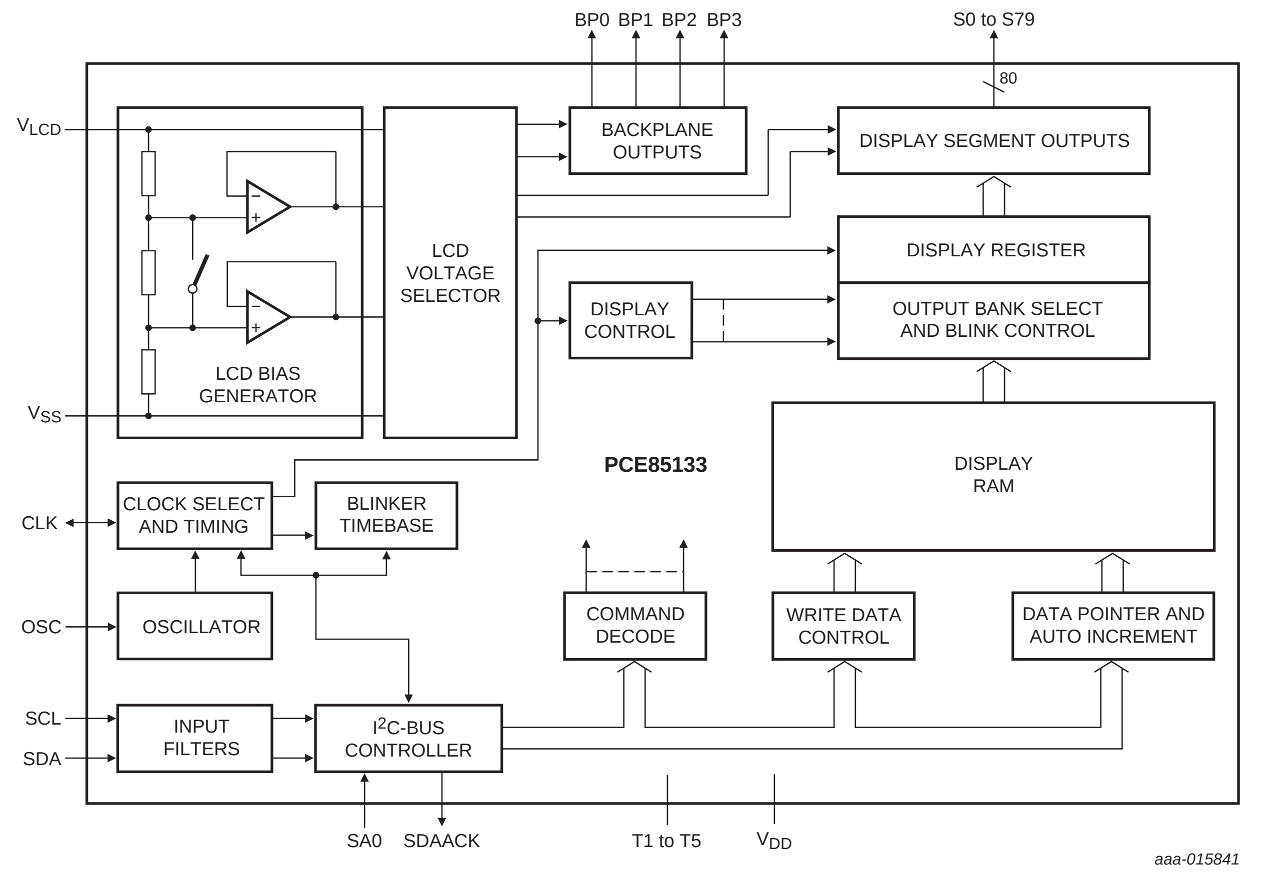

Fig 1. Block diagram of PCE85133AUG

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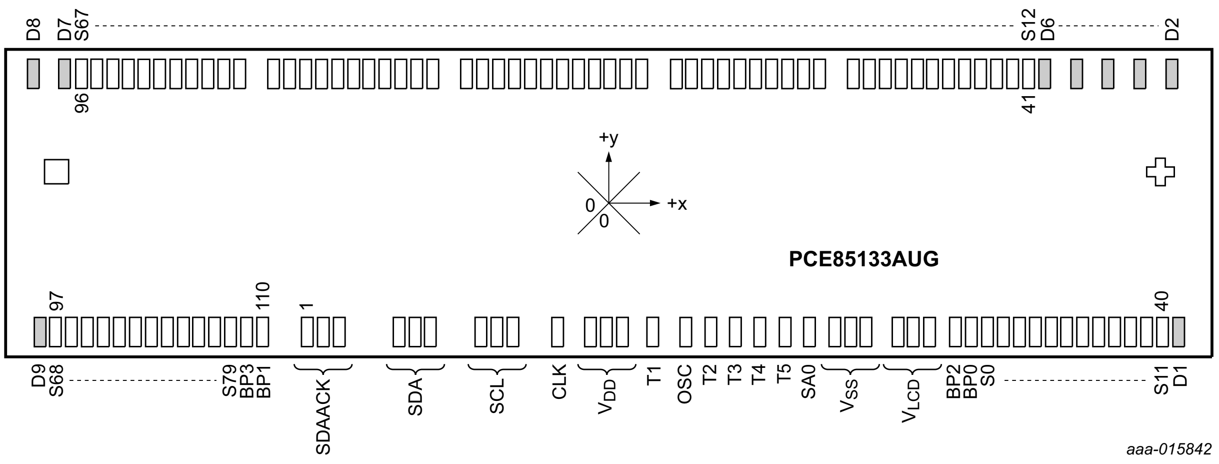
5. Pinning information

5.1 Pinning



Viewed from active side. For mechanical details, see Figure 27.

Fig 2. Pin configuration for PCE85133AUG

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5.2 Pin description

Table 3. Pin description overview

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
SDAACK	1 to 3	I^2C-bus acknowledge output
SDA	4 to 6	I^2C-bus serial data input
SCL	7 to 9	I^2C-bus serial clock input
CLK	10	clock input and output
V_{DD}	11 to 13	supply voltage
T1	14	test pin; must be left open
OSC	15	oscillator select • connect to V_{DD} for external clock • connect to V_{SS} for internal clock
T2	16	test pin; must be tied to V_{DD}
T3 to T5	17 to 19	test pins; must be tied to V_{SS}
SA0	20	I^2C-bus slave address input • connect to V_{DD} for logic 1 • connect to V_{SS} for logic 0
V_{SS}[1]	21 to 23	ground supply voltage
V_{LCD}	24 to 26	LCD supply voltage
BP2	27	LCD backplane output
BP0	28	
BP3	109	
BP1	110	
S0 to S79	29 to 108	LCD segment output
D1 to D9[2]	-	dummy pins

[1] The substrate (rear side of the die) is at V_{SS} potential and should be electrically isolated.

[2] The dummy pads are connected to V_{SS} but not tested.

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6. Functional description

6.1 Commands of PCE85133AUG

The command decoder identifies command bytes that arrive on the I^{2}C-bus. The commands available to the PCE85133AUG are defined in Table 4.

Table 4. Definition of commands

Command	Operation code								Reference
Bit	7	6	5	4	3	2	1	0	
mode-set	1	1	0	0	E	B	M[1:0]		Table 5
initialize-RAM	1	1	1	0	0	0	0	0	Table 6
load-data-pointer	0	P[6:0]							Table 7
bank-select	1	1	1	1	1	0	I	O	Table 8

Table 5. Mode-set command bit description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**[1]
		0	disabled (blank)[2]
		1	enabled
2	B		**LCD bias configuration**[3]
		0	⅓ bias
		1	½ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; 1 backplane (BP0)
		10	1:2 multiplex; 2 backplanes (BP0 and BP1)
		11	1:3 multiplex; 3 backplanes (BP0 to BP2)
		00	1:4 multiplex; 4 backplanes (BP0 to BP3)

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[3] Not applicable for static drive mode.

Table 6. Initialize-RAM command bit description

See Section 6.3.1.

Bit	Symbol	Value	Description
7 to 0	-	11100000	**initializing the RAM access**

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Table 7. Load-data-pointer command bit description

See Section 6.3.1.

Bit	Symbol	Value	Description
7	-	0	fixed value
6 to 0	P[6:0]	0000000 to 1001111	**data pointer** 7-bit binary value of 0 to 79, transferred to the data pointer to define one of 80 display RAM addresses

Table 8. Bank-select command bit description[1]

See Section 6.3.4 and Section 6.3.5.

Bit	Symbol	Value	Description	
			Static	1:2 multiplex
7 to 2	-	111110	fixed value	
1	I		**input bank selection**: storage of arriving display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**output bank selection**: retrieval of LCD display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 or 1:4 multiplex drive modes.

6.2 Clock and frame frequency

6.2.1 Oscillator

The internal logic and the LCD drive signals of the PCE85133AUG are timed by a frequency f_{clk} which either is derived from the built-in oscillator frequency f_{osc}:

$$f_{clk} = \frac{f_{osc}}{64} \qquad (1)$$

or equals an external clock frequency $f_{clk(ext)}$:

$$f_{clk} = f_{clk(ext)} \qquad (2)$$

6.2.1.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to V_{SS}.

6.2.1.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK then becomes the external clock input.

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

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6.2.2 Frame frequency

The clock frequency f_{clk} determines the LCD frame frequency f_{fr} and is calculated as follows:

$$f_{fr} = \frac{f_{clk}}{24} \quad (3)$$

6.3 Display RAM

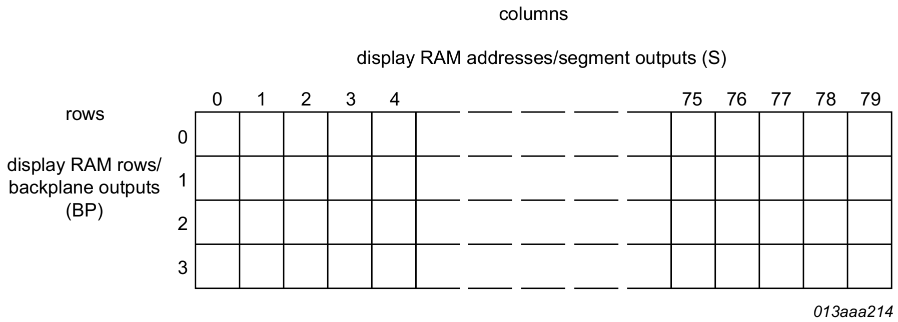
The display RAM is a static 80 × 4 RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD segments/elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bit map, Figure 3, shows rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and columns 0 to 79 which correspond with the segment outputs S0 to S79. In multiplexed LCD applications the segment data of the 1st, 2nd, 3rd and 4th row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.



The display RAM bitmap shows the direct relationship between the display RAM addresses and the segment outputs and between the bits in a RAM word and the backplane outputs.

Fig 3. Display RAM bitmap

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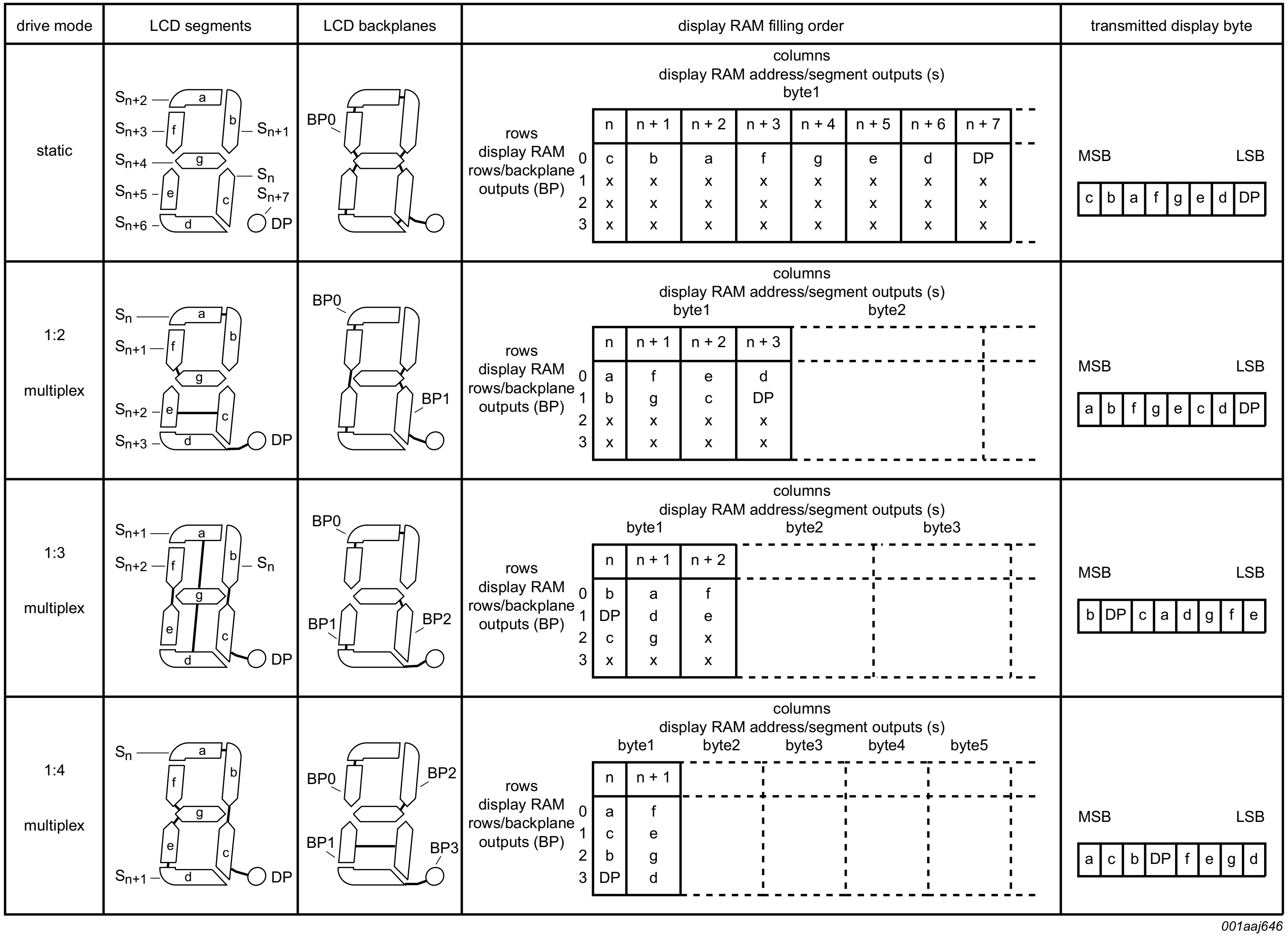

x = data bit unchanged

Fig 4. Relationships between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

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When display data is transmitted to the PCE85133AUG, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly, in pairs, triples or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 4; the RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 4:

- In static drive mode, the eight transmitted data bits are placed into row 0 as 1 byte.
- In 1:2 multiplex drive mode, the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.
- In 1:3 multiplex drive mode, the 8 bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 6.3.2).
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.

6.3.1 Writing to RAM

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM.

The sequence always commences with the initialize-RAM command (see Table 6). Following this command, the data pointer has to be set to the desired RAM address using the load-data-pointer command (see Table 7). After this, an arriving data byte is stored at the display RAM address indicated by the data pointer. The RAM writing procedure is illustrated in Figure 5 and the filling order of the RAM is shown in Figure 4.

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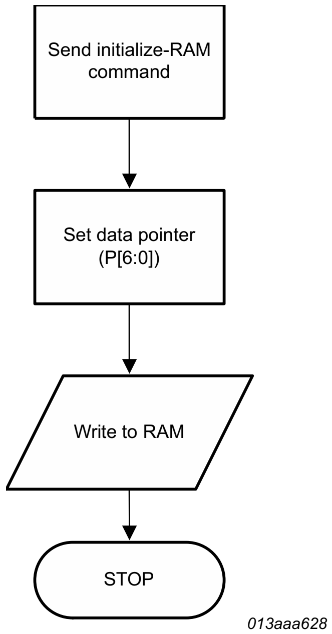

Fig 5. RAM writing procedure

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^{2}C-bus data access terminates early, then the state of the data pointer is unknown. So, the data pointer must be rewritten before further RAM accesses.

6.3.2 RAM writing in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 9 (see Figure 4 as well).

Table 9. Standard RAM filling in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. ***are not connected*** *to any segments/elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**:**
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 10.

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Table 10. Entire RAM filling by rewriting in 1:3 multiplex drive mode

Assumption: BP2/S2, BP2/S5, BP2/S8 etc. ***are connected*** *to segments/elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 10 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 etc. have to be connected to segments/elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written.
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6.
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6.

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some segments/elements remain unused or can be used, but it has to be considered in the module layout process as well as in the driver software design.

6.3.3 Writing over the RAM address boundary

In all multiplex drive modes, depending on the setting of the data pointer, it is possible to fill the RAM over the RAM address boundary. In this case, the additional bits are discarded.

6.3.4 Output bank selector

The output bank selector (see Table 8) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCE85133AUG includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

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6.3.5 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 8). The input bank selector functions independently to the output bank selector.

6.4 Initialization

At power-on, the status of the I²C-bus and the registers of the PCE85133AUG is undefined. Therefore the PCE85133AUG should be initialized as quickly as possible after power-on to ensure a proper bus communication and to avoid display artifacts. The following instructions should be accomplished for initialization:

- I²C-bus (see Section 7) initialization
  - generating a START condition
  - sending 0h and ignoring the acknowledge
  - generating a STOP condition
- Mode-set command (see Table 5), setting
  - bit E = 0
  - bit B to the required LCD bias configuration
  - bits M[1:0] to the required LCD drive mode
- Initialize-RAM command (see Table 6)
- Load-data-pointer command (see Table 7), setting
  - bits P[6:0] to 0h (or any other required address)
- Bank-select command (see Table 8), setting
  - bit I to 0
  - bit O to 0
- writing meaningful information (for example, a logo) into the display RAM (see Section 6.3 on page 7)

After the initialization, the display can be switched on by setting bit E = 1 with the mode-set command.

6.5 Possible display configurations

The display configurations possible with the PCE85133AUG depend on the required number of active backplane outputs. A selection of display configurations is given in Table 11.

All of the display configurations given in Table 11 can be implemented in a typical system as shown in Figure 7.

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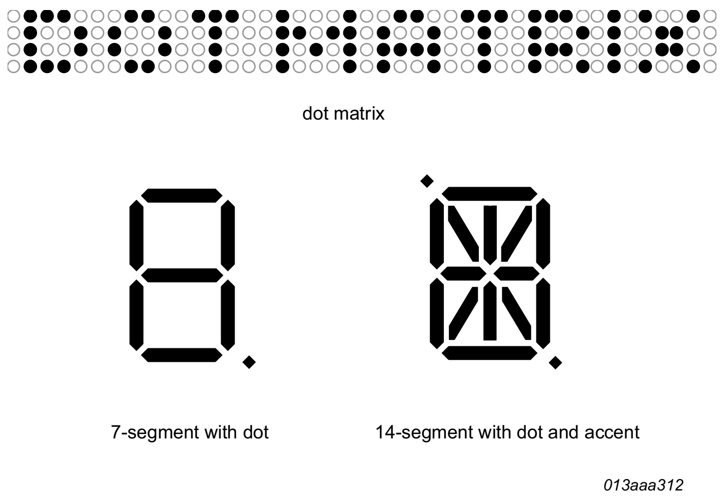

Fig 6. Example of displays suitable for PCE85133AUG

Table 11. Selection of possible display configurations

Number of				
Backplanes	Icons	Digits/Characters		Dot matrix: segments/ elements
		7-segment[1]	14-segment[2]	
4	320	40	20	320 (4 × 80)
3	240	30	15	240 (3 × 80)
2	160	20	10	160 (2 × 80)
1	80	10	5	80 (1 × 80)

[1] 7 segment display has 8 segments/elements including the decimal point.

[2] 14 segment display has 16 segments/elements including decimal point and accent dot.

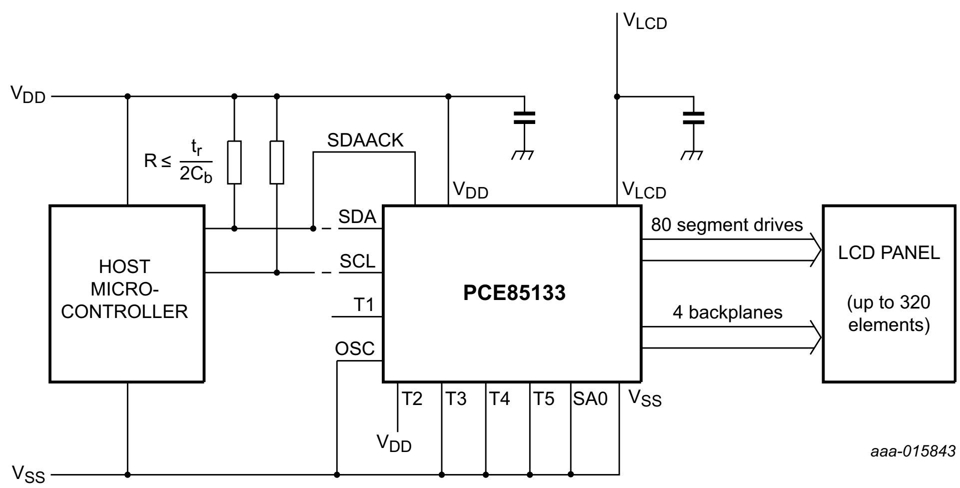

Fig 7. Typical system configuration

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The host microcontroller maintains the 2-line I²C-bus communication channel with the PCE85133AUG. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

6.6 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between pins V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the ½ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

6.7 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 12.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

Table 12. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (4)$$

where the values for n are

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n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 5:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (5)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 6:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (6)$$

Using Equation 6, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

6.7.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 8. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (7)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (8)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 4 to Equation 6) and the V_{LCD} voltage.

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$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

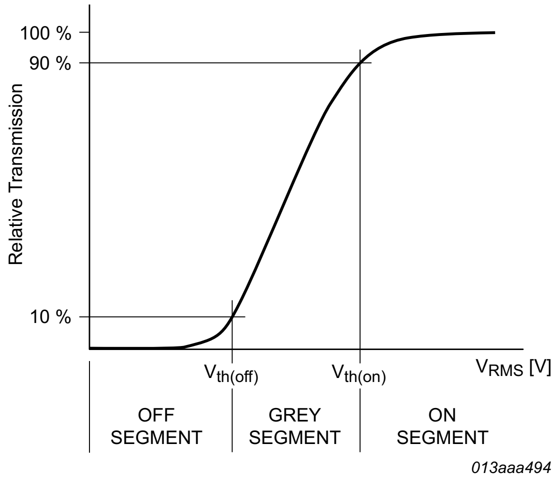

Fig 8. Electro-optical characteristic: relative transmission curve of the liquid

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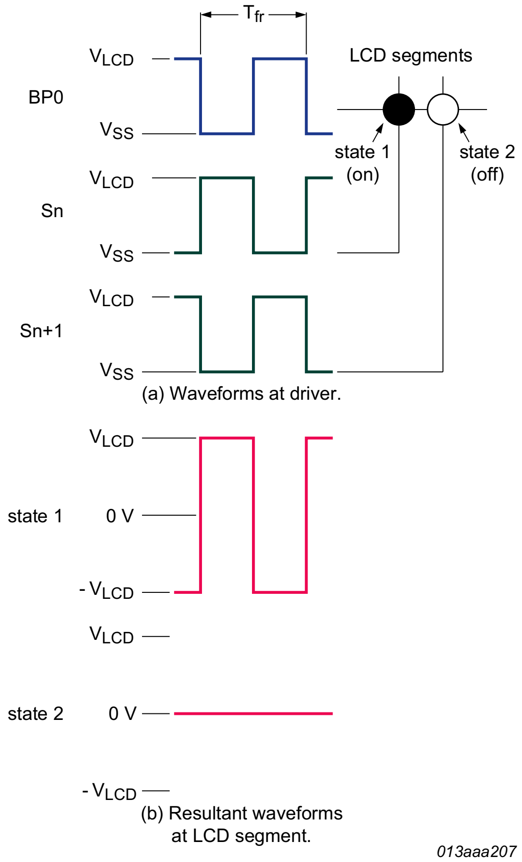
6.8 LCD drive mode waveforms

6.8.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 9.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 9. Static drive mode waveforms

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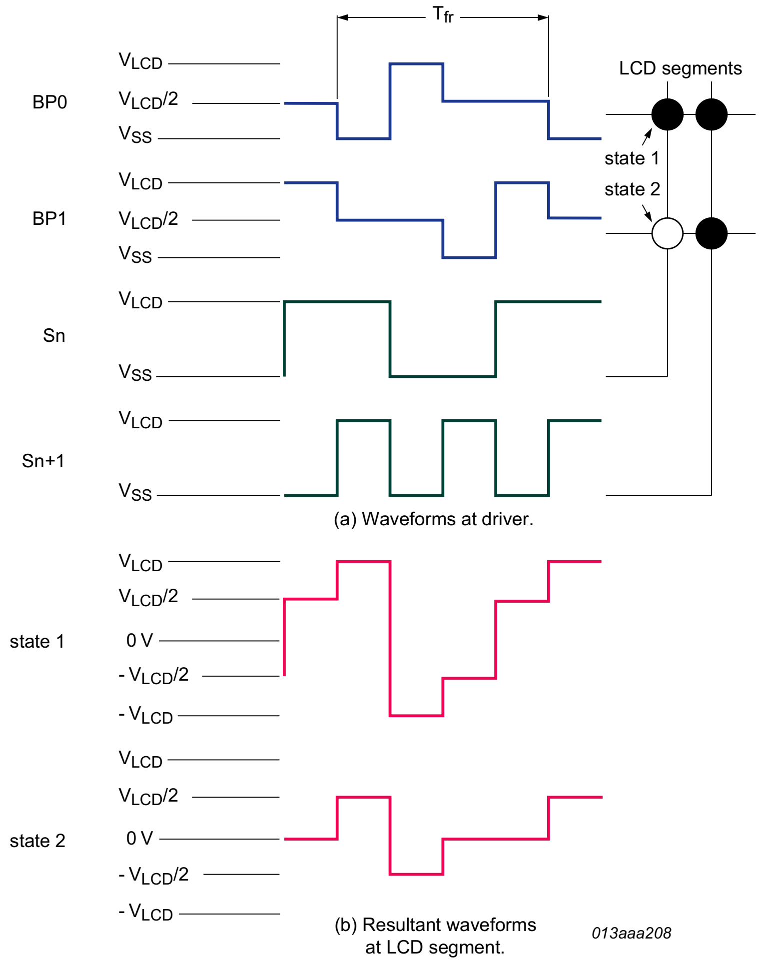
6.8.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCE85133AUG allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 10 and Figure 11.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 10. Waveforms for the 1:2 multiplex drive mode with ½ bias

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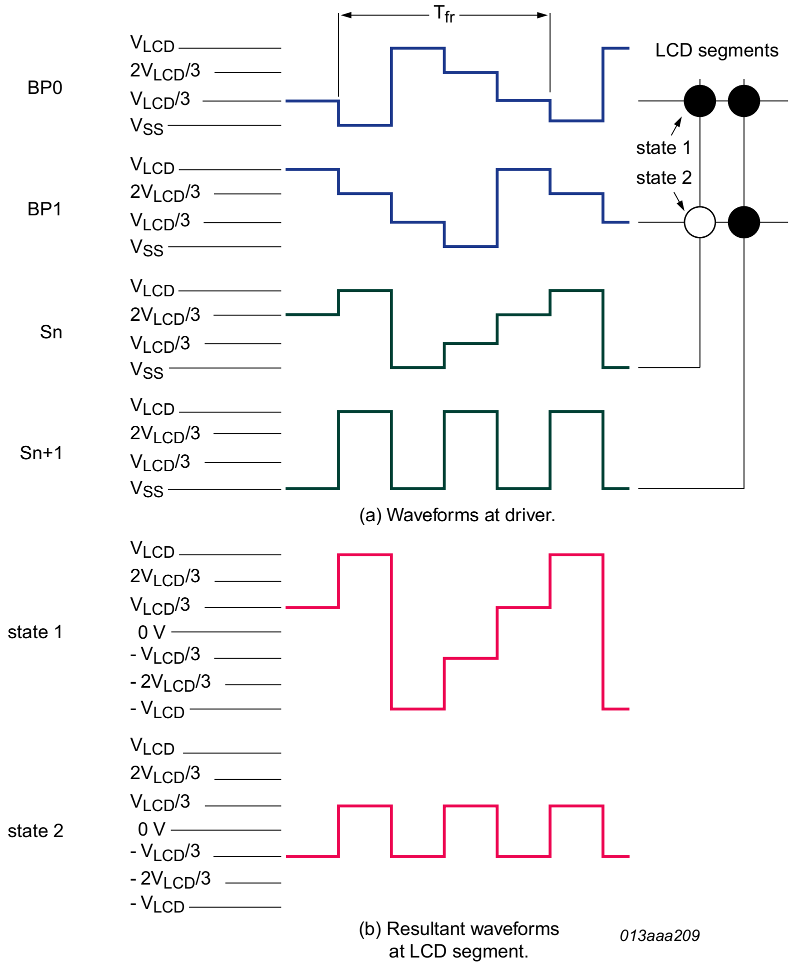

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 11. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

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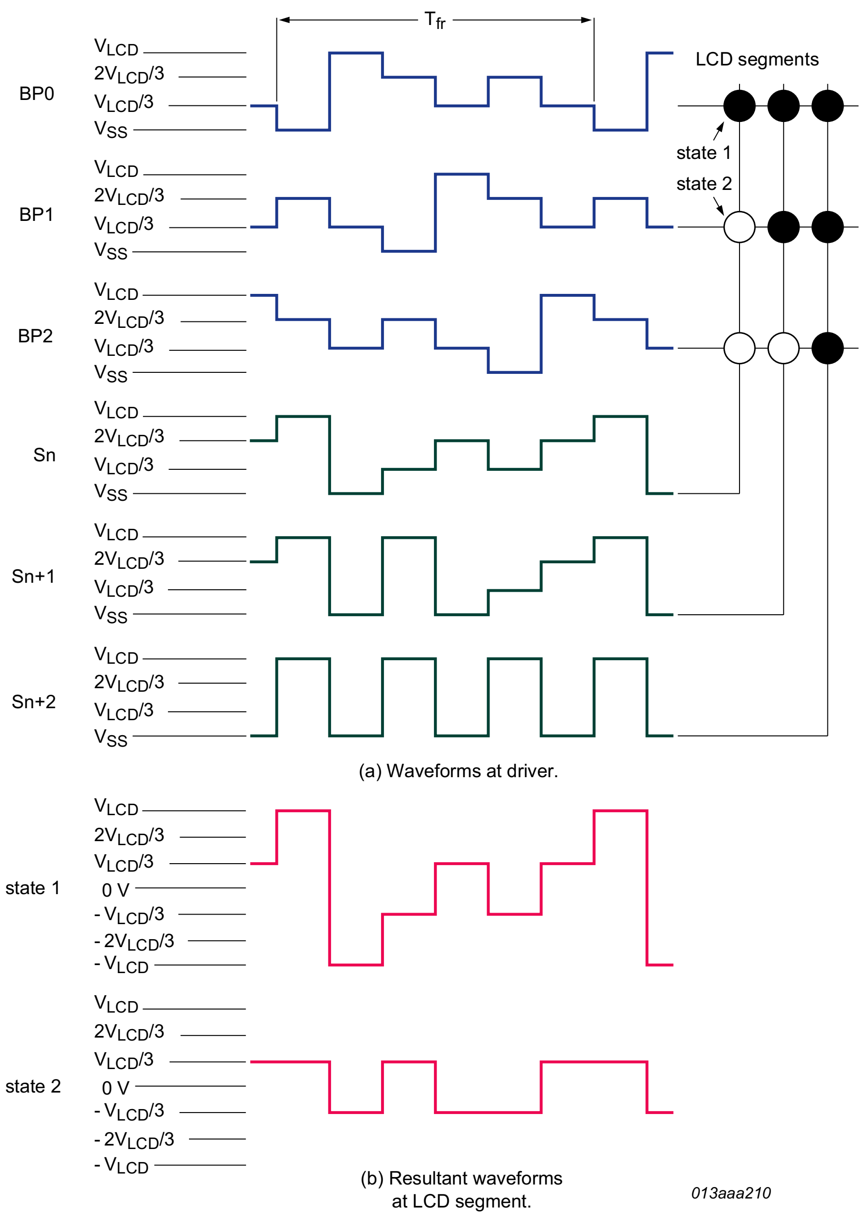
6.8.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 12.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 12. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

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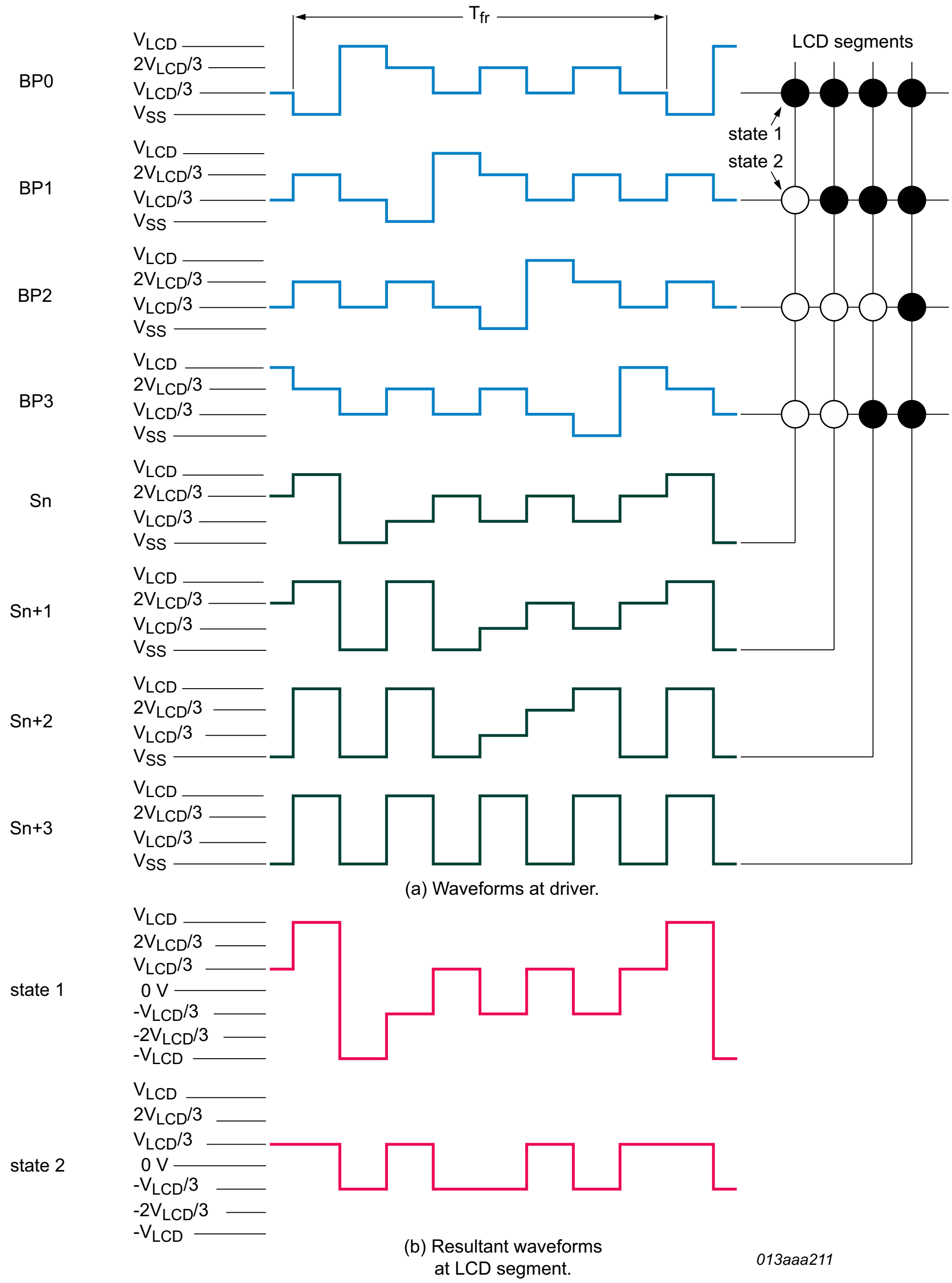
6.8.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 13.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 13. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

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6.9 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In the 1:4 multiplex drive mode, BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1; therefore, these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, respectively, BP1 and BP3 carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: The same signal is carried by all four backplane outputs; and they can be connected in parallel for very high drive requirements.

6.10 Segment outputs

The LCD drive section includes 80 segment outputs (S0 to S79) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 80 segment outputs are required, the unused segment outputs must be left open-circuit.

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7. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

By connecting pin SDAACK to pin SDA on the PCE85133AUG, the SDA line becomes fully I²C-bus compatible. In COG applications where the track resistance from the SDAACK pin to the system SDA line can be significant, possibly a voltage divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. As a consequence, it may be possible that the acknowledge generated by the PCE85133AUG cannot be interpreted as logic 0 by the master. In COG applications where the acknowledge cycle is required, it is therefore necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level.

By separating the acknowledge output from the serial data line (having the SDAACK open circuit), design efforts to generate a valid acknowledge level can be avoided. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

The following definition assumes that SDA and SDAACK are connected and refers to the pair as SDA.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see Figure 14).

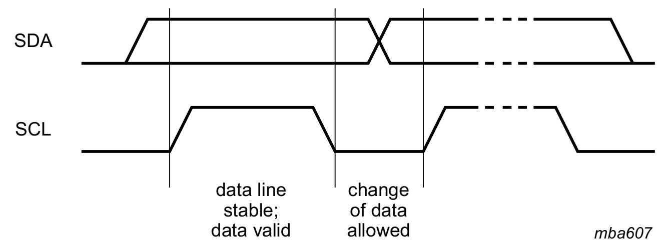

Fig 14. Bit transfer

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

2. For further information, consider the NXP application note: Ref. 1 “AN10170”.

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The START and STOP conditions are shown in Figure 15.

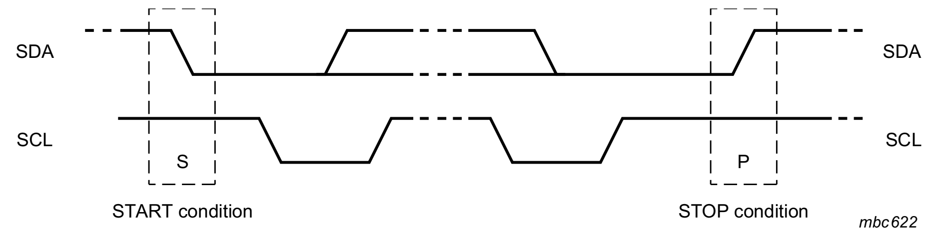

Fig 15. Definition of START and STOP conditions

7.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 16.

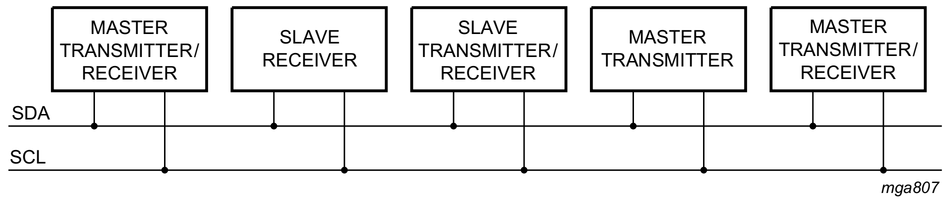

Fig 16. System configuration

7.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^{2}C-bus is shown in Figure 17.

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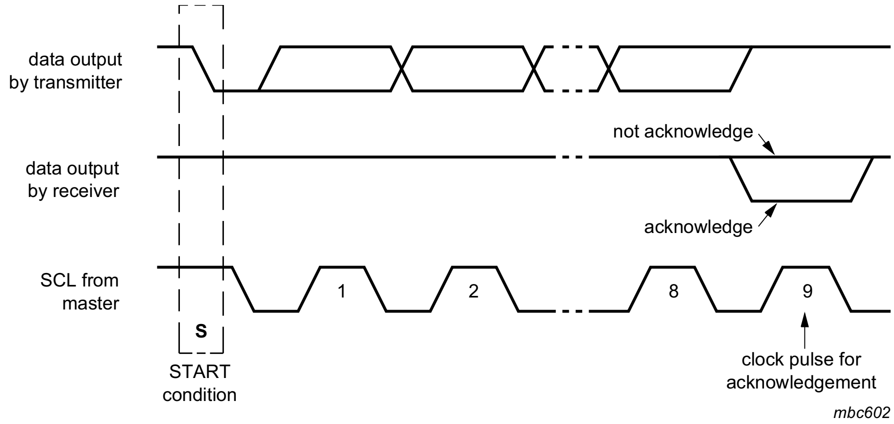

Fig 17. Acknowledgement on the I²C-bus

7.5 I²C-bus controller

The PCE85133AUG acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCE85133AUG are the acknowledge signals from the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data, and on the hardware subaddress.

7.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are used to address the PCE85133AUG. The entire I²C-bus slave address byte is shown in Table 13.

Table 13. I²C slave address byte

	Slave address							
Bit	7 MSB	6	5	4	3	2	1	0 LSB
	0	1	1	1	0	0	SA0	R/$\overline{W}$

The PCE85133AUG is a write-only device and will not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte that a PCE85133AUG will respond to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

The I²C-bus protocol is shown in Figure 18. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the PCE85133AUG slave addresses.

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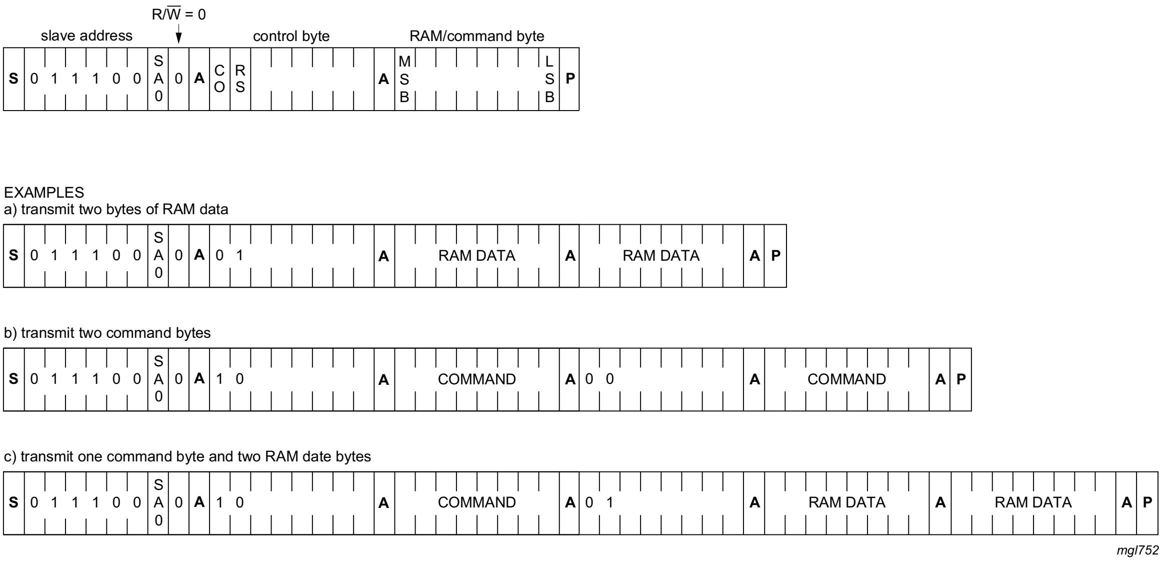

Fig 18. I²C-bus protocol

After acknowledgement, the control byte is sent, defining if the next byte is a RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data (see Figure 19 and Table 14). In this way, it is possible to configure the device and then fill the display RAM with little overhead.

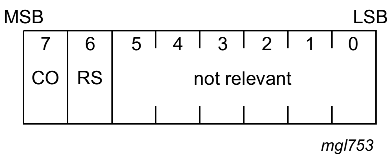

Fig 19. Control byte format

Table 14. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-		not relevant

The command bytes and control bytes are also acknowledged by the PCE85133AUG.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated. After the last display byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be asserted to RESTART an I²C-bus access.

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8. Internal circuitry

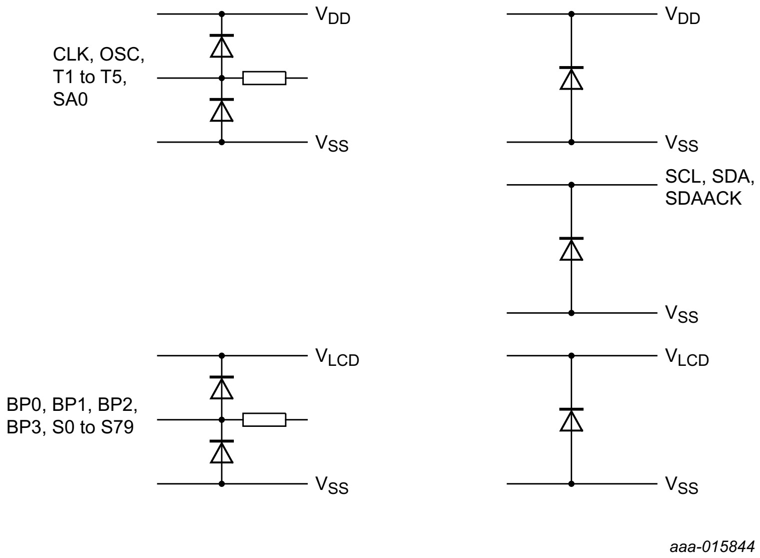

Fig 20. Device protection diagram

9. Safety notes

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION	
	Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION	
	Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

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10. Limiting values

Table 15. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
V_{LCD}	LCD supply voltage			–0.5	+6.5	V
$V_{i(n)}$	voltage on any input	V_{DD} related inputs		–0.5	+6.5	V
$V_{o(n)}$	voltage on any output	V_{LCD} related outputs		–0.5	+6.5	V
I_I	input current			–10	+10	mA
I_O	output current			–10	+10	mA
I_{DD}	supply current			–50	+50	mA
I_{SS}	ground supply current			–50	+50	mA
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	±4000	V
I_{lu}	latch-up current		[3]	-	100	mA
T_{stg}	storage temperature		[4]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Stresses above these values listed may cause permanent damage to the device.

[2] Pass level; Human Body Model (HBM) according to Ref. 7 "JESD22-A114".

[3] Pass level; latch-up testing, according to Ref. 8 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 11 "UM10569") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

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11. Static characteristics

Table 16. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 8.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		1.8	-	5.5	V
V_{LCD}	LCD supply voltage		2.5	-	5.5	V
I_{DD}	supply current	$f_{clk(ext)}$ = 1536 Hz; V_{DD} = 5.5 V; see Figure 21 [1]	-	3	6	µA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1536 Hz; V_{DD} = 5.5 V;V_{LCD} = 8.0 V; see Figure 21 [1]	-	22	45	µA
Logic						
V_I	input voltage		V_{SS} − 0.5	-	V_{DD} + 0.5	V
V_{IH}	HIGH-level input voltage	on pins CLK, OSC, T1 to T5, SA0	$0.7V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	on pins CLK, OSC, T1 to T5, SA0	V_{SS}	-	$0.3V_{DD}$	V
V_{OH}	HIGH-level output voltage		$0.8V_{DD}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.2V_{DD}$	V
I_{OH}	HIGH-level output current	output source current; on pin CLK; V_{OH} = 4.6 V; V_{DD} = 5 V	1	-	-	mA
I_{OL}	LOW-level output current	output sink current; on pin CLK, T1; V_{OL} = 0.4 V; V_{DD} = 5 V	1	-	-	mA
I_L	leakage current	on pins OSC, CLK, SCL, SDA, T2 to T5, SA0; V_I = V_{DD} or V_{SS}	−1	-	+1	µA
C_I	input capacitance	[3]	-	-	7	pF
I²C-bus[2]						
Input on pins SDA and SCL						
V_I	input voltage		V_{SS} − 0.5	-	5.5	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
V_{IL}	LOW-level input voltage		V_{SS}	-	$0.3V_{DD}$	V
C_I	input capacitance	[3]	-	-	7	pF
$I_{OL(SDA)}$	LOW-level output current on pin SDA	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V	3	-	-	mA

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Table 16. Static characteristics *…continued*

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 8.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

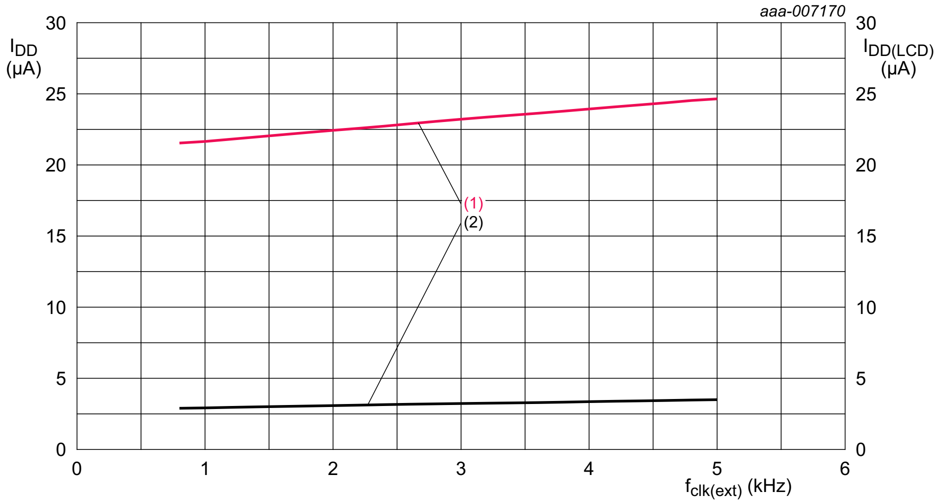
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LCD outputs						
ΔV_O	output voltage variation	on pins BP0 to BP3; C_{bpl} = 35 nF	−100	-	+100	mV
		on pins S0 to S79; C_{sgm} = 5 nF	−100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V				
		on pins BP0 to BP3 [4]	-	1.5	10	kΩ
		on pins S0 to S79 [4]	-	6.0	13.5	kΩ

[1] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I²C-bus inactive.

[2] The I²C-bus interface of PCE85133AUG is 5 V tolerant.

[3] Not tested, design specification only.

[4] Outputs measured individually and sequentially.



Conditions: V_{DD} = 5.5 V; V_{LCD} = 8 V; T_{amb} = 27 °C; all RAM filled with 0.

(1) $I_{DD(LCD)}$.

(2) I_{DD}.

Fig 21. Current consumption with respect to external clock frequency

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12. Dynamic characteristics

Table 17. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 8.0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
Internal: output pin CLK						
f_{clk}	clock frequency	[1]	2630	3600	4680	Hz
f_{fr}	frame frequency		-	150	-	Hz
Δf_{fr}	frame frequency variation		110	150	195	Hz
External: input pin CLK						
$f_{clk(ext)}$	external clock frequency		800	-	7000	Hz
$t_{clk(H)}$	HIGH-level clock time		90	-	-	µs
$t_{clk(L)}$	LOW-level clock time		90	-	-	µs
Outputs: pins BP0 to BP3 and S0 to S79						
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V	-	-	30	µs
I²C-bus: timing[2]						
Pin SCL						
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
Pin SDA						
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
Pins SCL and SDA						
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz	-	-	0.3	µs
		f_{SCL} < 125 kHz	-	-	1.0	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{w(spike)}$	spike pulse width	on bus	-	-	50	ns

[1] Typical output duty cycle of 50 %.

[2] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}. For I²C-bus timings, see Figure 24.

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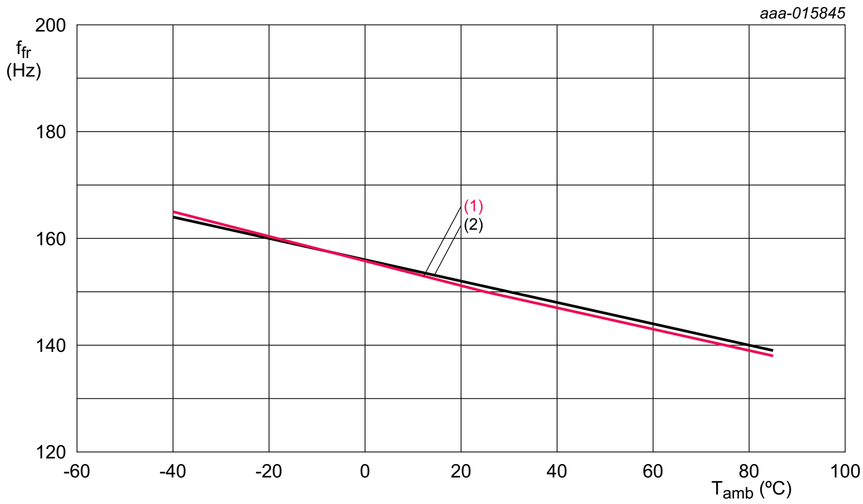

(1) V_{DD} = 5.5 V.

(2) V_{DD} = 1.8 V.

Fig 22. Frame frequency with respect to temperature

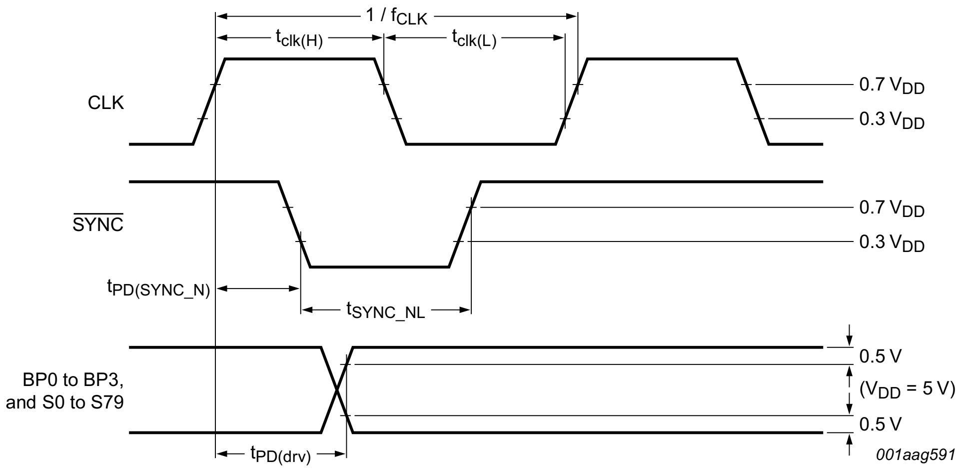

Fig 23. Driver timing waveforms

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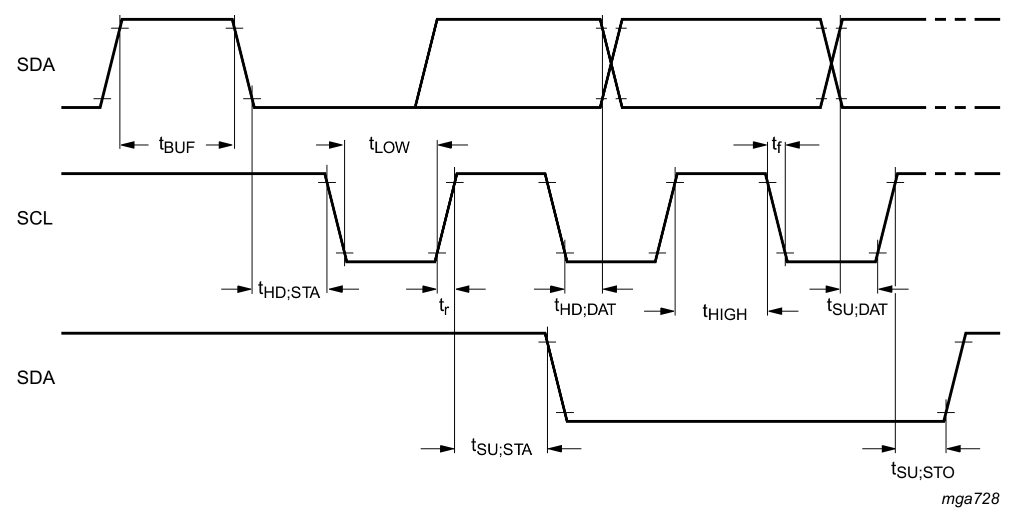

Fig 24. I²C-bus timing waveforms

13. Application information

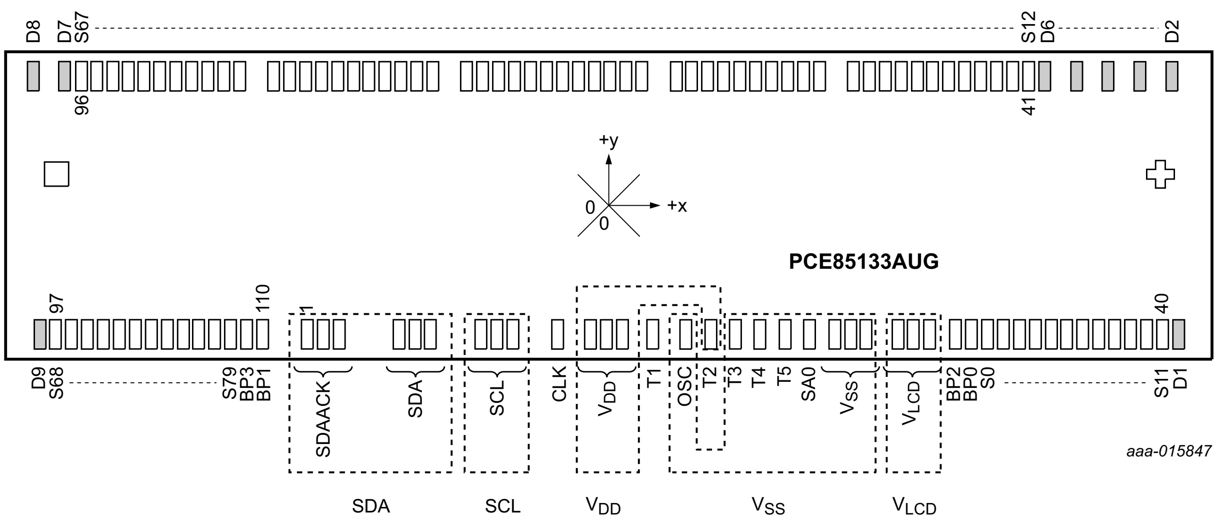

Fig 25. Schematic ITO connections when using the internal oscillator

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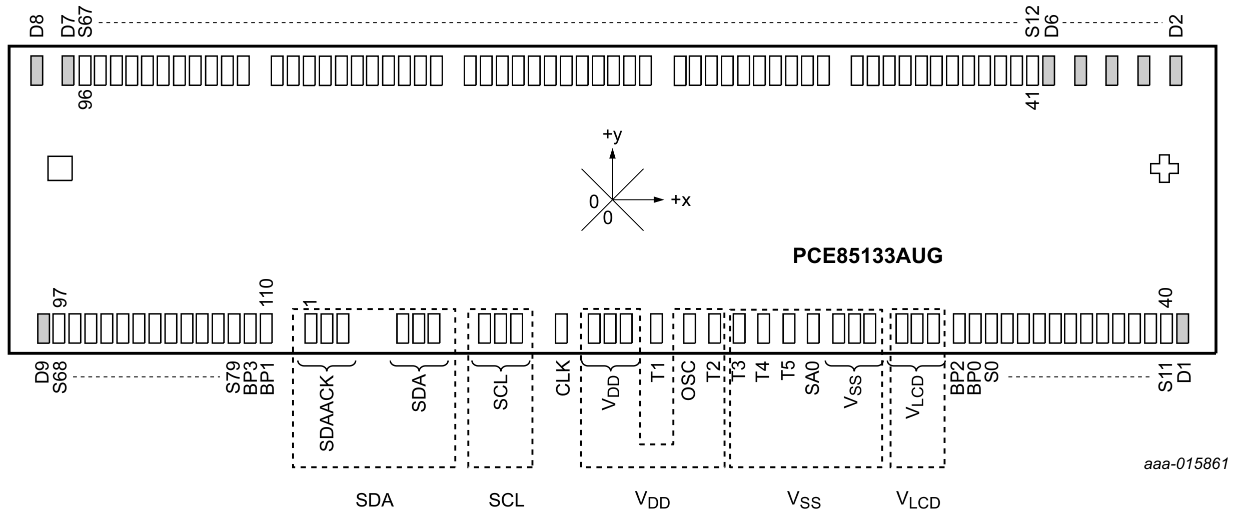

Fig 26. Schematic ITO connections when using an external oscillator

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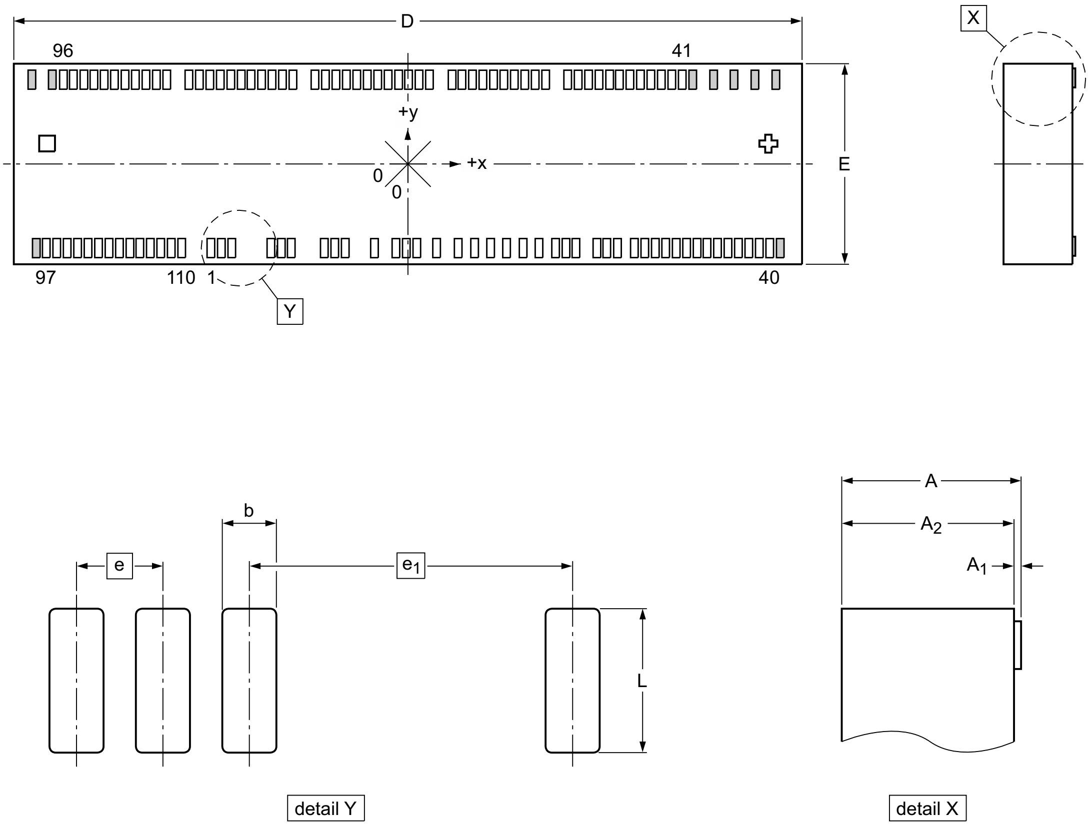
14. Bare die outline

Bare die; 110 bumps **PCE85133AUG**



Note
1. Not drawn to scale.

pce85133aug_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCE85133AUG	- - -	- - -	- - -			~~14-06-11~~ 14-06-17

Fig 27. Bare die outline of PCE85133AUG

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Table 18. Dimensions of PCE85133AUG

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	b	D	E	e	e_1	L
max	-	0.018	-	-	-	-	-	-	-
nom	0.40	0.015	0.38	0.03	4.16	1.07	0.054	0.203	0.09
min	-	0.012	-	-	-	-	-	-	-

Table 19. Bump locations of PCE85133AUG

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 27.

Symbol	Bump	X (µm)	Y (µm)	Description
SDAACK	1	–1022.67	–436.5 [1]	I²C-bus acknowledge output
SDAACK	2	–968.67	–436.5	
SDAACK	3	–914.67	–436.5	
SDA	4	–712.17	–436.5 [1]	I²C-bus serial data input
SDA	5	–658.17	–436.5	
SDA	6	–604.17	–436.5	
SCL	7	–433.17	–436.5	I²C-bus serial clock input
SCL	8	–379.17	–436.5	
SCL	9	–325.17	–436.5	
CLK	10	–173.52	–436.5	clock input and output
V_{DD}	11	–61.47	–436.5	supply voltage
V_{DD}	12	–7.47	–436.5	
V_{DD}	13	46.53	–436.5	
T1	14	149.58	–436.5	test pin
OSC	15	262.08	–436.5	oscillator select
T2	16	345.78	–436.5	test pins
T3	17	429.48	–436.5	
T4	18	513.18	–436.5	
T5	19	596.88	–436.5	
SA0	20	680.58	–436.5	I²C-bus slave address input
V_{SS}	21	765.63	–436.5	ground supply voltage
V_{SS}	22	819.63	–436.5	
V_{SS}	23	873.63	–436.5	
V_{LCD}	24	979.83	–436.5	LCD supply voltage
V_{LCD}	25	1033.83	–436.5	
V_{LCD}	26	1087.83	–436.5	
BP2	27	1176.03	–436.5	LCD backplane output
BP0	28	1230.03	–436.5	
S0	29	1284.03	–436.5	LCD segment output
S1	30	1338.03	–436.5	
S2	31	1392.03	–436.5	
S3	32	1446.03	–436.5	

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Table 19. Bump locations of PCE85133AUG

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 27.

Symbol	Bump	X (μm)	Y (μm)	Description
S4	33	1500.03	–436.5	LCD segment output
S5	34	1554.03	–436.5	
S6	35	1608.03	–436.5	
S7	36	1662.03	–436.5	
S8	37	1716.03	–436.5	
S9	38	1770.03	–436.5	
S10	39	1824.03	–436.5	
S11	40	1878.03	–436.5	
S12	41	1423.53	436.5	
S13	42	1369.53	436.5	
S14	43	1315.53	436.5	
S15	44	1261.53	436.5	
S16	45	1207.53	436.5	
S17	46	1153.53	436.5	
S18	47	1099.53	436.5	
S19	48	1045.53	436.5	
S20	49	991.53	436.5	
S21	50	937.53	436.5	
S22	51	883.53	436.5	
S23	52	829.53	436.5	
S24	53	714.06	436.5	
S25	54	660.06	436.5	
S26	55	606.06	436.5	
S27	56	552.06	436.5	
S28	57	498.06	436.5	
S29	58	444.06	436.5	
S30	59	390.06	436.5	
S31	60	336.06	436.5	
S32	61	282.06	436.5	
S33	62	228.06	436.5	
S34	63	112.59	436.5	
S35	64	58.59	436.5	
S36	65	4.59	436.5	
S37	66	–49.41	436.5	
S38	67	–103.41	436.5	
S39	68	–157.41	436.5	
S40	69	–211.41	436.5	

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Table 19. Bump locations of PCE85133AUG

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 27.

Symbol	Bump	X (μm)	Y (μm)	Description
S41	70	–265.41	436.5	LCD segment output
S42	71	–319.41	436.5	
S43	72	–373.41	436.5	
S44	73	–427.41	436.5	
S45	74	–481.41	436.5	
S46	75	–596.88	436.5	
S47	76	–650.88	436.5	
S48	77	–704.88	436.5	
S49	78	–758.88	436.5	
S50	79	–812.88	436.5	
S51	80	–866.88	436.5	
S52	81	–920.88	436.5	
S53	82	–974.88	436.5	
S54	83	–1028.88	436.5	
S55	84	–1082.88	436.5	
S56	85	–1136.88	436.5	
S57	86	–1252.35	436.5	
S58	87	–1306.35	436.5	
S59	88	–1360.35	436.5	
S60	89	–1414.35	436.5	
S61	90	–1468.35	436.5	
S62	91	–1522.35	436.5	
S63	92	–1576.35	436.5	
S64	93	–1630.35	436.5	
S65	94	–1684.35	436.5	
S66	95	–1738.35	436.5	
S67	96	–1792.35	436.5	
S68	97	–1876.05	–436.5	
S69	98	–1822.05	–436.5	
S70	99	–1768.05	–436.5	
S71	100	–1714.05	–436.5	
S72	101	–1660.05	–436.5	
S73	102	–1606.05	–436.5	
S74	103	–1552.05	–436.5	
S75	104	–1498.05	–436.5	
S76	105	–1444.05	–436.5	
S77	106	–1390.05	–436.5	
S78	107	–1336.05	–436.5	
S79	108	–1282.05	–436.5	

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Table 19. Bump locations of PCE85133AUG

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 27.

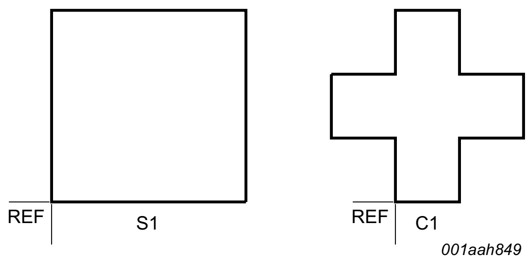
Symbol	Bump	X (μm)	Y (μm)	Description
BP3	109	−1228.05	−436.5	LCD backplane output
BP1	110	−1174.05	−436.5	
D1	-	1932.03	−436.5	dummy pads
D2	-	1909.53	436.5	
D3	-	1801.53	436.5	
D4	-	1693.53	436.5	
D5	-	1585.53	436.5	
D6	-	1477.53	436.5	
D7	-	−1846.35	436.5	
D8	-	−1953	436.5	
D9	-	−1930.05	−436.5	

[1] For most applications, SDA and SDAACK are shorted together; see Section 7.

Table 20. Gold bump hardness

Type number	Min	Max	Unit[1]
PCE85133AUG	60	120	HV

[1] Pressure of diamond head: 10 g to 50 g.



The positions of the alignment marks are approximately shown in Figure 27.

Fig 28. Alignment marks of PCE85133AUG

Table 21. Alignment mark locations

All x/y coordinates represent the position of the REF point (see Figure 28) with respect to the center (x/y = 0) of the chip; see Figure 27.

Symbol	Size (μm)	X (μm)	Y (μm)
S1	81 × 81	−1916.1	45
C1	81 × 81	1855.8	45

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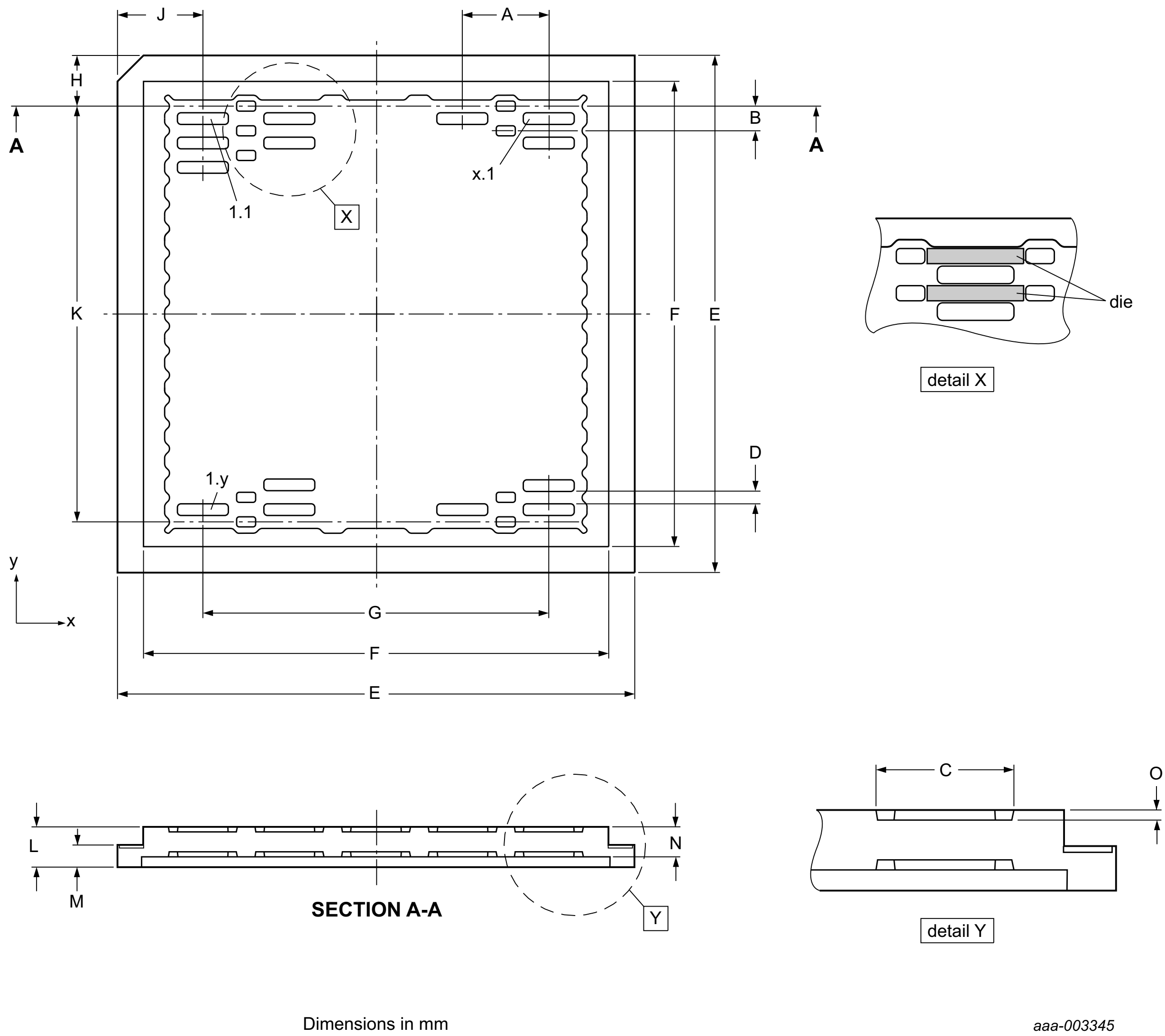
15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

16. Packing information

16.1 Packing information on the tray



Schematic drawing, not drawn to scale. Top side view. For dimensions, see Table 22. Tray has pockets on both, top side and bottom side. The IC is stored with the active side up. To get the active side down, turn the tray.

Fig 29. Tray details of PCE85133AUG

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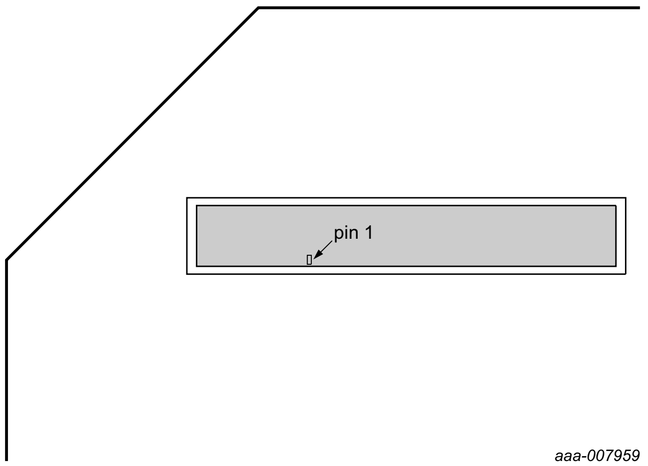
Table 22. Specification of 3 inch tray details

Tray details are shown in Figure 29. Nominal values without production tolerances.

Tray details														
Dimensions														
A	B	C	D	E	F	G	H	J	K	L	M	N	O	Unit
6.0	2.5	4.26	1.17	76.0	68.0	60.0	6.75	8.0	62.5	4.2	2.6	3.2	0.48	mm
Number of pockets														
x direction							y direction							
11							26							



The orientation of the IC in a pocket with active side up is indicated by the position of pin 1 with respect to the chamfer on the upper left corner of the tray.

Fig 30. Die alignment in the tray

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17. Appendix

17.1 LCD segment driver selection

Table 23. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8553DTT	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^{2}C / SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^{2}C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCA8547AHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	I^{2}C	TQFP64	Y
PCA8547BHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^{2}C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	–40 to 95	I^{2}C	LQFP80	Y
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^{2}C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	I^{2}C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCF8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	I^{2}C	TSSOP56	N
PCF8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCA8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^{2}C	TSSOP56	Y
PCA8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 85	I^{2}C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	I^{2}C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^{2}C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^{2}C	Bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^{2}C	Bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^{2}C	Bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^{2}C	Bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110[2]	N	N	–40 to 85	I^{2}C	Bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110[2]	N	N	–40 to 95	I^{2}C	Bare die	Y

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Table 23. Selection of LCD segment drivers *...continued*

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA85233UG	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	150, 220[2]	N	N	–40 to 105	I²C	Bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 85	I²C	Bare die	N
PCA8530DUG	102	204	-	408	-	-	-	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 105	I²C / SPI	Bare die	Y
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 95	I²C	Bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	117 to 176[1]	N	N	–40 to 95	I²C	Bare die	Y
PCF8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 85	I²C / SPI	Bare die	N
PCA8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 105	I²C / SPI	Bare die	Y

[1] Software programmable.

[2] Hardware selectable.

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18. Abbreviations

Table 24. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
COG	Chip-On-Glass
DC	Direct Current
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
MM	Machine Model
RAM	Random Access Memory
RC	Resistance-Capacitance
RMS	Root Mean Square

19. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10706 —** Handling bare die

[3] **AN10853 —** ESD and EMC sensitivity of IC

[4] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[5] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[6] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[7] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **UM10204 —** I^2C-bus specification and user manual

[11] **UM10569 —** Store and transport requirements

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20. Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCE85133AUG v.2	20150722	Product data sheet	-	PCE85133AUG v.1
Modifications:	• Figure 1 "Block diagram of PCE85133AUG" is updated.			
PCE85133AUG v.1	20150318	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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