PIC16F627A/628A/648A

PIC16F627A/628A/648A Rev. A Silicon/Data Sheet Errata

The PIC16F627A/628A/648A parts you have received conform functionally to the Device Data Sheet (DS40044**F**), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the **PIC16F627A/628A/648A silicon**. Where noted, issues apply to listed revision only.

1. Module: Programming Operations

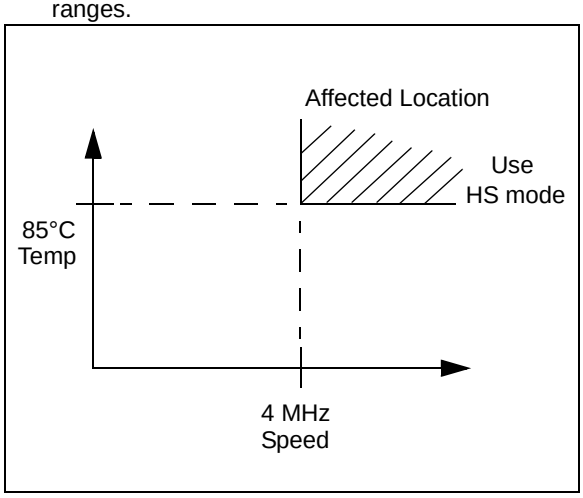
1. PIC16F627A/628A silicon Rev. A3. Accessing of the data EEPROM memory in Low Voltage Programming (LVP) mode.
   - The data EEPROM memory cannot be accessed when programming in LVP mode.
   - The Flash program memory and the Configuration bits can be accessed properly in LVP mode.
2. PIC16F627A/628A silicon Rev. A3 and A4. Flash program memory can only be programmed with a VDD of 4.5V-5.5V.
3. PIC16F627A/628A silicon Rev. A6 and PIC16F648A silicon Rev. A3.
   - The Flash program memory is able to be programmed with a VDD of 2.0V-5.5V.
   - For code protection security, the Flash program memory can only be erased using the Bulk Erase command. The Bulk Erase function of all current and future revisions of the PIC16F627A/628A/648A requires a VDD of 4.5V-5.5V.

2. Module: EC Clock

1. PIC16F648A Silicon Rev. A1.

   When using the EC OSC mode at frequencies >4 MHz and temperatures >85°C, the part may execute incorrectly from the program memory, causing malfunction.

   This problem only affects E-temp parts. Industrial grade parts are unaffected. HS mode should be used for frequencies >4 MHz at extended temps. All other clock modes work to their specified ranges.



Note:	This problem is corrected in PIC16F648A Rev. A3. (Date code 0420XXX and later.)

2. PIC16F627A/628A Silicon revision A3, A4 and A5. PIC16F648A Silicon revision A1.

   Unexpected program execution may occur when waking from Sleep.

   Work around

   Use HS Clock mode.

Note:	This problem is corrected in PIC16F648A Rev. A3 and PIC16F627A/628A Rev. A6. (Date code 0420XXX and later.)

3. Module: Data EEPROM Memory

1. PIC16F648A Silicon revision A1 and A3 and PIC16F627A/628A silicon revision A3, A4, A5 and A6.

Note:	This problem is corrected in PIC16F648A Rev. A5 and PIC16F627A/628A Rev. A8.

Unexpected program execution may occur during data EEPROM write cycles.

Work around

Execute a SLEEP instruction immediately after setting the EECON1 WR bit and allow the EEIF to wake the processor from Sleep. This requires the PEIE bit of the INTCON register and the EEIE bit of the PIE1 register to be set. All other interrupt enables must be cleared so that only the EE write completion will wake the processor.

Note:	Most peripherals suspend operation during Sleep. Other precautions may be necessary to ensure all peripheral operations are complete or in a safe halted mode before beginning an EEPROM write.

The following example assumes that the desired address is present in the EEADR register and the desired data to be written is in the EEDATA register:

EXAMPLE 1: DATA EEPROM WRITE CODE EXAMPLE

```
BANKSEL  0X00          ;select Bank0
BCF      PIR1, EEIF    ;ensure write complete
                       ;flag is clear
BANKSEL  0x80          ;change to Bank1
MOVLW    1 << PEIE     ;enable only
                       ;peripheral interrupt
MOVWF    INTCON        ;
MOVLW    1 << EEIE     ;enable only EE write
                       ;complete interrupt
MOVWF    PIE1          ;
BSF      EECON1, WREN  ;enable EE write
MOVLW    0x55          ;required write
                       ;protect squence
MOVWF    EECON2        ;
MOVLW    0xAA          ;second part of
                       ;sequence
MOVWF    EECON2        ;
BSF      EECON1, WR    ;initiate write
SLEEP                  ;suspend operation
                       ;during write
BCF      EECON1,WREN   ;disable EE write
                       ;program execution
                       ;resumes with this
                       ;instruction upon EE
                       ;write completion
```

2. The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work around

- Avoid operations on the PIR1 register when writing to the EEPROM memory.
- Poll the WR bit (EECON1<1>) to determine when the write is complete.
- Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer Interrupt Service Routine to verify the EEPROM write success.
- If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

4. Module: USART Control

1. USART control of the RB1/RX/DT and RB2/TX/CK differs from the data sheet. Figure 5-9 and Figure 5-10 indicate that the USART circuit overrides the output drivers via the Peripheral OE signal. In fact, the Peripheral OE signal forces the TRISB<2:1> to an output (Reset) state (see Figure 1). Subsequently, the TRISB<2:1> must be set or configured to receive data.

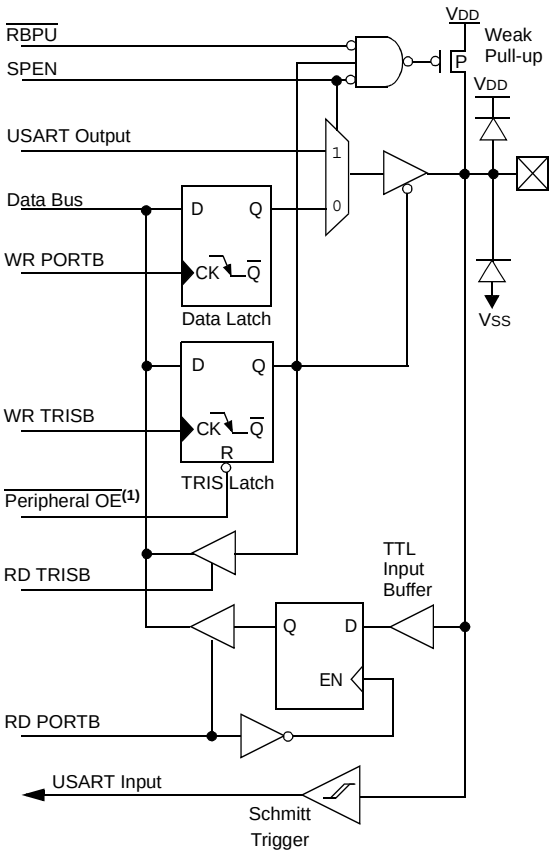
   Work around

   In Asynchronous mode, when transmit is enabled (TXEN = 1 and SPEN = 1), the TRISB<2> latch is cleared to '0' by the USART peripheral circuitry. When disabling transmit (TXEN = 0), the TRISB<2> bit should be set to '1' to configure the RB2/TX/CK pin as an input.

   In Synchronous mode, when changing from transmit to receive, clear the TXEN bit first, then set TRISB<1> to '1' to configure the RB1/RX/DT pin as an input before setting SREN or CREN to receive.

   When disabling the USART (SPEN = 0), TRIS<2:1> should be reconfigured for input or output as required by the application.

FIGURE 1: BLOCK DIAGRAM OF RBI, RB2



Note 1: Peripheral OE (output enable) is only active if peripheral select is active.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40044F), the following clarifications and corrections should be noted.

1. Module: In-Circuit Serial Programming™

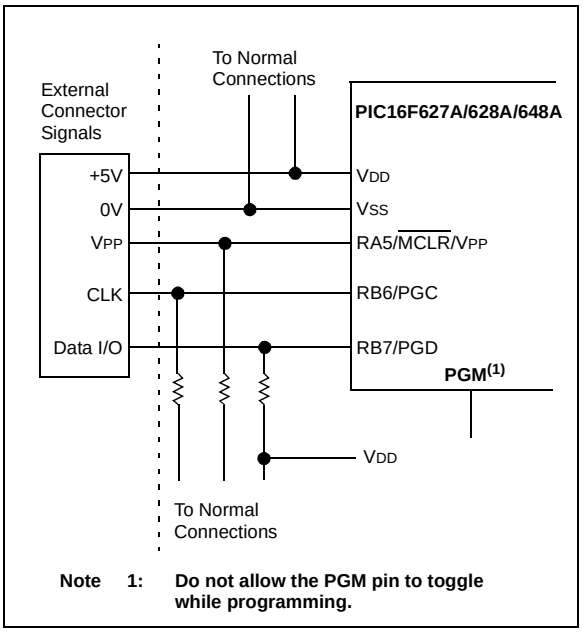
Section 14.11: In-Circuit Serial Programming and Figure 14-18: Typical In-Circuit Serial Programming Connection. The following paragraph and Note box are being added to the end of Section 14.11 and Figure 14-18 is updated to include PGM, noted in bold.

14.11 In-Circuit Serial Programming

If LVP is not being used for programming, but the LVP Configuration bit is set (or LVP feature is enabled), the PGM pin must not be allowed to toggle while programming. The PGM pin is edge sensitive and if an edge is detected during programming, it may cause the PC to reset. If the LVP feature is disabled, the PGM pin will have no effect on programming.

Note:	The LVP feature is enabled by default when the LVP Configuration bit is set.

FIGURE 14-18: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING™ CONNECTION



Note 1: Do not allow the PGM pin to toggle while programming.

2. Module: Electrical Specifications (Internal Oscillator Parameters)

Replace Table 17-5: Precision Internal Oscillator Parameters with the folowing updated table.

TABLE 17-5: INTERNAL OSCILLATOR PARAMETERS

Para. No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
F10	FIOSCFAST	Fast Oscillator Frequency	3.96	4	4.04	MHz	VDD = 3.5 V, 25°C
			3.92	4	4.08	MHz	2.0 V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C
			3.80	4	4.20	MHz	2.0 V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (IND) -40°C ≤ TA ≤ +125°C (EXT)
F11	FIOSCSLOW	Slow Oscillator Frequency (Internal, uncalibrated)	31.4	48	78.62	kHz	2.0 V ≤ VDD ≤ 5.5V, 25°C
F14	Tioscst	Oscillator Wake-up from Sleep start-up time	—	6	8	µs	VDD = 2.0V, -40°C to +85°C
			—	4	8	µs	VDD = 3.0V, -40°C to +85°C
			—	3	5	µs	VDD = 5.0V, -40°C to +85°C

APPENDIX A: REVISION HISTORY

Rev. A Document (2/12/03)

First revision of this document.

Rev. B Document (3/26/03)

Added 4.5V-5.5V VDD programming requirement on Rev. A2, A3 & A4 silicon.

Rev. C Document (5/13/03)

Added Item 1 to Clarifications/Corrections Section; Instruction Set, Example 1: (SUBWF).

Rev. D Document (7/10/03)

Revised document title.

Item 1: Added Module 2: EC Clock for PIC16F648A silicon. Clarifications/Corrections to the Data Sheet, Added Module 2: Timing Diagrams and Specifications, Table 17-4.

Item 2: Added correction to 28-Pin QFN package, Pin 1.

Rev. E Document (8/15/03)

Module 2: EC Clock: Added Item 2: "PIC16F627A/628A Silicon revision A1, A2, A3 and A4. PIC16F648A Silicon revision A1".

Added Module 3: Data EEPROM Memory, Item 1.

Clarifications/Corrections to the Data Sheet: Added Module 4: I/O Ports, Module 5: Timer1 and Module 6: Data EEPROM Memory.

Rev. F Document (9/03/03)

Module 1: Corrections to Item 2. Module 2: Corrections to Item 2. Module 3: Corrections to Item 1.

Clarifications/Corrections to the Data Sheet: Module 2: Timing Diagrams and Specifications, added Item 2, corrections to Section 17.2, parameter D020.

Rev. G Document (12/12/03)

Revise second paragraph, first page. Module 3, Item 1: Add note. Clarifications/Corrections to the Data Sheet: Module 2: Corrections to Item 2 and Table 17.2. Module 2: Added item 3 and corrections to Table 17.2 and 17.3. Module 4: Add Figure 5-4 from Data Sheet. Module 6: Corrections to Example 13-4.

Rev. H Document (01/15/04)

Module 1: Update to Item 2, added Item 3. Module 2: Add note to Items 1 and 2. Clarifications/Corrections to the Data Sheet: Added Module 7: Correction to Table 17-6. Corrected Table and Figure numbers in Section 17.0. Added Module 8: Correction to Sections 6.2.1 and 7.3.1, Table references.

Rev. J Document (06/02/04)

Revised note, Module 2: EC Clock; Items 1 and 2. Revised note, Module 3: Data EEPROM Memory; Item 1. Clarifications/Corrections to the Data Sheet; Data Sheet Module 2: Timing Diagrams and specifications; parameters D033 and D043 updated to Rev. B of data sheet.

Rev. K Document (11/2004)

Added Item 2 to Module 3: "Data EEPROM Memory" for PIC16F627A/628A/648A silicon.

Rev. L Document (4/2005)

Added Module 4: "USART Control" for PIC16F627A/628A/648A silicon.

Clarifications/Corrections to the Data Sheet: Removed all modules. The data sheet has been updated.

Rev. M Document (2/2007)

Clarifications/Corrections to the Data Sheet: Added Module 1: In-Circuit Serial Programming.

Rev. N Document (11/2008)

Clarifications/Corrections to the Data Sheet: Added Module 2: Electrical Specifications (Internal Oscillator Parameters).

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