

High Efficiency Thyristor

$$V_{RRM} = 800 \text{ V}$$

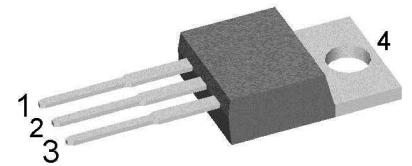
$$I_{TAV} = 20 \text{ A}$$

$$V_T = 1,31 \text{ V}$$

Single Thyristor

Part number

CS19-08ho1



Backside: anode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-220

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Terms Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact the sales office, which is responsible for you.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you.

Should you intend to use the product in aviation, in health or live endangering or life support applications, please notify. For any such application we urgently recommend

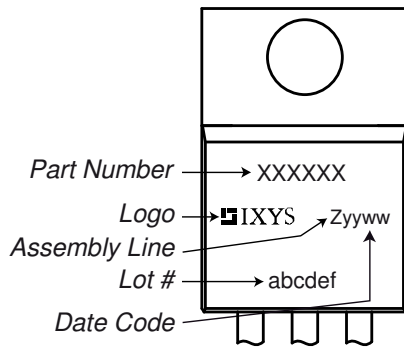
- to perform joint risk and quality assessments;

- the conclusion of quality agreements;

- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

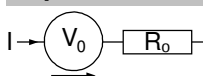
Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			900	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}C$			800	V
I_{RD}	reverse current, drain current	$V_{R/D} = 800 V$	$T_{VJ} = 25^{\circ}C$		50	μA
		$V_{R/D} = 800 V$	$T_{VJ} = 125^{\circ}C$		1	mA
V_T	forward voltage drop	$I_T = 20 A$	$T_{VJ} = 25^{\circ}C$		1,32	V
		$I_T = 40 A$			1,65	V
		$I_T = 20 A$	$T_{VJ} = 125^{\circ}C$		1,31	V
		$I_T = 40 A$			1,73	V
I_{TAV}	average forward current	$T_C = 110^{\circ}C$	$T_{VJ} = 125^{\circ}C$		20	A
$I_{T(RMS)}$	RMS forward current	180° sine			31	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 125^{\circ}C$		0,86	V
r_T	slope resistance				22	m Ω
R_{thJC}	thermal resistance junction to case				0,7	K/W
R_{thCH}	thermal resistance case to heatsink			0,50		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}C$		170	W
I_{TSM}	max. forward surge current	$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 45^{\circ}C$		180	A
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		195	A
		$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 125^{\circ}C$		155	A
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		165	A
I^2t	value for fusing	$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 45^{\circ}C$		160	A ² s
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		160	A ² s
		$t = 10 ms$; (50 Hz), sine	$T_{VJ} = 125^{\circ}C$		120	A ² s
		$t = 8,3 ms$; (60 Hz), sine	$V_R = 0 V$		115	A ² s
C_J	junction capacitance	$V_R = 230 V$ $f = 1 MHz$	$T_{VJ} = 25^{\circ}C$		9	pF
P_{GM}	max. gate power dissipation	$t_p = 30 \mu s$	$T_C = 125^{\circ}C$		5	W
		$t_p = 300 \mu s$			2,5	W
P_{GAV}	average gate power dissipation				0,5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}C$; $f = 50 Hz$ repetitive, $I_T = 60 A$			150	A/ μs
		$t_p = 200 \mu s$; $di_G/dt = 0,15 A/\mu s$; $I_G = 0,15 A$; $V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 20 A$			500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		500	V/ μs
		$R_{GK} = \infty$; method 1 (linear voltage rise)				
V_{GT}	gate trigger voltage	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		1,5	V
			$T_{VJ} = -40^{\circ}C$		2,5	V
I_{GT}	gate trigger current	$V_D = 6 V$	$T_{VJ} = 25^{\circ}C$		28	mA
			$T_{VJ} = -40^{\circ}C$		50	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}C$		0,2	V
I_{GD}	gate non-trigger current				3	mA
I_L	latching current	$t_p = 10 \mu s$	$T_{VJ} = 25^{\circ}C$		75	mA
		$I_G = 0,1 A$; $di_G/dt = 0,1 A/\mu s$				
I_H	holding current	$V_D = 6 V$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}C$		50	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}C$		2	μs
		$I_G = 0,1 A$; $di_G/dt = 0,1 A/\mu s$				
t_q	turn-off time	$V_R = 100 V$; $I_T = 20 A$; $V = \frac{2}{3} V_{DRM}$ $T_{VJ} = 100^{\circ}C$ $di/dt = 10 A/\mu s$ $dv/dt = 20 V/\mu s$ $t_p = 200 \mu s$		150		μs

Package TO-220			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			35	A
T_{VJ}	virtual junction temperature		-40		125	°C
T_{op}	operation temperature		-40		100	°C
T_{stg}	storage temperature		-40		150	°C
Weight				2		g
M_D	mounting torque		0,4		0,6	Nm
F_C	mounting force with clip		20		60	N

Product Marking


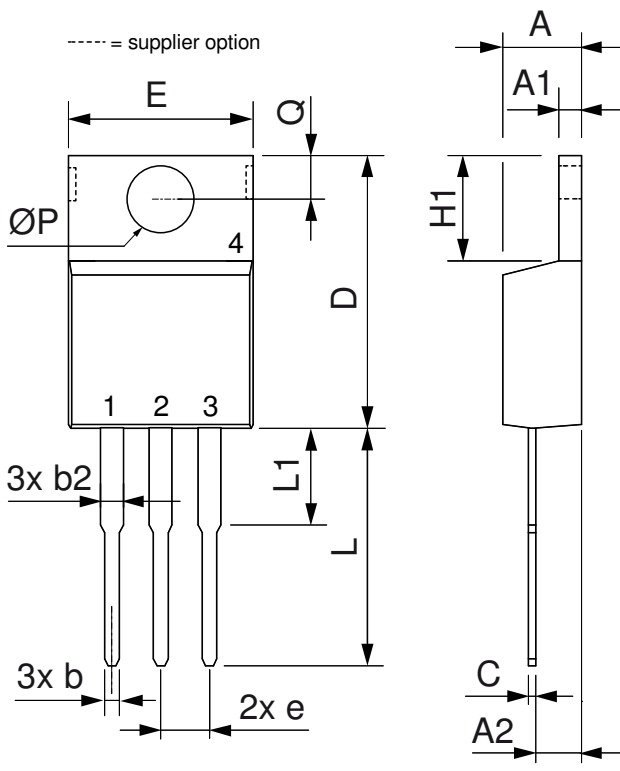
Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CS19-08ho1	CS19-08ho1	Tube	50	471038

Similar Part	Package	Voltage class
CS19-08ho1S	TO-263AB (D2Pak) (2)	800
CS19-12ho1	TO-220AB (3)	1200
CS19-12ho1S	TO-263AB (D2Pak) (2)	1200

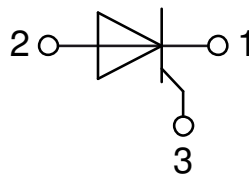
Equivalent Circuits for Simulation
** on die level*
 $T_{VJ} = 125\text{ °C}$

Thyristor

$V_{0\ max}$	threshold voltage	0,86	V
$R_{0\ max}$	slope resistance *	19	mΩ

Outlines TO-220



Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.32	4.82	0.170	0.190
A1	1.14	1.39	0.045	0.055
A2	2.29	2.79	0.090	0.110
b	0.64	1.01	0.025	0.040
b2	1.15	1.65	0.045	0.065
C	0.35	0.56	0.014	0.022
D	14.73	16.00	0.580	0.630
E	9.91	10.66	0.390	0.420
e	2.54	BSC	0.100	BSC
H1	5.85	6.85	0.230	0.270
L	12.70	13.97	0.500	0.550
L1	2.79	5.84	0.110	0.230
ØP	3.54	4.08	0.139	0.161
Q	2.54	3.18	0.100	0.125



Thyristor

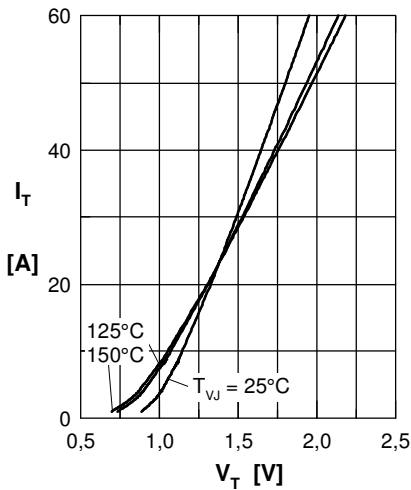


Fig. 1 Forward characteristics

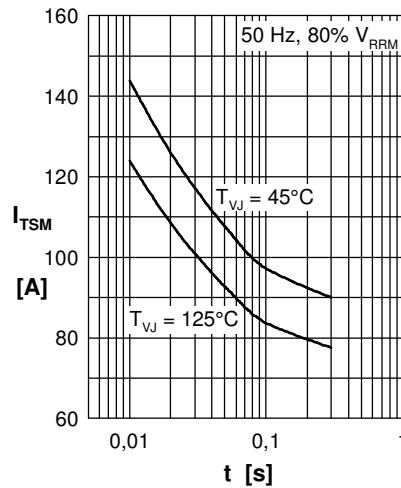


Fig. 2 Surge overload current

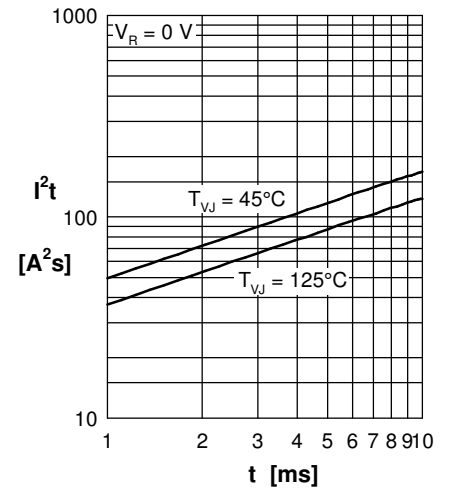


Fig. 3 I^2t versus time (1-10 ms)

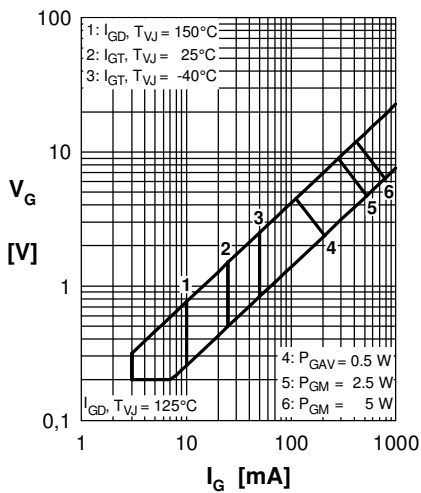


Fig. 4 Gate trigger characteristics

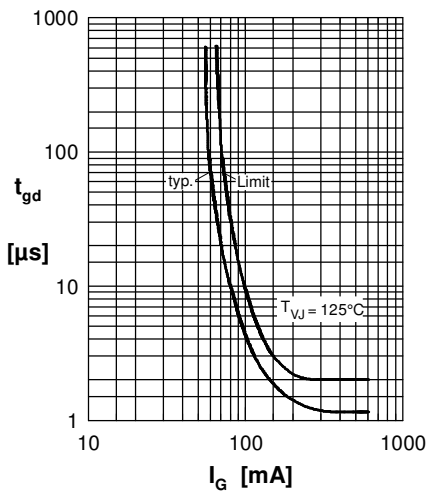


Fig. 5 Gate controlled delay time

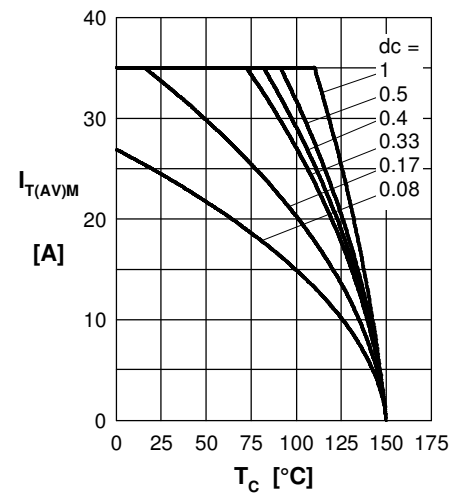


Fig. 6 Max. forward current at case temperature

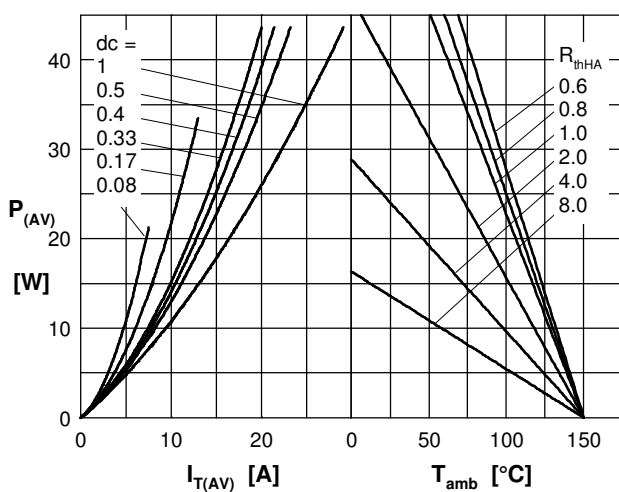


Fig. 7a Power dissipation versus direct output current
Fig. 7b and ambient temperature

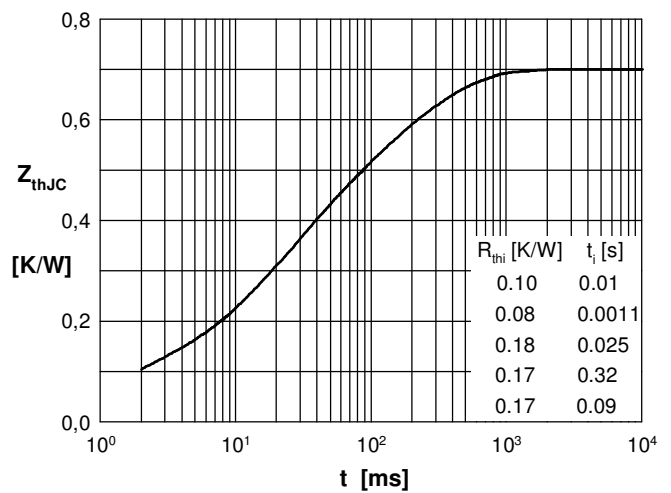


Fig. 8 Transient thermal impedance junction to case