

8-Channel Ultra-Low Phase Noise Continuous Waveform Transmitter with Beamformer

Features

- 8-Channel Ultrasound Continuous Waveform (CW) Transmitter with Integrated Beamformer
- CW Output $\pm 1V$ to $\pm 6V_{p-p}$ with Low R_{ON}
- -160 dbc/Hz Ultra-Low Phase Noise at 1 kHz Offset and 5 MHz
- 8-Bit Programmable Per-Channel Beamforming Phase Delay
- 8-Bit Programmable Dividers for CW Frequency with Input Clock Frequency up to 250 Mhz
- Input Clock Compatible with LVDS/SSTL or Single-Ended LVCMOS
- LVCMOS 2.5V Logic for the Control I/O pins
- Fast SPI Interface Supports up to 200 MHz
- SPI Interface Supports Daisy Chaining and Broadcasting Mode

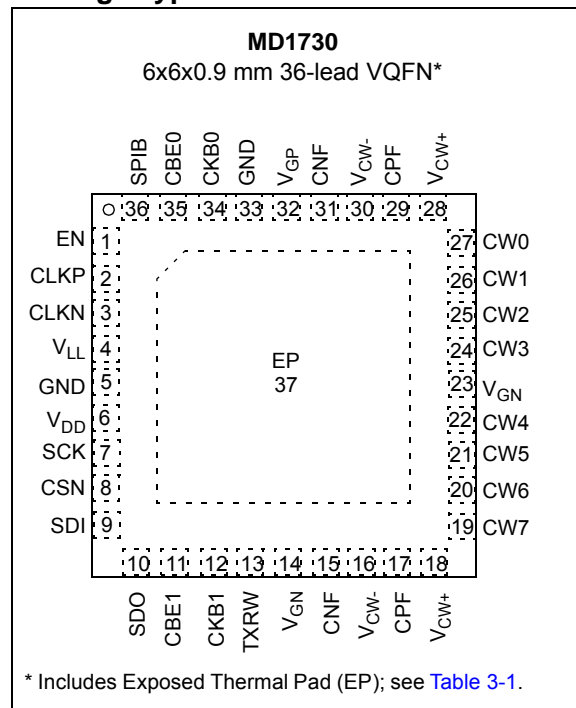
Applications

- Medical Ultrasound Imaging System for Cardiovascular Application
- Ultrasound Fetal Heart Monitoring Device
- Ultrasound Flow Meter
- Programmable Array Pattern Generator

General Description

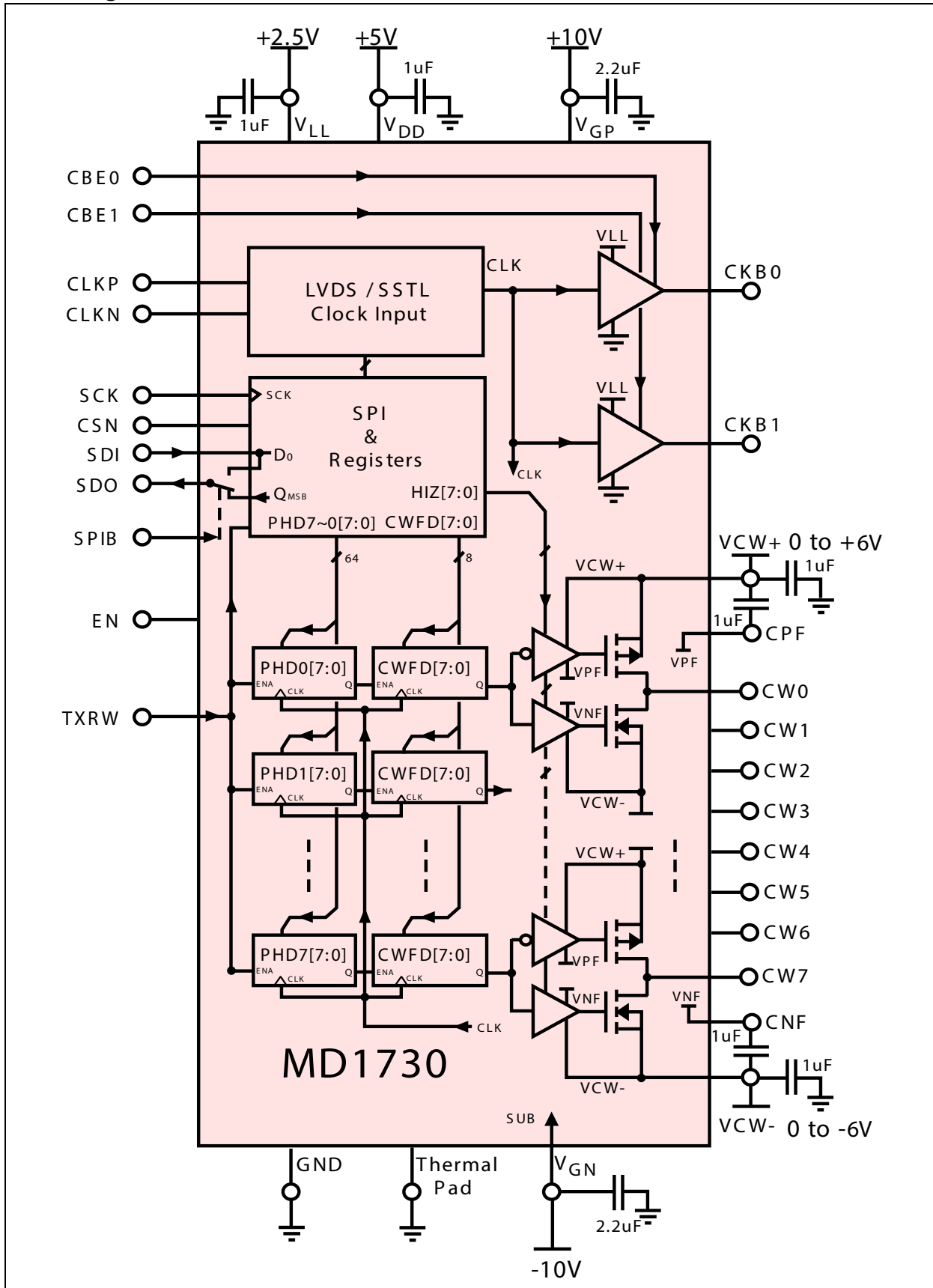
The MD1730 is an 8-channel ultra-low phase noise CW transmitter with integrated beamformer. It is designed for medical ultrasound imaging systems requiring high-performance CW Doppler mode. The MD1730 has a dedicated signal path designed to minimize phase noise to the output. In addition, it has a high-speed SPI interface that enables CW beamforming features. The outputs of the MD1730 can swing up to $\pm 6V$ and each output has a separate programmable phase delay. Additionally, by programming the internal frequency divider register, the MD1730 can output different CW frequencies from a single clock source. For instance, when the input clock frequency is 160 MHz and the frequency divider is set to 16, an output CW frequency of 5 MHz can be obtained with a phase delay step size of 6.25 ns, which translates to an angular resolution of 11.25 degrees.

Package Type

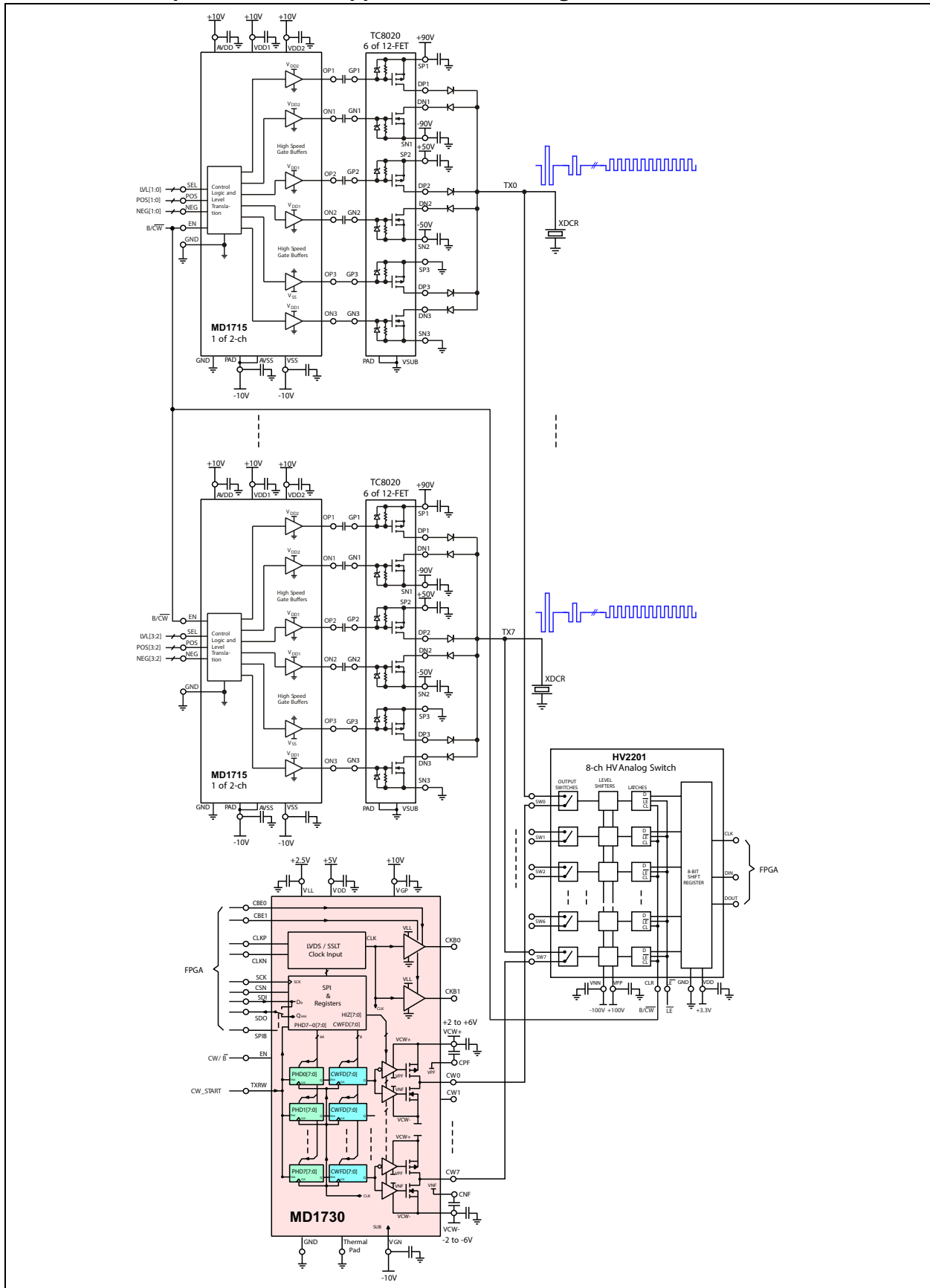


MD1730

Block Diagram



MD1730 CW Output via HV2201 Application Block Diagram



MD1730

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Positive Logic Supply (V_{LL}).....	-0.5V to +3.0V
Positive Supply Voltage (V_{DD}).....	-0.5V to +6.0V
Positive Supply Voltage (V_{GP}).....	-0.5V to +13.5V
Negative Supply Voltage (V_{GN}).....	+0.5V to -13.5V
CW Output Positive Supply Voltage (V_{CW+}).....	-0.5V to +12V
CW Output Negative Supply Voltage (V_{CW-}).....	+0.5V to -12V
All Digital Inputs (V_{IN}).....	-0.5V to +3.0V
CW Outputs (V_{OUT}).....	-12V to +12V
Operating Ambient Temperature	0°C to +85°C
Maximum Junction Temperature	0°C to +85°C
Storage Temperature	+125°C
Thermal Resistance Junction to Ambient (Θ_{JA} , JESD51-5).....	25°C/W
Thermal Resistance Junction to Bottom Cu Pad (Θ_{JB} , JESD51-5)	6.4°C/W
Thermal Resistance Junction to Package Top (Θ_{JC} , JESD51-5).....	13.5°C/W
ESD Rating All Pins	±1.0 kV

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: INPUT/OUTPUT PIN DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^\circ C$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Supply						
Logic Supply Voltage	V_{LL}	2.35	2.50	2.65	V	$(V_{GP} + V_{CW-}) \geq 10V$ $(V_{GN} + V_{CW+}) \geq 10V$ $T_A = 0$ to +85°C, Note 2
VDD Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
Positive Supply Voltage	V_{GP}	8.0	10	12	V	
Negative Supply Voltage	V_{GN}	-12	-10	-8.0	V	
CW Output Positive Supply	V_{CW+}	1.0	—	6.0	V	
CW Output Negative Supply	V_{CW-}	-6.0	—	-1.0	V	
V_{LL} Quiescent Current	I_{LLQ}	—	0.02	0.1	mA	EN = 0, $f_{CLK} = f_{SCK} = 0$ All logic input no transit
V_{DD} Quiescent Current	I_{DDQ}	—	0.15	0.2	mA	
V_{GP} Quiescent Current	I_{GPQ}	—	1.0	2.0	µA	
V_{GN} Quiescent Current	I_{GNQ}	—	33	45	µA	
V_{CW+} Quiescent Current	I_{CW+Q}	—	26	45	µA	
V_{CW-} Quiescent Current	I_{CW-Q}	—	6	10	µA	
V_{LL} Enabled Current	I_{LLEN}	—	6.0	9.0	mA	EN = 1, $f_{SCK} = 120$ MHz TXRW = 0, SDI = 0, SDO no load.
V_{DD} Enabled Current	I_{DDEN}	—	0.2	0.3	mA	
V_{GP} Enabled Current	I_{GPEN}	—	2.0	3.0	mA	
V_{GN} Enabled Current	I_{GNEN}	—	2.0	3.0	mA	
V_{CW+} Enabled Current	I_{CW+EN}	—	2.0	3.0	mA	
V_{CW-} Enabled Current	I_{CW-EN}	—	2.0	3.0	mA	

Note 1: Characterized only; not 100% tested in production.

2: Design Guidance Only (DGO).

MD1730

TABLE 1-1: INPUT/OUTPUT PIN DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^{\circ}C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{LL} Current at CW 5MHz	I_{LL5}	—	2.5	3.0	mA	EN = 1, $f_{CLK} = 80$ MHz, TXRW = 1, CW 5 MHz, no load 8-channel
V_{DD} Current at CW 5MHz	I_{DD5}	—	1.0	2.0	mA	
V_{GP} Current at CW 5MHz	I_{GP5}	—	6.0	10	mA	
V_{GN} Current at CW 5MHz	I_{GN5}	—	12	18	mA	
V_{CW+} Current at CW 5MHz	I_{CW+5}	—	26	35	mA	
V_{CW-} Current at CW 5MHz	I_{CW-5}	—	21	30	mA	
SPI & Logic						
Input Logic High Voltage	V_{IH}	$0.8 V_{LL}$	—	V_{LL}	V	2.5V LVCMOS
Input Logic Low Voltage	V_{IL}	0	—	$0.2 V_{LL}$	V	
Input Logic High Current	I_{IH}	—	—	1.0	μA	
Input Logic Low Current	I_{IL}	—	—	—	μA	
SPI and Logic Input Capacitance	C_{IN}	—	4.5	—	pF	Note 1
Output Logic High Current	I_{OH}	—	—	—	mA	2.5V LVCMOS
Output Logic Low Current	I_{OL}	—	—	—	mA	
SDO Output Logic High Voltage	V_{OH}	—	—	—	V	with 5 pF load
SDO Output Logic Low Voltage	V_{OL}	—	—	0.35	V	

Note 1: Characterized only; not 100% tested in production.

2: Design Guidance Only (DGO).

TABLE 1-2: SPI AND LOGIC AC ELECTRICAL SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^{\circ}C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Rise Time	t_r	—	0.65	—	ns	1.5 pF load, Note 1
Output Fall Time	t_f	—	0.65	—		
Output Rise Propagation Delay	t_{dr}	—	2.8	—	ns	CLK rise 50% to output 50%, after latency. Note 1
Output Fall Propagation Delay	t_{df}	—	3.0	—		
Delay Time Matching	t_{dm}	—	± 0.5	± 1.0	ns	Channel to channel, Note 1, $f_{CLK} = 80$ MHz
SDI Valid to SCK, Setup Time	t_1	0.6	1.0	—	ns	Note 1
SCK To SDI Data Hold Time	t_2	2.0	—	—	ns	
SCK High Time % of $1/f_{CLK}$	t_3	45	—	55	%	Note 2
SCK Low Time % of $1/f_{CLK}$	t_4	45	—	55	%	
CSN Hi-Time	t_5	2-cycle	—	—	SCK	Note 2
SCK Rise to CSN Rise	t_6	—	2.0	—	ns	Note 1
CSN Low to SCK Rise	t_7	—	0.8	—	ns	
SDO Valid from SCK Rise	t_8	—	3.1	4.0	ns	SPIB = 0, 1.5 pF Load, Note 1
CSN Rise to SCK Rise	t_9	—	2.0	—	ns	Note 1
CSN Rise to TXRW or SPIB Rise	t_{10}	9-cycle			SCK	Note 2
TXRW or SPIB Fall to CSN Fall	t_{11}	1-cycle				

Note 1: Characterized only; not 100% tested in production.

2: Design Guidance Only (DGO).

TABLE 1-2: SPI AND LOGIC AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^{\circ}C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
SDO to SDI Valid Delay	t_{12}	—	2.3	3.0	ns	SPIB = 1, 1.5 pF Load, Note 1
TXRW Rise to CLKP Rise	t_{13}	—	2.5	—	ns	Note 1
Latency to CW Wave Rise	t_{14}	2-cycle			CLK	After TXRW = 1, PHD=0, Note 2
Latency CSN Rise to TXRW Fall	t_{15}	2-cycle	—	—	CLK	Note 2
SCK Clock Frequency	f_{SCK}	—	—	200	MHz	Note 1
EN Off Time	t_{EN-Off}	—	20	30	ns	Note 2
EN On Time	t_{EN-On}	—	150	300	μs	2.0 μF on CPF/CNF, Note 2

Note 1: Characterized only; not 100% tested in production.

2: Design Guidance Only (DGO).

TABLE 1-3: CLOCK BUFFER OUTPUTS AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^{\circ}C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Clock Output Frequency Range	f_{CKB}	40	160	250	MHz	Note 1
Clock Output Duty Cycle	D%	45	—	55	%	Note 2
CKB0,1 Rise Time	t_{rb}	—	0.6	1.0	ns	$f_{CLK} = 80$ Mhz, 1.5 pF load, Note 1
CKB0,1 Fall Time	t_{fb}	—	0.5	1.0		
Output Rise Propagation Delay	t_{drb}	—	2.0	3.0	ns	CLK rise to CKB, 50%, Note 1
Output Fall Propagation Delay	t_{dfb}	—	2.0	3.0		
CBE Enable Time	t_{cbe}	—	2.1	3.0		
CKB0,1 Output logic high	V_{OHCKB}	—	V_{LL}	—	V	Note 2
CKB0,1 Output Logic low	V_{OLCKB}	—	GND	—	V	Note 2

Note 1: Characterized only; not 100% tested in production.

2: Design Guidance Only (DGO).

TABLE 1-4: CW OUTPUTS DC/AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^{\circ}C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
CW Output Peak to Peak Voltage	V_{CWOUT}	-6.0	-	+6.0	V	
CW Output Rise Propagation Delay	t_{drCW}	—	4.0	6.0	ns	TxCLK 50% to CWx 10%, after latency, Note 1
CW Output Fall Propagation Delay	t_{dfCW}	—	4.0	6.0		
CW Output Maximum Current	$I_{CW\pm}$	± 250	± 300	—	mA	$V_{CW\pm} = \pm 5.0V$, 0.1 Ω load, Note 1

Note 1: Characterized only; not 100% tested in production.

2: Design Guidance Only (DGO).

MD1730

TABLE 1-4: CW OUTPUTS DC/AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^{\circ}C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Static Output Resistance PFET	R_{ONCW}	—	7.5	12	Ω	RON at $V_{CW\pm} = \pm 5.0V$, $I_{CW\pm} = \pm 100$ mA load, Note 1
Static Output Resistance NFET		—	6.5	11		
Change in $R_{DS(ON)}$ with Temperature	ΔR_{ONCW}	—	—	1.0	%/C	$V_{CW\pm} = \pm 5.0V$, Note 2
CW Phase Resolution	RE_{Phase}	—	1	—	CLK	Note 2
CW Phase Noise	N_{Phase}	—	-160	—	dBc/Hz	CW 5 MHz, 1 kHz Offset, Note 1

Note 1: Characterized only; not 100% tested in production.

Note 2: Design Guidance Only (DGO).

TABLE 1-5: LVDS / SSTL CLOCK INPUTS AC / DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, $V_{LL} = +2.5V$, $V_{GP} = +10V$, $V_{GN} = -10V$, $V_{CW+} = +6.0V$, $V_{CW-} = -6.0V$, $V_{DD} = +5V$, $T_A = 25^{\circ}C$.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
CLKP/CLKN Clock Frequency	f_{CLK}	40	160	250	MHz	Note 1
Clock Input Slew Rate	t_{CSR}	1.0	—	—	V/ns	Note 2
Control/Data Input Slew Rate	t_{DSR}	1.0	—	—	V/ns	
Single Ended Clock Input						
SSTL Reference Voltage	V_{REFS}	1.13	1.25	1.38	V	Note 1
DC Input Logic High	$V_{IH(DC)}$	$V_{REFS} + 0.15$	—	$V_{LL} + 0.3$	V	Note 1
DC Input Logic Low	$V_{IL(DC)}$	-0.3	—	$V_{REFS} - 0.15$	V	Note 1
AC Input Logic High	$V_{IH(AC)}$	$V_{REFS} + 0.31$	—	—	V	$V_{REF} = 0.5V_{LL}$, Slew rate 1.0 V/ns, Note 1
AC Input Logic Low	$V_{IL(AC)}$	-	—	$V_{REFS} - 0.31$	V	
Differential Clock Input						
AC Differential Cross Point	$V_{X(AC)}$	$0.5V_{LL} - 0.2$	—	$0.5V_{LL} + 0.2$	V	CLK and \overline{CLK} , Note 1
DC Input Max Swing Voltage	$V_{SWING(DC)}$	0.3	—	$V_{LL} + 0.6$	V	Note 1
AC Differential Input Voltage	$V_{SWING(AC)}$	0.62	—	$V_{LL} + 0.6$	V	Note 1
DC Input Signal Voltage	$V_{IN(DC)}$	-0.3	—	$V_{LL} + 0.3$	V	Note 1
CLKP/CLKN Slew Rate	SLEW	1.0	—	—	V/ns	Note 2

Note 1: Characterized only; not 100% tested in production.

Note 2: Design Guidance Only (DGO).

NOTES:

MD1730

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

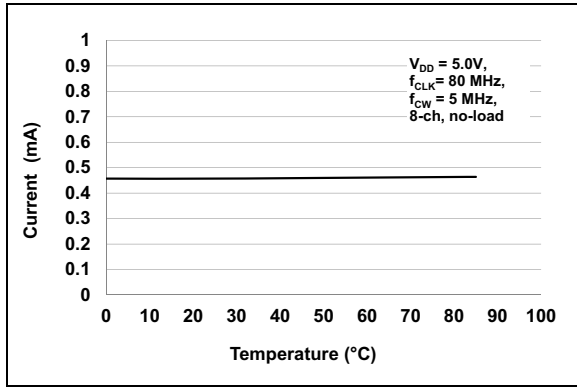


FIGURE 2-1: I_{DD} vs. Temperature.

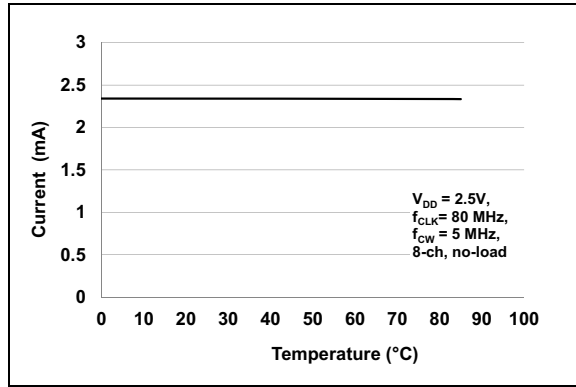


FIGURE 2-4: I_{VLL} vs. Temperature.

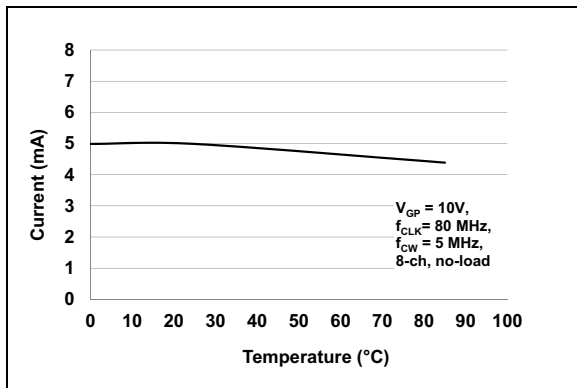


FIGURE 2-2: I_{VGP} vs. Temperature.

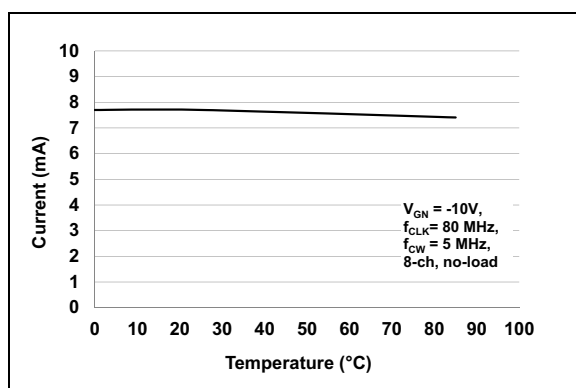


FIGURE 2-5: I_{VGN} vs. Temperature.

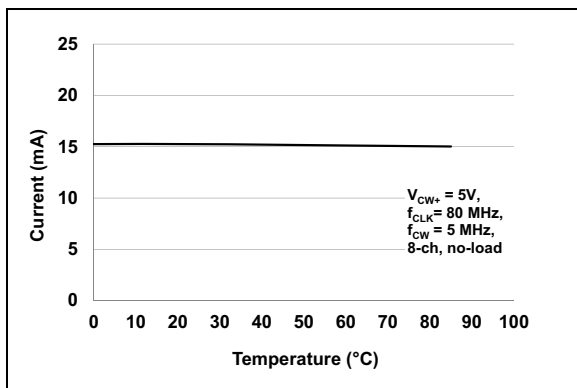


FIGURE 2-3: I_{VCW+} vs. Temperature.

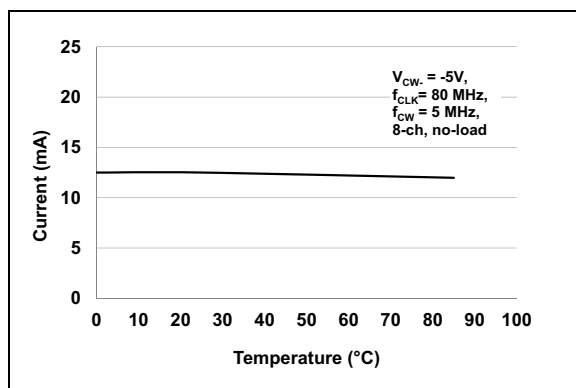


FIGURE 2-6: I_{VCW-} vs. Temperature.

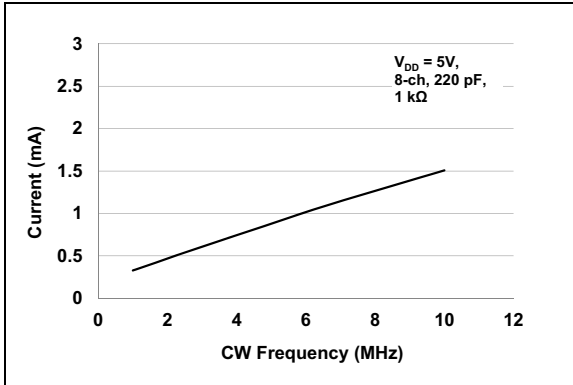


FIGURE 2-7: I_{VDD} vs. CW Output Frequency.

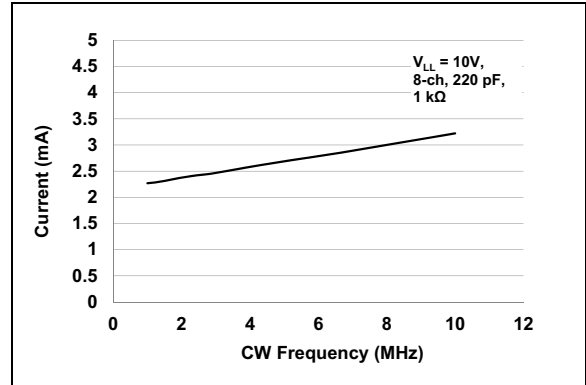


FIGURE 2-10: I_{VLL} vs. CW Output Frequency.

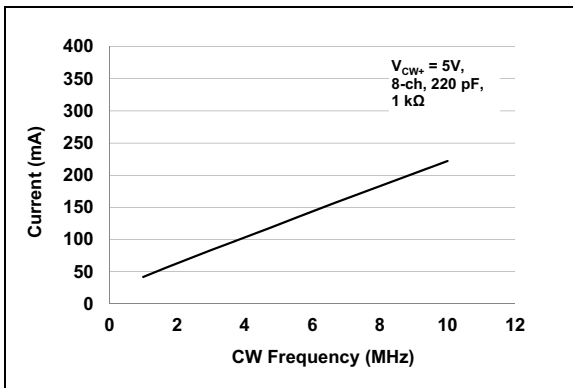


FIGURE 2-8: I_{VCW+} vs. CW Output Frequency.

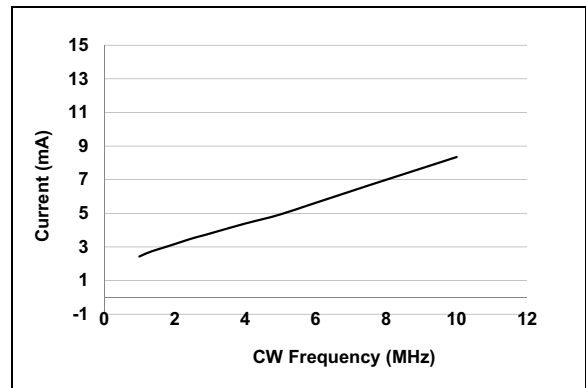


FIGURE 2-11: I_{VGN} vs. CW Output Frequency.

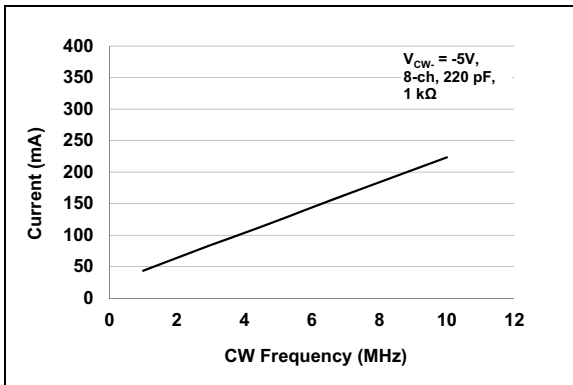


FIGURE 2-9: I_{VCW-} vs. CW Output Frequency.

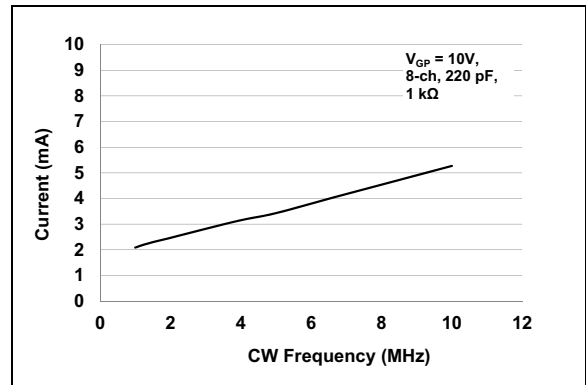


FIGURE 2-12: I_{VGP} vs. CW Output Frequency.

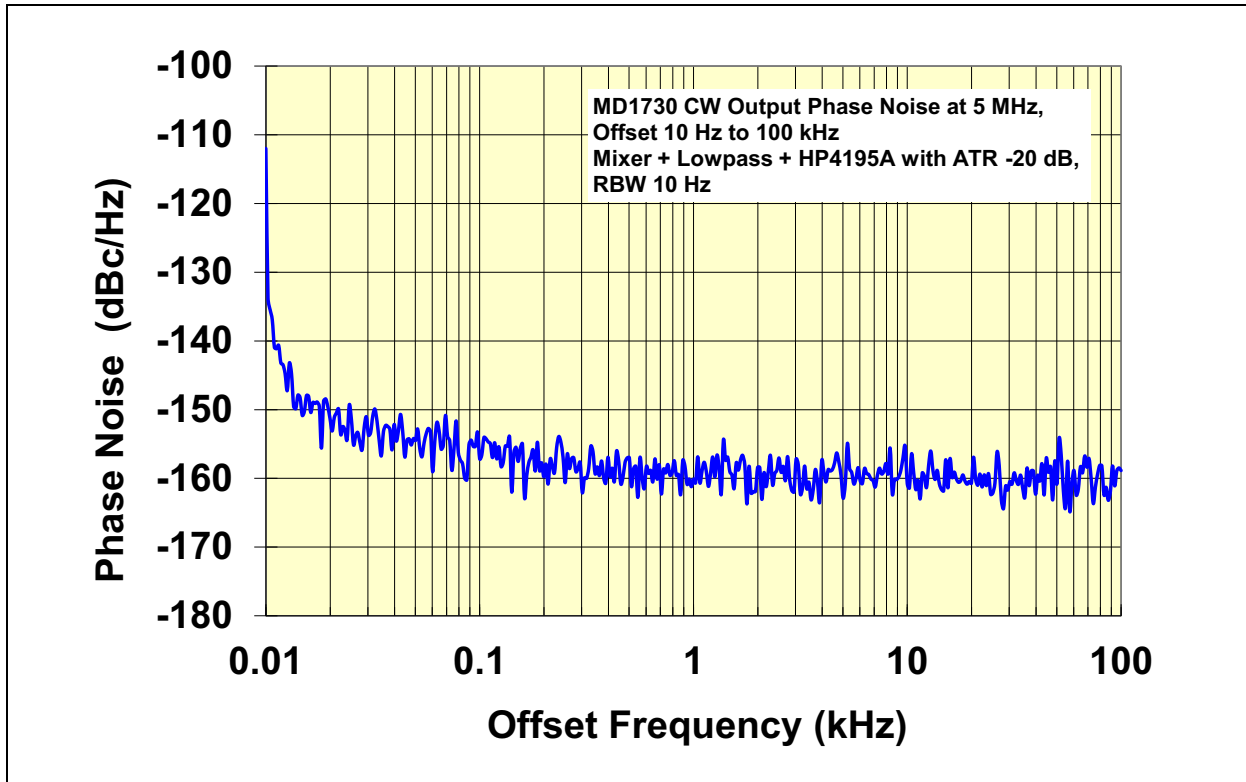


FIGURE 2-13: Typical CW Output Phase Noise Curves.

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

6x6 VQFN	Symbol	Pin Function
1	EN	Device Enable Input. When EN = 0, the SPI and the internal regulator are disabled. The device is enabled when EN = 1. Note that the EN pin has no control over the clock buffers, as the clock buffers have their dedicated enable pins.
2	CLKP	Positive Input of the Internal System Clock and is compatible with LVDS/SSTL. For LVCMOS 2.5V input refer to Figure 4-8 .
3	CLKN	Negative Input of the Internal System Clock and is compatible with LVDS/SSTL. For LVCMOS 2.5V input refer to Figure 4-8 .
4	V _{LL}	+2.5V Positive Voltage Power Supply, it requires a 1.0 μ F decoupling capacitor to GND
5, 33	GND	Ground, 0V
6	V _{DD}	+5V Positive Voltage Power Supply, it requires a 1.0 μ F decoupling capacitor to GND
7	SCK	Serial Peripheral Interface (SPI) clock input
8	CSN	Serial Peripheral Interface (SPI) chip-select. CSN is an active-low signal.
9	SDI	Serial Peripheral Interface (SPI) data input
10	SDO	Serial Peripheral Interface (SPI) data output
11, 35	CBE0-1	The clock buffer enable pin. When CBE _n = 0, the corresponding clock buffer is disabled. The clock buffer is enabled otherwise.
12, 34	CKB0-1	2.5V Single-ended Clock Buffer output pins
13	TXRW	CW Transmission Control pin. When TXRW = 0, the SPI is enabled for read/write. When TXRW = 1, the SPI is disabled and the CW transmission is started.
14, 23	V _{GN}	-10V Negative Voltage Power Supply, it requires a 2.2 μ F capacitor to GND. The V _{GN} supply is also the substrate and should be the most negative supply to the chip.
15, 31	CNF	Negative Floating Supply Bypass Capacitor pin. Connects 1 μ F/10V capacitor between this pin and the V _{CW-} pin.
16, 30	V _{CW-}	-1V to -6V Negative Voltage Power Supply for the CW output, it requires a 1.0 μ F decoupling capacitor per pin to GND
17, 29	CPF	Positive Floating Supply Bypass Capacitor pin. Connects 1 μ F/10V capacitor between this pin and the V _{CW+} pin.
18, 28	V _{CW+}	+1V to +6V Positive Voltage Power Supply for the CW output. It requires a 1.0 μ F decoupling capacitor per pin to GND.
19, 20, 21, 22, 24, 25, 26, 27	CW0-7	Channel 0-7 CW Waveform Output
32	V _{GP}	+10V Positive Voltage Power Supply, it requires a 2.2 μ F decoupling capacitor to GND
36	SPIB	SPI Broadcasting Mode pin. When SPIB = 1, the broadcast mode is enabled.
37	EP	Exposed Thermal Pad (EP); must be connected to GND

MD1730

NOTES:

4.0 DEVICE DESCRIPTION

4.1 Operation Description

The MD1730 is an 8-channel ultra-low phase noise monolithic CW transmitter. It consists of an SPI interface to program internal phase delay registers and frequency dividers to facilitate CW beamforming. It supports differential LVDS/SSTL and single-ended 2.5V LVCMOS clock inputs. The MD1730's output path is designed to provide ultra-low phase noise and can swing up to $\pm 6V$. The following sections provide a detailed overview of MD1730's feature set and operation.

4.2 Using The Built-in Clock Buffers

The MD1730 has two built-in single ended clock output buffers. The MD1730 can accept LVDS, SSTL25 and LVCMOS 2.5V clock at its input and provide a single-ended output buffered clock. The clock buffers are independent of the chip's main EN pin and each output clock buffer can be enabled or disabled separately using the CBE0 or CBE1 pin. The maximum clock frequency of the buffers is 250 MHz. The output timing diagram for the clock buffers is shown in [Figure 4-5](#). As shown in the diagram CKB0 and CKB1, clock outputs are only dependent on CBE0 and CBE1 respectively. This feature makes it convenient to drive the TX pulser retiming clock input, such as the HV7321. Using the built in clock buffers will save the cost of additional buffers, reduce PCB area, simplify the system clock distribution design and improve power savings as well.

4.3 SPI Registers Description

REGISTER 4-1: SPI CONTROL REGISTER DESCRIPTION

Data Bits	Description
W/R	The W/R is the read write control bit. When W/R = 1, the SPI writes the data provided at the addressed register. When W/R = 0, the SPI reads the data stored from the appropriate register. The read operation is disabled when SPIB = 1.
CWFD<7:0>	The CWFD<7:0> register stores the divisor value for setting the CW output frequency. The CW output frequency is set by using the equation ($f_{CW} = f_{CLK}/(2 * CWFD)$) except CWFD = 0. For CWFD = 0 the CW output frequency is $f_{CW} = f_{CLK}/2 * 512$. The CW output frequency ranges from $(f_{CLK}/512) \leq f_{CW} \leq (f_{CLK}/2)$. The register's initial value is 0.
PHD _{CH} <7:0>	PHD _{CH} <7:0> sets the phase delay for each individual channel. The equation for the output delay time is $PHD<7:0>/f_{CLK} + 2/f_{CLK}$ once TXRW goes high. The register initial value is 0. Refer to Figure 4-4 for further details.
HIZ _{CH}	HIZ _{CH} bit enables the channel output when the corresponding bit is 0. The channel is disabled and its' output becomes high Z when the corresponding bit is 1. The default register value is 0.

Note: CH denotes channel number 0 to 7.

MD1730

REGISTER 4-2: SPI REGISTER ADDRESS AND CONTROL BITS

W/R	SPI Register ADD<3:0>				Write or Read Data <7:0>							
	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
1 = Write 0 = Read MSB first. (See Section 4.3 and Section 4.4)	0	0	0	0	Channel 0 phase delay PHD0<7:0>							
	0	0	0	1	Channel 1 phase delay PHD1<7:0>							
	0	0	1	0	Channel 2 phase delay PHD2<7:0>							
	0	0	1	1	Channel 3 phase delay PHD3<7:0>							
	0	1	0	0	Channel 4 phase delay PHD4<7:0>							
	0	1	0	1	Channel 5 phase delay PHD5<7:0>							
	0	1	1	0	Channel 6 phase delay PHD6<7:0>							
	0	1	1	1	Channel 7 phase delay PHD7<7:0>							
	1	0	0	0	HIZ7	HIZ6	HIZ5	HIZ4	HIZ3	HIZ2	HIZ1	HIZ0
	1	0	0	1	CW frequency divisor number CWFD<7:0>							

Note: Power-On or EN = 0 sets all the registers to 0.

TABLE 4-1: PHD<7:0> PHASE DELAY TIME REGISTER DESCRIPTION

PHD<7:0>	Delay Time to Start Transmitting
00000000	0/f _{CLK} (Power-on default)
00000001	1/f _{CLK}
00000010	2/f _{CLK}
.....
11111110	254/f _{CLK}
11111111	255/f _{CLK}

TABLE 4-2: CWFD<7:0> CW FREQUENCY DIVIDER REGISTER DESCRIPTION

CWFD[7:0]	Transmit CW Frequency f _{CW}
00000000	f _{CLK} /512 (Power-on default)
00000001	f _{CLK} /2
00000010	f _{CLK} /4
00000011	f _{CLK} /6
.....
11111110	f _{CLK} /508
11111111	f _{CLK} /510

Note: The selected CW frequency is same for all the CW0~7 outputs: f_{CW} = f_{CLK}/2*CWFD. The CW frequency applies to all channels.

4.4 Serial Peripheral Interface (SPI)

The MD1730's SPI is used to program the phase delay and frequency divider registers. The SPI supports writing at speed up to 200 MHz and the MSB is shifted in first. SPI interface supports two operating modes: daisy chain mode and broadcasting mode.

When SPIB = 0, the MD1730 is in daisy chain mode. In this mode, it supports both read and write operations.

When SPIB = 1 the chip enters the "Broadcasting" mode. In this mode, the SDI data shifts into the shift register as well as to the SDO output. In this mode, the user can write the same register of different daisy chained chips with the same value in a single write

transaction. However, when SPIB = 1 the read operation is disabled. To verify the written data for each chip, the user can revert SPIB = 0 and perform a normal read operation.

4.4.1 SPI WRITE OPERATION EXAMPLES

The following is a 1-byte writing example for the register at ADD = 0011b with the data D<7:0> = 01010101 when SPIB = TXRW = 0.

1. The Write operation starts with setting CSN to low.
2. The SCK clock is used to shift in the following SDI data:

D12 = 1, W/R bit set equal to high for write operation.

ADD<11:8> = 0011b, address for channel-3's phase delay register.

D<7:0> = 01010101b, data to be written into channel-3's phase delay register.

The SDI data is shifted in at the rising edge of SCK.

- Once the complete data has been shifted in, the CSN should be taken high to finish the writing operation. The SDI data is latched into channel-3's phase delay register on the rising edge of the CSN signal. CSN has to be kept high for a minimum of 2-SCK cycles for the data to be written into the appropriate register.

In the case of eight chips daisy chained together as shown in [Figure 4-3](#), there should be 13 x 8 = 104 cycles of SCK before the CSN is taken high.

The MD1730 can also be used in the Broadcasting mode to write several daisy chained chips with the same data. The Broadcasting mode can be used to reduce the time required to write the SPI if several MD1730 chips need the same data. The following is a 1-byte writing example for the register at the address location ADD = 0011b with data D<7:0> = 01010101b while the MD1730 is set to broadcasting mode.

- The write operation starts with setting CSN to low with TXRW = 0 and SPIB = 1.
- The SCK clock is used to shift in the following SDI data to the first MD1730 chip:

D12 = 1, W/R bit set equal to high for write operation.

ADD<11:8> = 0011b, address for the channel-3's phase delay register.

D<7:0> = 01010101, data to be written into the channel-3's phase delay register.

The SDI data is shifted in at the rising edge of SCK.

In Broadcasting mode, the same set of data shifted into the first chip's SDI is sent to all the MD1730 chips along the daisy chain. As shown in [Figure 4-3](#) when SPIB = 1 an internal switch connects the SDI and SDO directly.

- Once the complete data has been shifted in, the CSN should be taken high to finish the writing operation. The SDI data is latched into each chip's channel-3 phase delay register on the rising edge of the CSN signal. CSN has to be kept high for a minimum of 2-SCK cycles for the data to be written into the appropriate register.

4.4.2 SPI READ OPERATION EXAMPLES

The following is a 2-byte reading example from the register at ADD = 0011b (Channel-3's phase delay register) when SPIB = TXRW = 0.

- The read operation starts with setting CSN to low.
- The SCK clock is used to shift in the following SDI data:

D12 = 0, W/R bit set equal to high for read operation.

ADD<11:8> = 0011b, address for channel-3's phase delay register.

D<7:0> = x, for a Read operation the data field is don't care.

The SDI data is shifted in at the rising edge of SCK.

- Once the complete data has been shifted into the SPI the CSN is taken high. While CSN is high the MD1730 fetches the data located at ADD<11:9> = 0011b and places it in its internal shift register.
- Once the complete data has been shifted in, the CSN should be taken high to finish the reading operation. While CSN is high the MD1730 fetches the data located at ADD<11:9> = 0011b and places it in its internal shift register. CSN has to be kept high for a minimum of 2-SCK cycles for the data to be fetched and placed into the internal shift register.
- The CSN is taken low and during the next 13 SCK clock cycles, the fetched data in the internal shift register is clocked out on the rising edge of SCK from the SDO of the MD1730.

MD1730

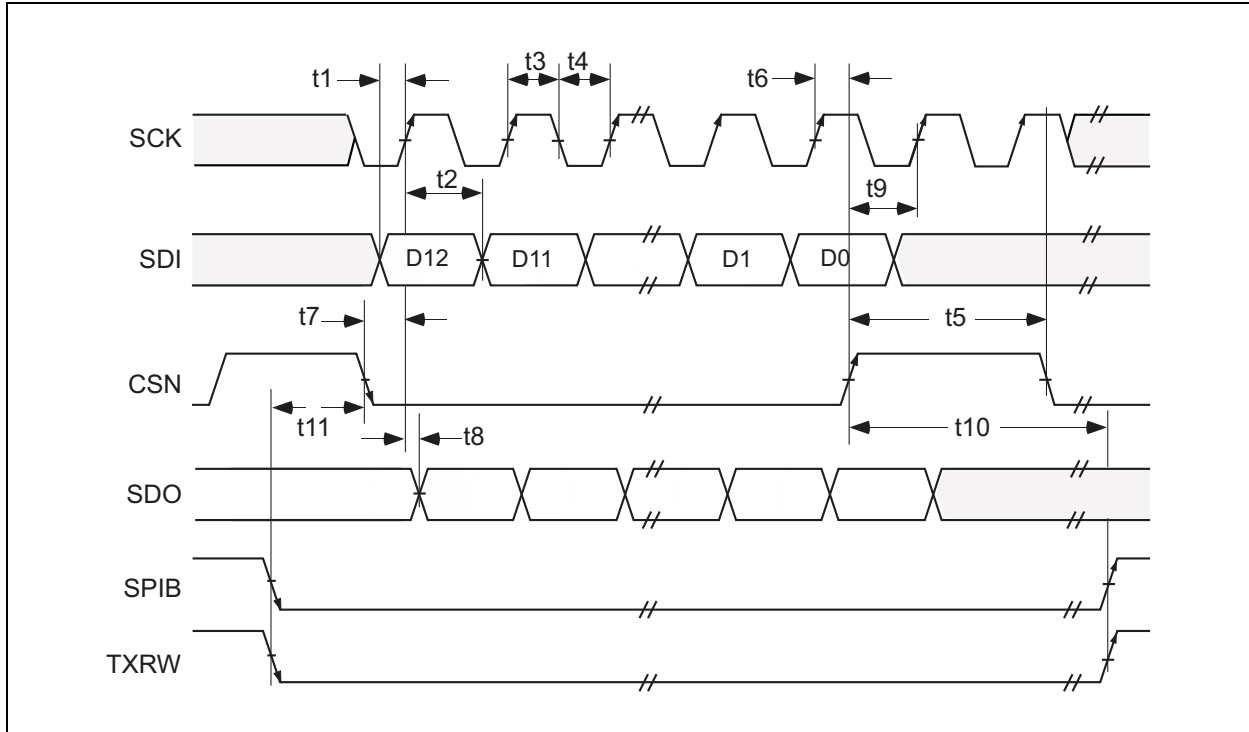


FIGURE 4-1: SPI Register Read/Write Timing with SPIB = 0, TXRW = 0.

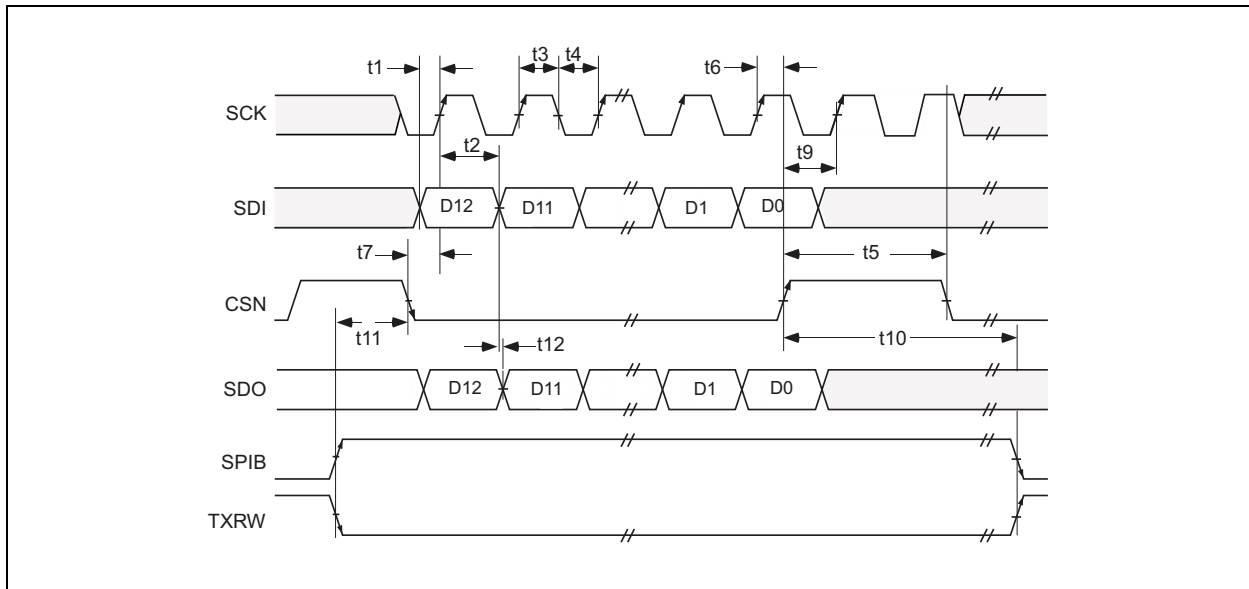


FIGURE 4-2: SPI Register Broadcasting Write Timing with SPIB = 1, TXRW = 0.

Note: When in SPIB = 1 mode, the SPI register READ operations are not available.

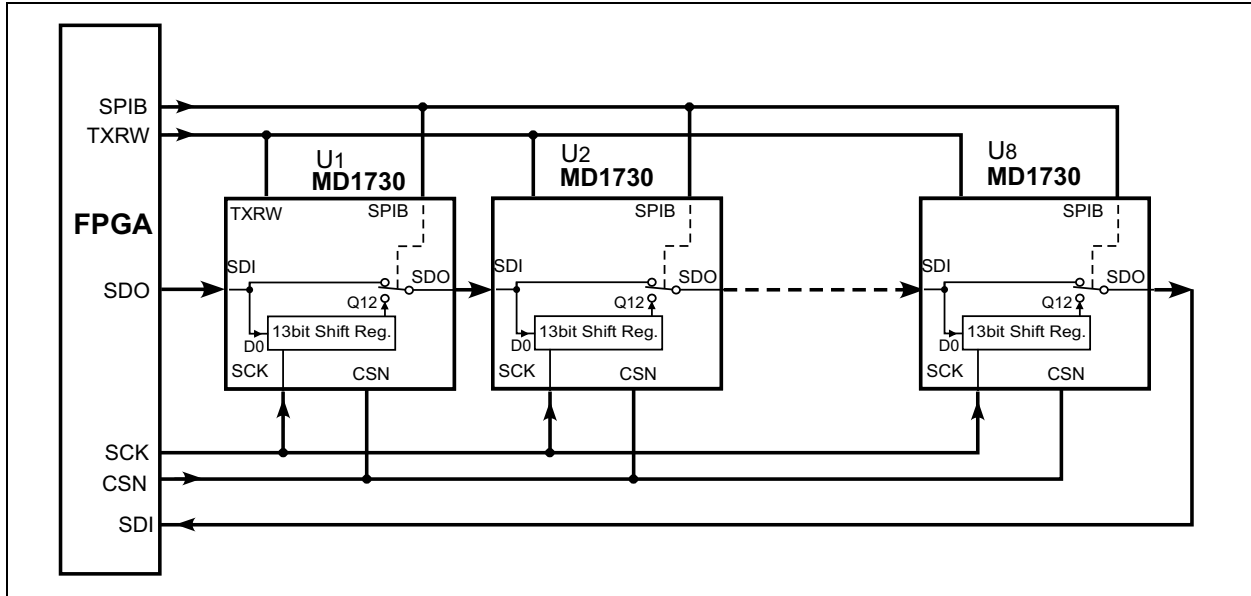


FIGURE 4-3: Multiple MD1730 Devices SPI Daisy Chain Connections.

4.5 CW0~7 Output Timing

The CW output waveform transmission timing is crucial to an ultrasound imaging system. Any small timing variations on the output can degrade the phase noise performance. The MD1730's internal circuitry is designed to ensure ultra-low phase noise. Figure 4-4 shows an example of the output waveform timing diagram. The chip is enabled by taking the EN pin high. Then using the SPI, channel-0's and channel-1's phase delay registers (PHD0<7:0> and PHD1<7:0>) are programmed with delays of 2 and 3 respectively. The rest of the channels are set to a high impedance state by programming the HIZ<7:0> register with data 11111100b. Furthermore, the frequency divider register (CWFD<7:0>) is set to 4. After completing the SPI operation the transmission starts by asserting

TXRW high. The phase delay counter starts counting down after a two CLK cycle latency. This is illustrated in Figure 4-4 for channel 0 and channel 1. In channel 0's case, the phase delay starts counting down from 2 to 0 after the latency and once the delay reaches 0 on the next rising edge of CLK, the positive output appears on the pin CW0. Based on the value of the CWFD<7:0> register, after 4-CLK cycles the CW0 output toggles to the negative supply rail. Subsequently, after 4-CLK cycles at the negative rail, the output switches back again to the positive supply rail, completing one full CW output wave cycle. This process continues until the TXRW pin deasserts low, which shuts the transmission off and forces the channel into a high impedance state. This same procedure applies to channel 1, which is also depicted in Figure 4-4.

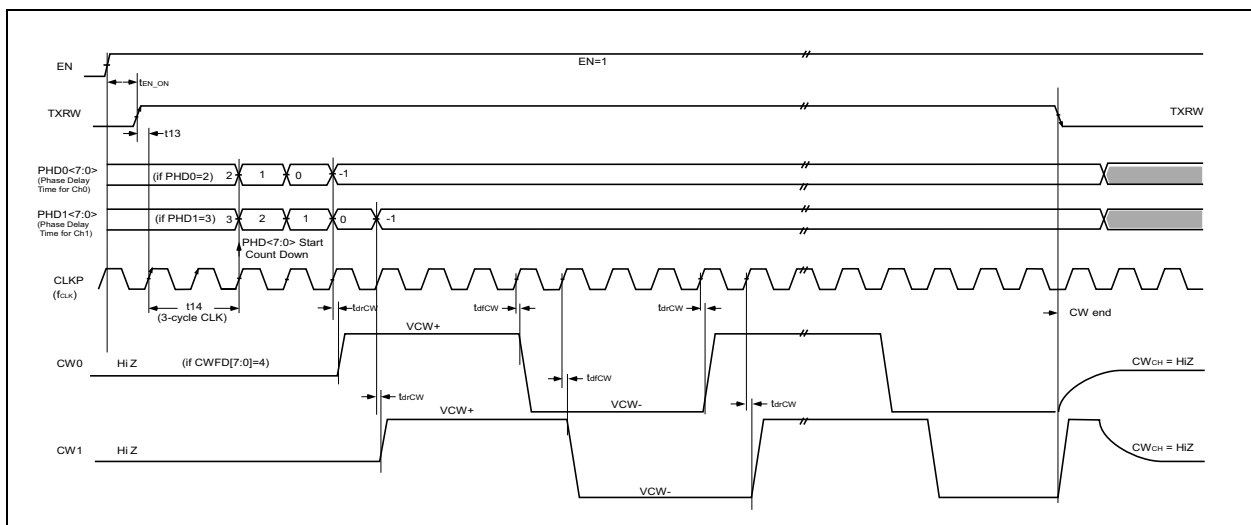


FIGURE 4-4: CW0~7 Output Timing Diagram.

MD1730

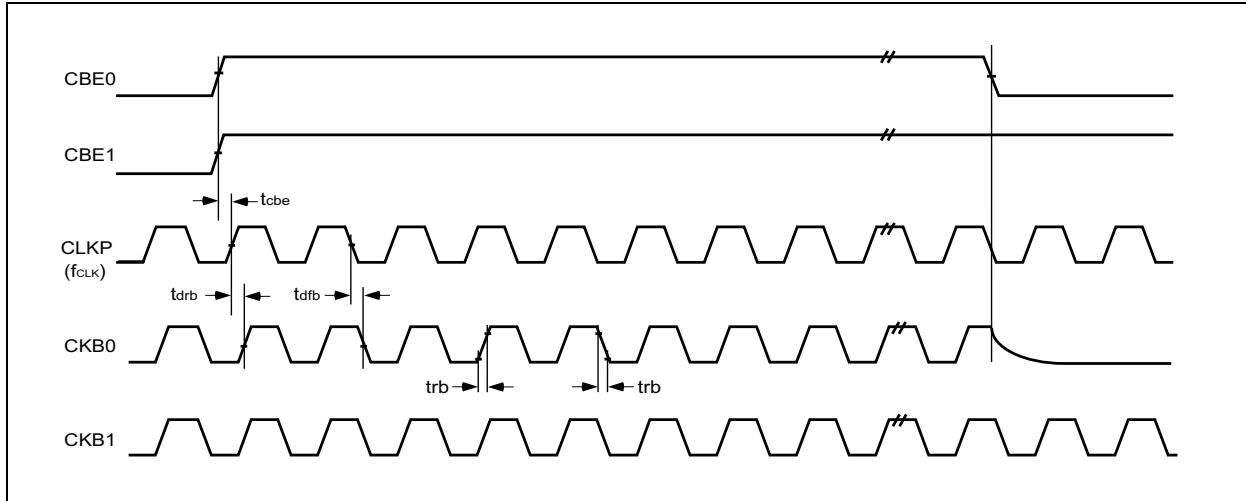


FIGURE 4-5: Clock Buffers CKB0/1 Output Timing Diagram.

4.6 MD1730 Working with Two HV7321

The diagrams shown in [Figure 4-6](#) and [Figure 4-7](#) illustrate the MD1730 driving two HV7321s.

When the HV7321 is operated in the specific mode, CW MODE = 1, along with the MD1730, the following steps should be taken to ensure the combination settings work correctly:

6. Apply all power supply rails to both chips and set HV7321's OEN = REN = PWS = 1 along with MD1730's EN = 1 to enable both chips. Set all other control logic pins to zero.
7. Adjust the VCW+ and VCW- power supplies to the required peak-to-peak voltage levels for CW output transmission. Please note that a higher peak-to-peak transmission voltage will result in the MD1730 dissipating more power. The power dissipation on the MD1730 is proportional to the square of the peak-to-peak voltage.
8. Assert HV7321's MODE pin high.
9. Program the MD1730 with the desired CW frequency divider and delay settings for CW transmission.
10. To place a channel in receive mode, set the corresponding pins SEL, NEG, POS = 011b on the HV7321. To place a channel to CW Transmit mode, set the corresponding pins SEL, NEG, POS to any other combination other than 011b on HV7321. This will put that channel of the HV7321 high voltage Tx output in High Z mode, but turn the channel's CWSW on.
11. Once the system is ready to perform CW Doppler measurement, assert TXRW high to start the CW transmission on the selected channels.

In the case user wants a channel not in High Z or CW Transmit mode, then similarly, to set the channel of HV7321 to High Z and also set the MD1730's corresponding bit in the HIZ register to 1.

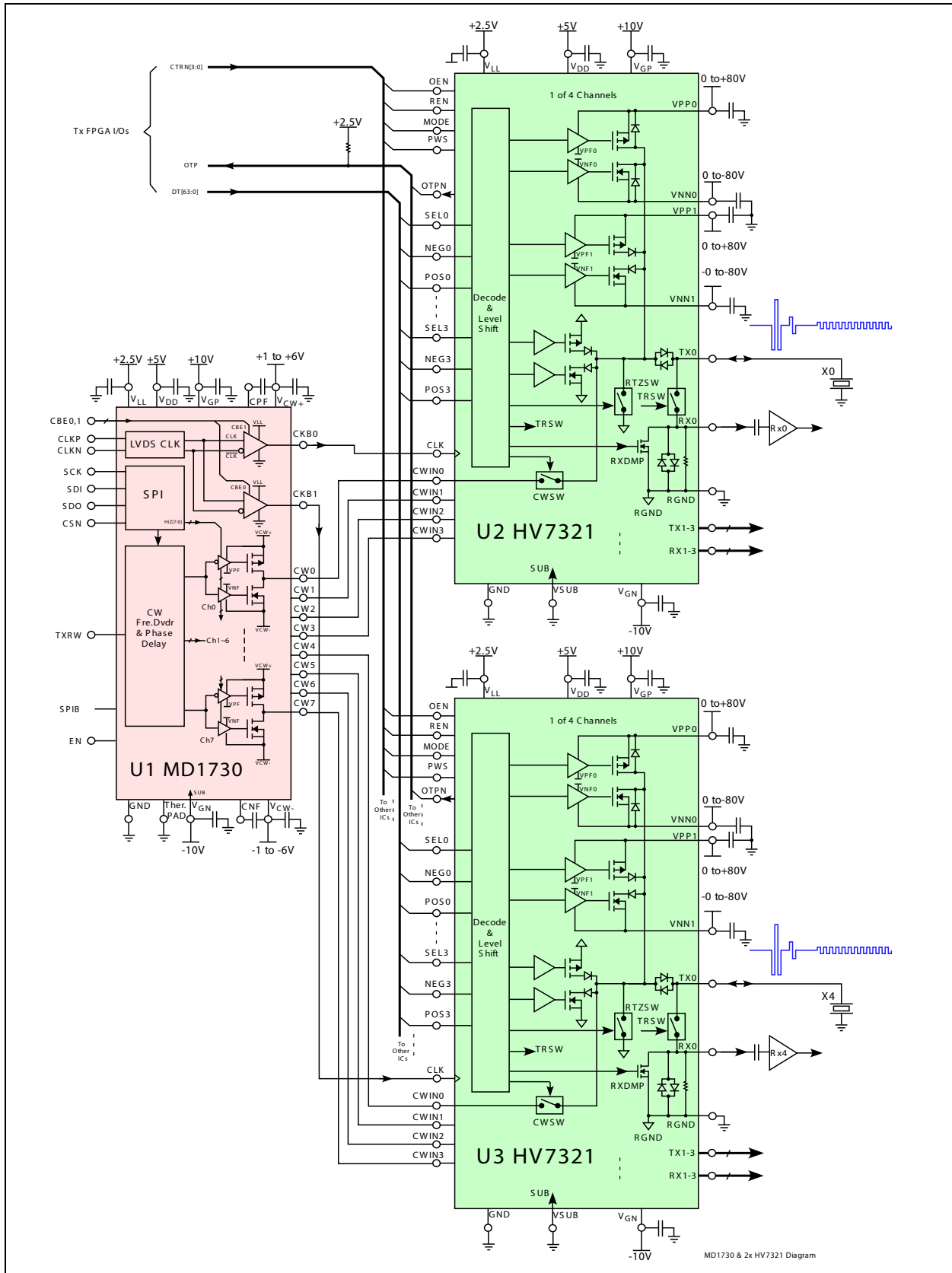


FIGURE 4-6: MD1730 Works with Two HV7321 4-Channel ±80V 2.6A 5-Level Ultrasound Pulsers.

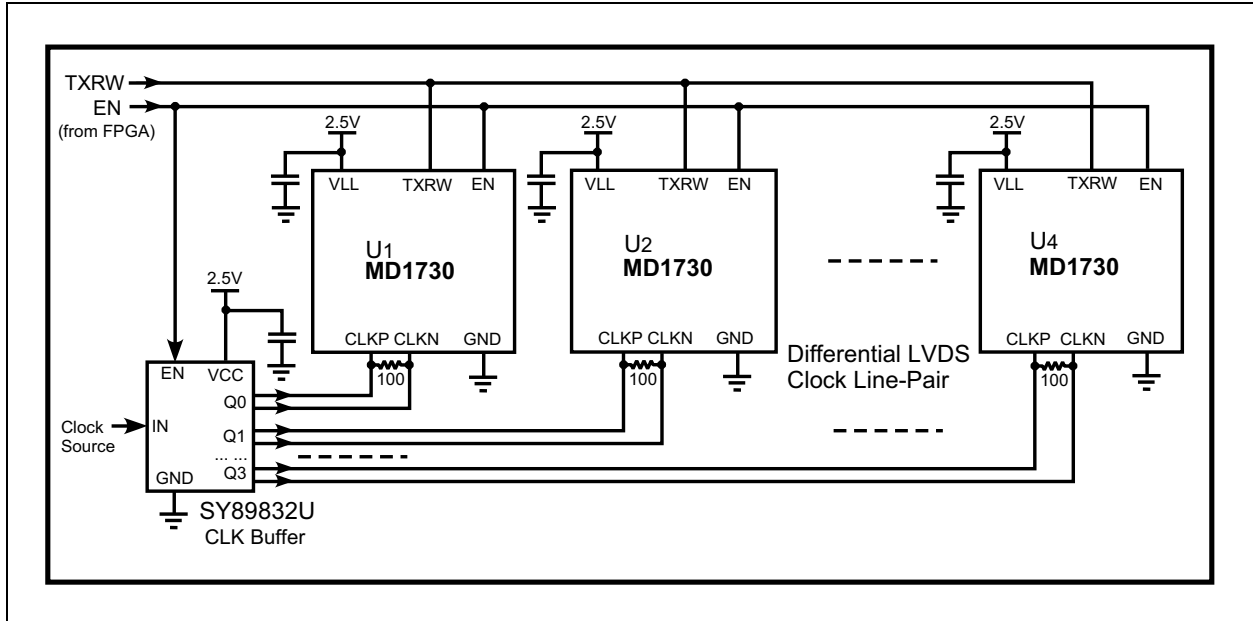


FIGURE 4-8: LVDS Differential Transmission Clock.

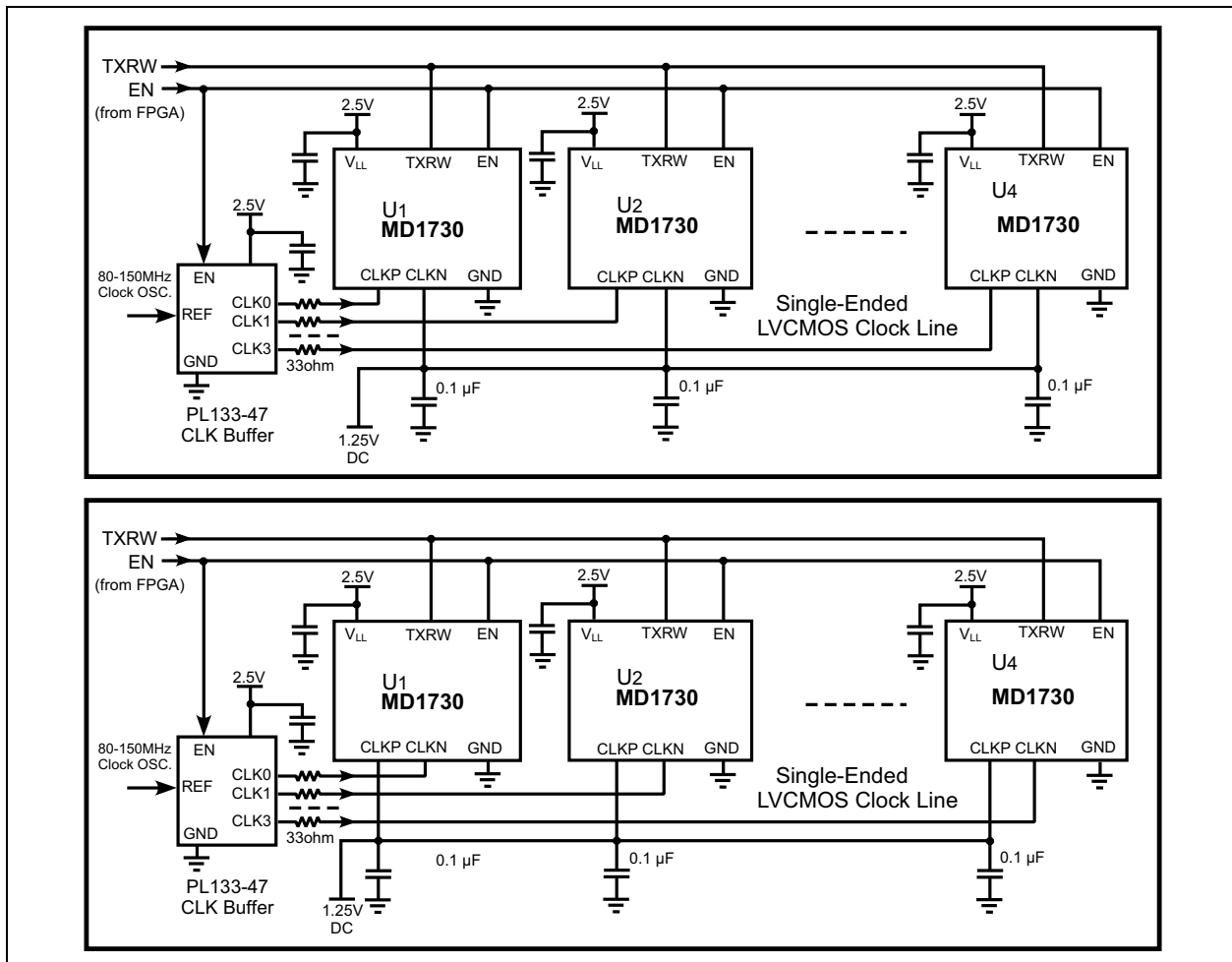


FIGURE 4-9: LVCMOS Single-Ended Transmission Clock.

MD1730

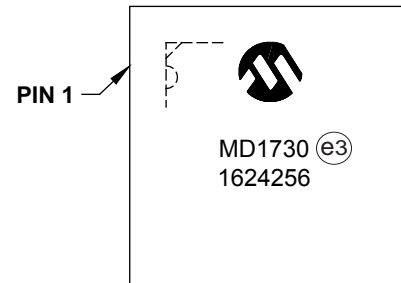
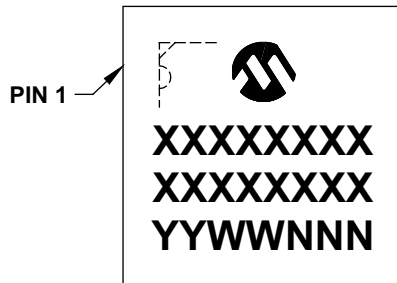
NOTES:

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

36-Lead VQFN (6x6x0.9 mm)

Example

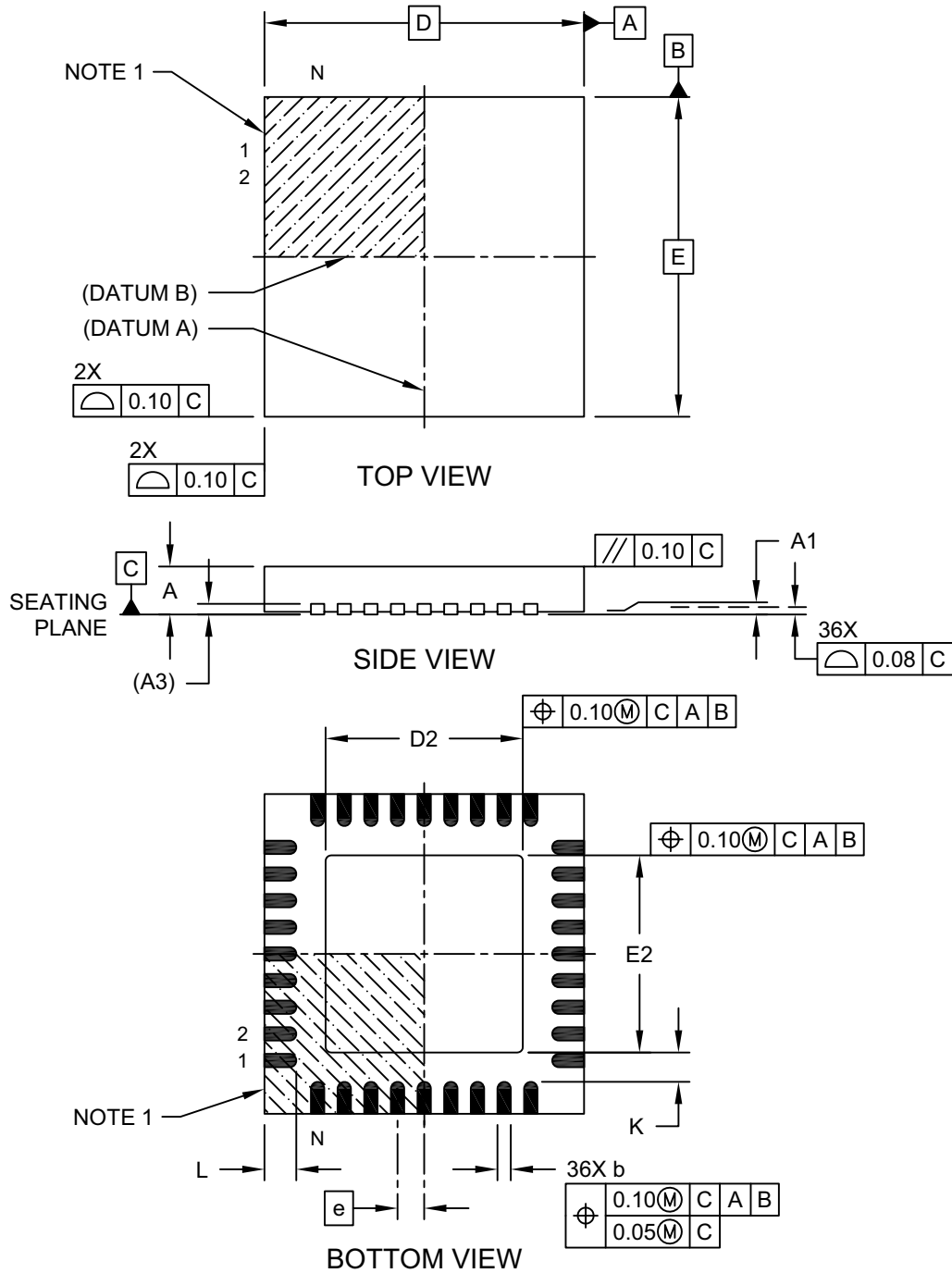


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

MD1730

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

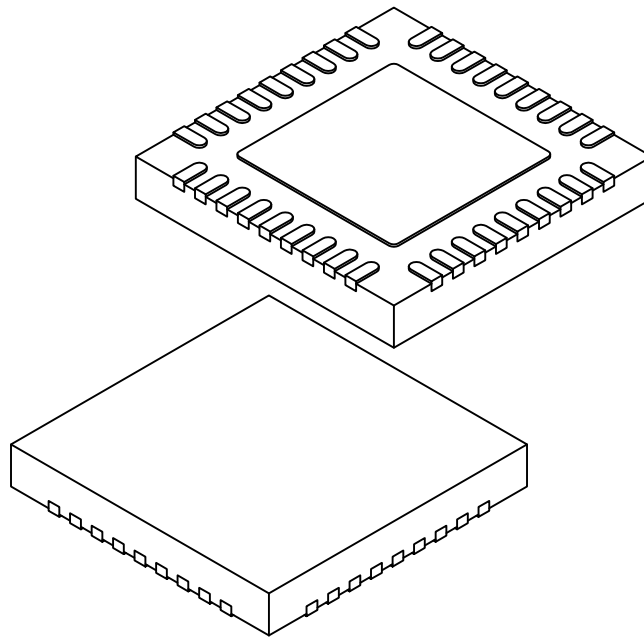
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Terminals	N		36		
Pitch	e		0.50 BSC		
Overall Height	A	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3		0.20 REF		
Overall Width	E		6.00 BSC		
Exposed Pad Width	E2	3.60	3.70	3.80	
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	3.60	3.70	3.80	
Terminal Width	b	0.18	0.25	0.30	
Terminal Length	L	0.50	0.60	0.75	
Terminal-to-Exposed-Pad	K	0.45	0.55	-	

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

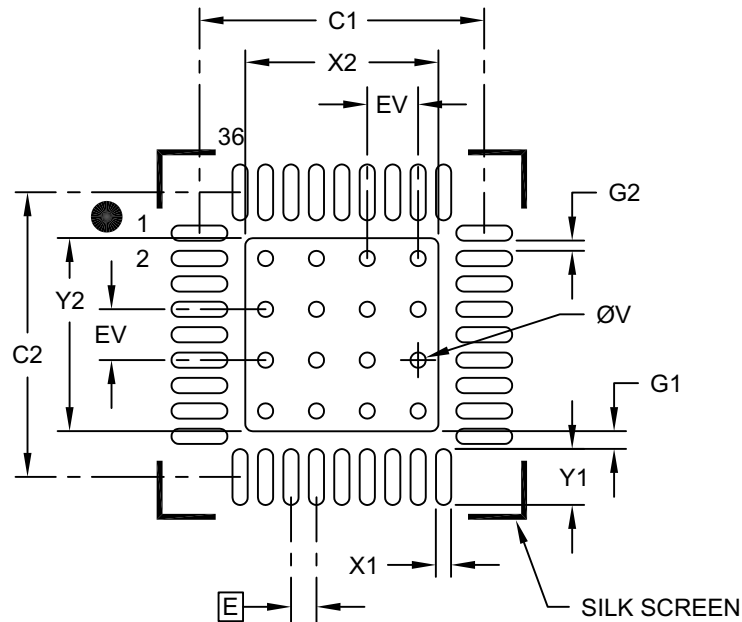
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-272B-M2 Sheet 2 of 2

MD1730

36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x0.9 mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.60	
Contact Pad Spacing	C2		5.60	
Contact Pad Width (X36)	X1			0.30
Contact Pad Length (X36)	Y1			1.10
Contact Pad to Center Pad (X36)	G1	0.35		
Space Between Contact Pads (X32)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2272B-M2

APPENDIX A: REVISION HISTORY

Revision A (September 2016)

- The original release of this document.

MD1730

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip sales office.

<u>PART NO.</u>	<u>[X]⁽¹⁾</u>	-	<u>X</u>	<u>/XX</u>
Device	Tape and Reel Option		Temperature Range	Package
Device:	MD1730:		Programmable High-Voltage, Ultrasound-Transmit Beamformer	
	MD1730T:		Programmable High-Voltage, Ultrasound-Transmit Beamformer (Tape and Reel)	
Temperature Range:	I	=	-40°C to +85°C (Industrial)	
Package:	M2	=	Very Thin Plastic Quad Flat Pack, No-Lead Package – 6x6x1.0 mm Body, 36-Lead (VQFN)	

Examples:

a) MD1730-I/M2: Programmable High-Voltage Ultrasound-Transmit Beamformer, 36LD 6x6 mm VQFN package

b) MD1730T-I/M2: Tape and Reel, Programmable High-Voltage Ultrasound-Transmit Beamformer, 36LD 6x6 mm VQFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

MD1730

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoC® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Klear, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQL, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-0925-0



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199

Tel: 480-792-7200

Fax: 480-792-7277

Technical Support:

[http://www.microchip.com/
support](http://www.microchip.com/support)

Web Address:

www.microchip.com

Atlanta

Duluth, GA

Tel: 678-957-9614

Fax: 678-957-1455

Austin, TX

Tel: 512-257-3370

Boston

Westborough, MA

Tel: 774-760-0087

Fax: 774-760-0088

Chicago

Itasca, IL

Tel: 630-285-0071

Fax: 630-285-0075

Cleveland

Independence, OH

Tel: 216-447-0464

Fax: 216-447-0643

Dallas

Addison, TX

Tel: 972-818-7423

Fax: 972-818-2924

Detroit

Novi, MI

Tel: 248-848-4000

Houston, TX

Tel: 281-894-5983

Indianapolis

Noblesville, IN

Tel: 317-773-8323

Fax: 317-773-5453

Los Angeles

Mission Viejo, CA

Tel: 949-462-9523

Fax: 949-462-9608

New York, NY

Tel: 631-435-6000

San Jose, CA

Tel: 408-735-9110

Canada - Toronto

Tel: 905-695-1980

Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office

Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong

Tel: 852-2943-5100

Fax: 852-2401-3431

Australia - Sydney

Tel: 61-2-9868-6733

Fax: 61-2-9868-6755

China - Beijing

Tel: 86-10-8569-7000

Fax: 86-10-8528-2104

China - Chengdu

Tel: 86-28-8665-5511

Fax: 86-28-8665-7889

China - Chongqing

Tel: 86-23-8980-9588

Fax: 86-23-8980-9500

China - Dongguan

Tel: 86-769-8702-9880

China - Guangzhou

Tel: 86-20-8755-8029

China - Hangzhou

Tel: 86-571-8792-8115

Fax: 86-571-8792-8116

China - Hong Kong SAR

Tel: 852-2943-5100

Fax: 852-2401-3431

China - Nanjing

Tel: 86-25-8473-2460

Fax: 86-25-8473-2470

China - Qingdao

Tel: 86-532-8502-7355

Fax: 86-532-8502-7205

China - Shanghai

Tel: 86-21-5407-5533

Fax: 86-21-5407-5066

China - Shenyang

Tel: 86-24-2334-2829

Fax: 86-24-2334-2393

China - Shenzhen

Tel: 86-755-8864-2200

Fax: 86-755-8203-1760

China - Wuhan

Tel: 86-27-5980-5300

Fax: 86-27-5980-5118

China - Xian

Tel: 86-29-8833-7252

Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen

Tel: 86-592-2388138

Fax: 86-592-2388130

China - Zhuhai

Tel: 86-756-3210040

Fax: 86-756-3210049

India - Bangalore

Tel: 91-80-3090-4444

Fax: 91-80-3090-4123

India - New Delhi

Tel: 91-11-4160-8631

Fax: 91-11-4160-8632

India - Pune

Tel: 91-20-3019-1500

Japan - Osaka

Tel: 81-6-6152-7160

Fax: 81-6-6152-9310

Japan - Tokyo

Tel: 81-3-6880-3770

Fax: 81-3-6880-3771

Korea - Daegu

Tel: 82-53-744-4301

Fax: 82-53-744-4302

Korea - Seoul

Tel: 82-2-554-7200

Fax: 82-2-558-5932 or

82-2-558-5934

Malaysia - Kuala Lumpur

Tel: 60-3-6201-9857

Fax: 60-3-6201-9859

Malaysia - Penang

Tel: 60-4-227-8870

Fax: 60-4-227-4068

Philippines - Manila

Tel: 63-2-634-9065

Fax: 63-2-634-9069

Singapore

Tel: 65-6334-8870

Fax: 65-6334-8850

Taiwan - Hsin Chu

Tel: 886-3-5778-366

Fax: 886-3-5770-955

Taiwan - Kaohsiung

Tel: 886-7-213-7828

Taiwan - Taipei

Tel: 886-2-2508-8600

Fax: 886-2-2508-0102

Thailand - Bangkok

Tel: 66-2-694-1351

Fax: 66-2-694-1350

EUROPE

Austria - Wels

Tel: 43-7242-2244-39

Fax: 43-7242-2244-393

Denmark - Copenhagen

Tel: 45-4450-2828

Fax: 45-4485-2829

France - Paris

Tel: 33-1-69-53-63-20

Fax: 33-1-69-30-90-79

Germany - Dusseldorf

Tel: 49-2129-3766400

Germany - Karlsruhe

Tel: 49-721-625370

Germany - Munich

Tel: 49-89-627-144-0

Fax: 49-89-627-144-44

Italy - Milan

Tel: 39-0331-742611

Fax: 39-0331-466781

Italy - Venice

Tel: 39-049-7625286

Netherlands - Drunen

Tel: 31-416-690399

Fax: 31-416-690340

Poland - Warsaw

Tel: 48-22-3325737

Spain - Madrid

Tel: 34-91-708-08-90

Fax: 34-91-708-08-91

Sweden - Stockholm

Tel: 46-8-5090-4654

UK - Wokingham

Tel: 44-118-921-5800

Fax: 44-118-921-5820

06/23/16