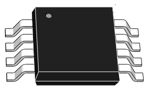
TSZ182

Very high accuracy (25 µV) high bandwidth (3 MHz) zero drift 5 V dual operational amplifiers

Datasheet - production data

DFN8 2x2



MiniSO8

Features

- Very high accuracy and stability: offset voltage 25 µV max at 25 °C, 35 µV over full temperature range (-40 °C to 125 °C)
- Rail-to-rail input and output
- Low supply voltage: 2.2 - 5.5 V
- Low power consumption: 1 mA max. at 5 V
- Gain bandwidth product: 3 MHz
- Automotive qualification is ongoing (TSZ182IYST)
- Extended temperature range: -40 to 125 °C
- Micropackages: DFN8 2x2 and MiniSO8

Benefits

- Higher accuracy without calibration
- Accuracy virtually unaffected by temperature change

Related products

- See *TSZ121, TSZ122 or TSZ124* for zero drift amplifiers with more power savings (400 kHz for 40 µA)
- See *TSV711* or *TSV731* for continuous-time precision amplifiers

Applications

- High accuracy signal conditioning
- Automotive current measurement and sensor signal conditioning
- Medical instrumentation

Description

The TSZ182 is a dual operational amplifier featuring very low offset voltages with virtually zero drift versus temperature changes.

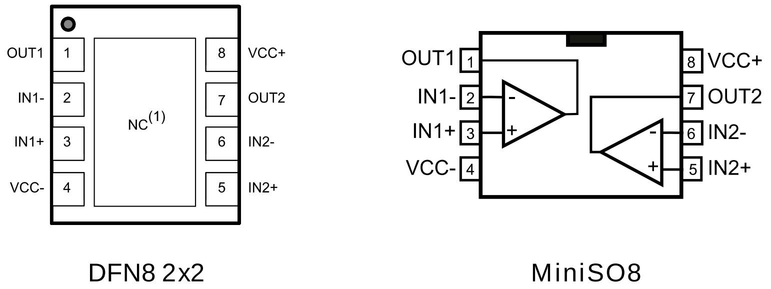
The TSZ182 offers rail-to-rail input and output, excellent speed/power consumption ratio, and 3 MHz gain bandwidth product, while consuming just 1 mA at 5 V. The device also features an ultra-low input bias current.

These features make the TSZ182 ideal for high-accuracy high-bandwidth sensor interfaces.

Contents

1 Package pin connections

Figure 1: Pin connections for each package (top view)



1. The exposed pad of the DFN8 2x2 can be connected to V_{CC-} or left floating.

2 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage (1)		6	V
V_{id}	Differential input voltage (2)		$\pm V_{CC}$	
V_{in}	Input voltage (3)		(V_{CC-}) - 0.2 to (V_{CC+}) + 0.2	
I_{in}	Input current (4)		10	mA
T_{stg}	Storage temperature		-65 to 150	°C
T_j	Maximum junction temperature		150	
R_{thja}	Thermal resistance junction-to-ambient (5) (6)	DFN8 2x2	57	°C/W
		MiniSO8	190	
ESD	HBM: human body model (7)		4	kV
	CDM: charged device model (8)		1.5	
	Latch-up immunity		200	mA

Notes:

(1) All voltage values, except differential voltage, are with respect to network ground terminal.

(2) The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.

(3) V_{CC} - V_{in} must not exceed 6 V, V_{in} must not exceed 6 V.

(4) Input current must be limited by a resistor in series with the inputs.

(5) R_{th} are typical values.

(6) Short-circuits can cause excessive heating and destructive dissipation.

(7) Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

(8) Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.2 to 5.5	V
V_{icm}	Common mode input voltage range	(V_{CC-}) - 0.1 to (V_{CC+}) + 0.1	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 3: Electrical characteristics at V_{CC}+ = 2.2 V with V_{CC}- = 0 V, Vicm = V_{CC}/2, T = 25 °C, and RL = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		3.5	35	µV
		-40 °C < T< 125 °C			45	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)	-40 °C < T< 125 °C			0.1	µV/°C
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		30	200 (2)	pA
		-40 °C < T< 125 °C			300 (2)	
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		60	400 (2)	
		-40 °C < T< 125 °C			600 (2)	
CMR1	Common-mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{ic} = 0 V to V_{CC}, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C	96	115		dB
		-40 °C < T< 125 °C	94			
CMR3	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{ic} = 1.1 V to V_{CC}, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C	102	120		
		-40 °C < T< 125 °C	100			
A_{vd}	Large signal voltage gain, V_{out} = 0.5 V to (V_{cc} - 0.5 V)	T = 25 °C	112	130		
		-40 °C < T< 125 °C	100			
V_{OH}	High-level output voltage, V_{OH} = V_{cc} - V_{out}	T = 25 °C		15	40	mV
		-40 °C < T< 125 °C			70	
V_{OL}	Low-level output voltage	T = 25 °C		10	30	
		-40 °C < T< 125 °C			70	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	4	6		mA
		-40 °C < T< 125 °C	2.5			
	I_{source} (V_{out} = 0 V)	T = 25 °C	3.5	4		
		-40 °C < T< 125 °C	2			
I_{CC}	Supply current (per channel, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C		0.7	1	
		-40 °C < T< 125 °C			1.2	
AC performance						
GBP	Gain bandwidth product	T = 25 °C, R_L = 10 kΩ, C_L = 100 pF	1.6	2.3		MHz
		-40 °C < T< 125 °C, R_L = 10 kΩ, C_L = 100 pF	1.2			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		59		degrees
G_m	Gain margin			16		dB
SR	Slew rate (3)	T = 25 °C	3	4.6		V/µs
		-40 °C < T< 125 °C	2.5			

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_s	Settling time	To 0.1%, V_{in} = 0.8 Vpp		500		ns
e_n	Equivalent input noise voltage density	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		50		
$e_{n\text{-}pp}$	Voltage noise	f = 0.1 to 10 Hz		0.6		µVpp
C_s	Channel separation	f = 1 kHz		120		dB
t_{init}	Initialization time, G = 100 [(4)]	T = 25 °C		60		µs
		-40 °C < T< 125 °C		100		

Notes:

(1)See *Section 5.5: "Input offset voltage drift over temperature"*. Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.

(2)Guaranteed by design.

(3)Slew rate value is calculated as the average between positive and negative slew rates.

(4)Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization

Table 4: Electrical characteristics at V_{CC+} = 3.3 V with V_{CC-} = 0 V, Vicm = V_{CC}/2, T = 25 °C, and RL = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		2	30	µV
		-40 °C < T< 125 °C			40	
$\Delta V_{io}/\Delta T$	Input offset voltage drift [1]	-40 °C < T< 125 °C			0.1	µV/°C
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		30	200 [2]	pA
		-40 °C < T< 125 °C			300 [2]	
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		60	400 [2]	
		-40 °C < T< 125 °C			600 [2]	
CMR1	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{out} = V_{CC}/2, R_L > 1 MΩ	V_{ic} = 0 V to V_{CC}, T = 25 °C	104	120		dB
		V_{ic} = 0 V to V_{CC}, -40 °C < T< 125 °C	102			
CMR2	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{out} = V_{CC}/2, R_L > 1 MΩ	V_{ic} = 0 V to V_{CC} - 1.8 V, T = 25 °C	106	132		
		V_{ic} = 0 V to V_{CC} - 2 V, -40 °C < T< 125 °C	106			
A_{vd}	Large signal voltage gain, V_{out} = 0.5 V to (V_{cc} - 0.5 V)	T = 25 °C	120	138		
		-40 °C < T< 125 °C	110			
V_{OH}	High-level output voltage, V_{OH} = V_{cc} - V_{out}	T = 25 °C		16	40	mV
		-40 °C < T< 125 °C			70	
V_{OL}	Low-level output voltage	T = 25 °C		11	30	
		-40 °C < T< 125 °C			70	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	10	15		mA
		-40 °C < T< 125 °C	7.5			
	I_{source} (V_{out} = 0 V)	T = 25 °C	6	11		
		-40 °C < T< 125 °C	4			
I_{CC}	Supply current (per channel, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C		0.7	1	mA
		-40 °C < T< 125 °C			1.2	
AC performance						
GBP	Gain bandwidth product	T = 25 °C, R_L = 10 kΩ, C_L = 100 pF	2	2.8		MHz
		-40 °C < T< 125 °C, R_L = 10 kΩ, C_L = 100 pF	1.6			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		56		degrees
G_m	Gain margin			15		dB
SR	Slew rate [3]	T = 25 °C	2.6	4.5		V/µs
		-40 °C < T< 125 °C	2.1			
t_s	Settling time	To 0.1%, V_{in} = 1.2 Vpp		550		ns

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage density	f = 1 kHz		40		nV/√Hz
		f = 10 kHz		40		
e_{n-pp}	Voltage noise	f = 0.1 to 10 Hz		0.5		µVpp
C_s	Channel separation	f = 1 kHz		120		dB
t_{init}	Initialization time, G = 100 [4]	T = 25 °C		60		µs
		-40 °C < T< 125 °C		100		

Notes:

(1)See *Section 5.5: "Input offset voltage drift over temperature"*. Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.

(2)Guaranteed by design.

(3)Slew rate value is calculated as the average between positive and negative slew rates.

(4)Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization

Table 5: Electrical characteristics at V_{CC+} = 5 V with V_{CC-} = 0 V, Vicm = $V_{CC}/2$, T = 25 °C, and RL = 10 kΩ connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	25	µV
		-40 °C < T< 125 °C			35	
$\Delta V_{io}/\Delta T$	Input offset voltage drift (1)	-40 °C < T< 125 °C			0.1	µV/°C
I_{ib}	Input bias current (V_{out} = $V_{CC}/2$)	T = 25 °C		30	200 (2)	pA
		-40 °C < T< 125 °C			300 (2)	
I_{io}	Input offset current (V_{out} = $V_{CC}/2$)	T = 25 °C		60	400 (2)	
		-40 °C < T< 125 °C			600 (2)	
CMR1	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{out} = $V_{CC}/2$, R_L > 1 MΩ	V_{ic} = 0 V to V_{CC}, T = 25 °C	108	126		dB
		V_{ic} = 0 V to V_{CC}, -40 °C < T< 125 °C	108			
CMR2	Common mode rejection ratio, 20 log ($\Delta V_{icm}/\Delta V_{io}$), V_{out} = $V_{CC}/2$, R_L > 1 MΩ	V_{ic} = 0 V to V_{CC} - 1.8 V, T = 25 °C	112	136		
		V_{ic} = 0 V to V_{CC} - 2 V, -40 °C < T< 125 °C	112			
SVR1	Supply voltage rejection ratio, 20 log ($\Delta V_{CC}/\Delta V_{io}$), V_{CC} = 2.2 to 5.5 V, V_{ic} = 0 V, R_L > 1 MΩ	T = 25 °C	105	123		
		-40 °C < T< 125 °C	104			
A_{vd}	Large signal voltage gain, V_{out} = 0.5 V to (V_{cc} - 0.5 V)	T = 25 °C	120	144		
		-40 °C < T< 125 °C	110			
EMIRR (3)	EMI rejection ratio, EMIRR = -20 log ($V_{RFpeak}/\Delta V_{io}$)	V_{RF} = 100 mV_p, f = 400 MHz		52		
		V_{RF} = 100 mV_p, f = 900 MHz		52		
		V_{RF} = 100 mV_p, f = 1800 MHz		72		
		V_{RF} = 100 mV_p, f = 2400 MHz		85		
V_{OH}	High-level output voltage, V_{OH} = V_{cc} - V_{out}	T = 25 °C		18	40	mV
		-40 °C < T< 125 °C			70	
V_{OL}	Low-level output voltage	T = 25 °C		13	30	
		-40 °C < T< 125 °C			70	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	20	29		mA
		-40 °C < T< 125 °C	15			
	I_{source} (V_{out} = 0 V)	T = 25 °C	15	25		
		-40 °C < T< 125 °C	10			
I_{CC}	Supply current (per channel, V_{out} = $V_{CC}/2$, R_L > 1 MΩ)	T = 25 °C		0.8	1	
		-40 °C < T< 125 °C			1.2	
AC performance						

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product	T = 25 °C, R_L = 10 kΩ, C_L = 100 pF	2	3		MHz
		-40 °C < T< 125 °C, R_L = 10 kΩ, C_L = 100 pF	1.6			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		56		degrees
G_m	Gain margin			15		dB
SR	Slew rate [(4)]	T = 25 °C	2.9	4.7		V/µs
		-40 °C < T< 125 °C	2.4			
t_s	Settling time	To 0.1 %, V_{in} = 1.5 Vpp		600		ns
		To 0.01 %, V_{in} = 1 Vpp		4		µs
e_n	Equivalent input noise voltage	f = 1 kHz		37		nV/√Hz
		f = 10 kHz		37		
$e_{n\text{-}pp}$	Voltage noise	f = 0.1 to 10 Hz		0.4		µVpp
C_s	Channel separation	f = 100 Hz		135		dB
t_{init}	Initialization time, G = 100 [(5)]	T = 25 °C		60		µs
		-40 °C < T< 125 °C		100		

Notes:

(1)See *Section 5.5: "Input offset voltage drift over temperature"*. Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.

(2)Guaranteed by design

(3)Tested on the MiniSO8 package, RF injection on the IN- pin

(4)Slew rate value is calculated as the average between positive and negative slew rates

(5)Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization

4 Electrical characteristic curves

Figure 2: Supply current vs. supply voltage

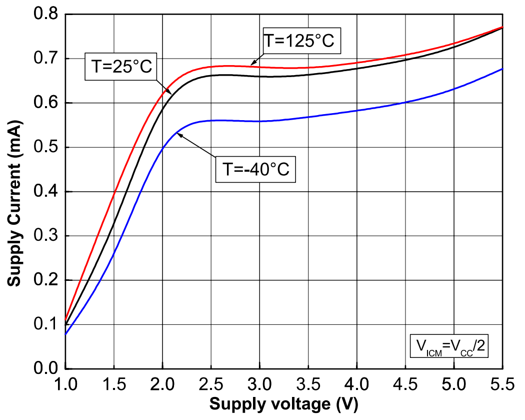


Figure 3: Input offset voltage distribution at Vcc = 5 V

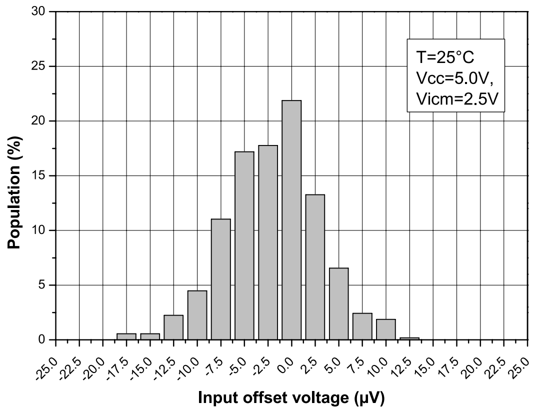


Figure 4: Input offset voltage distribution at Vcc = 3.3 V

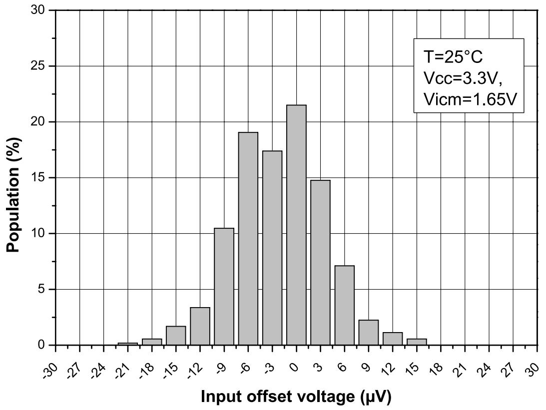


Figure 5: Input offset voltage distribution at Vcc = 2.2 V

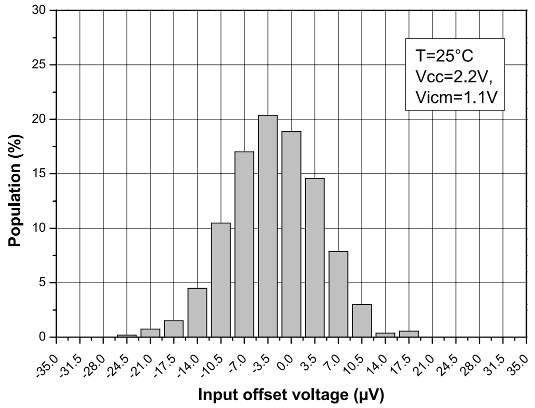


Figure 6: Input offset voltage distribution at Vcc = 5 V, T = 125 °C

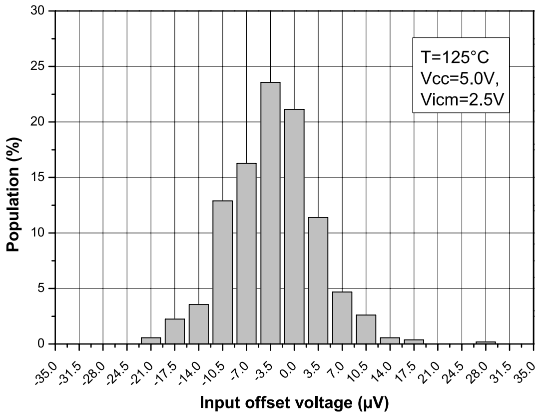


Figure 7: Input offset voltage distribution at Vcc = 5 V, T = -40 °C

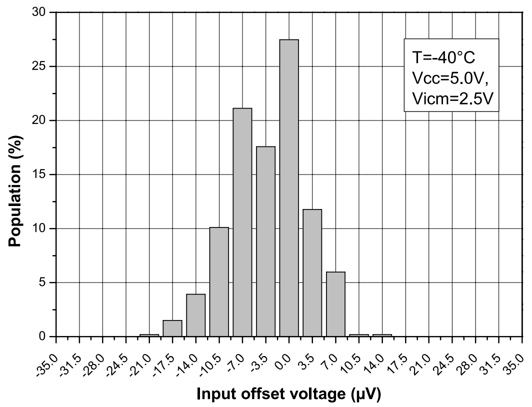


Figure 8: Input offset voltage distribution at V_{CC} = 2.2 V, T = 125 °C

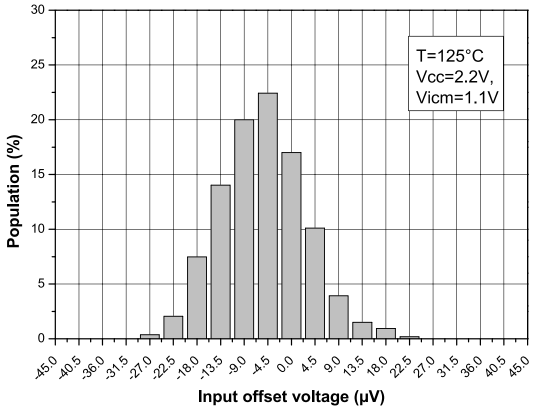


Figure 9: Input offset voltage distribution at V_{CC} = 2.2 V, T = -40 °C

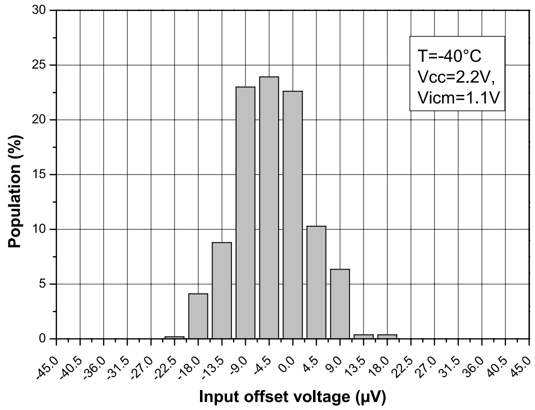


Figure 10: Input offset voltage vs. supply voltage

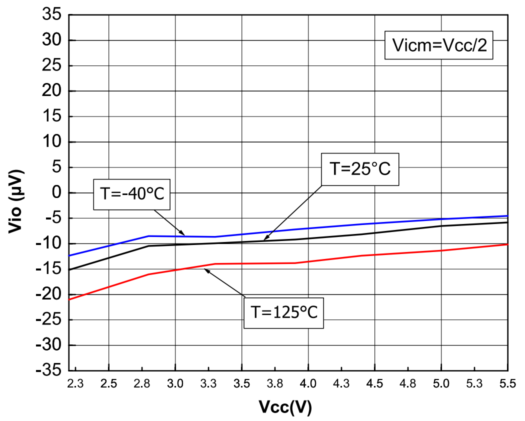


Figure 11: Input offset voltage vs. input common-mode at V_{CC} = 5.5 V

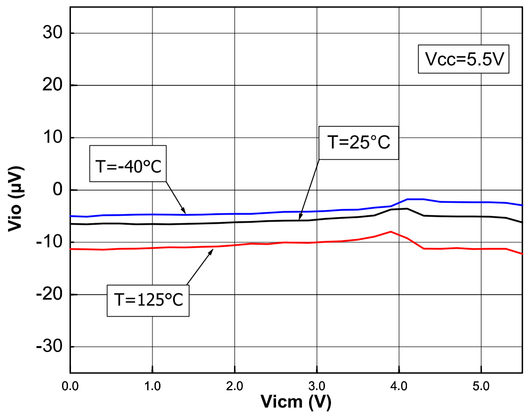


Figure 12: Input offset voltage vs. input common-mode at V_{CC} = 3.3 V

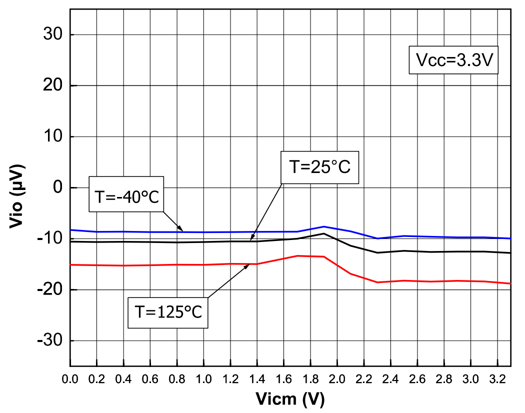


Figure 13: Input offset voltage vs. input common-mode at V_{CC} = 2.2 V

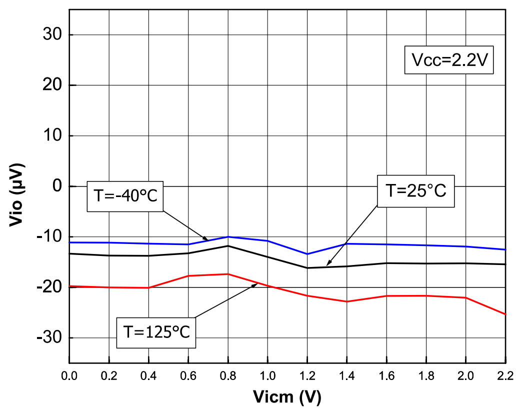


Figure 14: Input offset voltage vs temperature

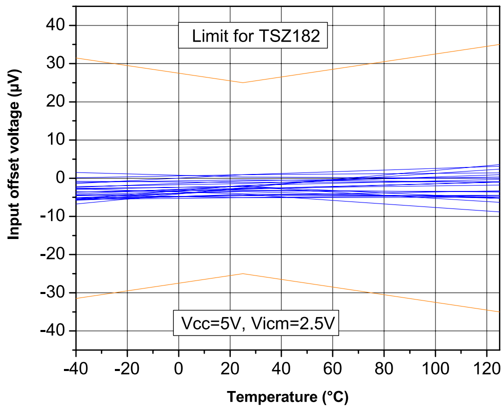


Figure 15: V_{OH} vs supply voltage

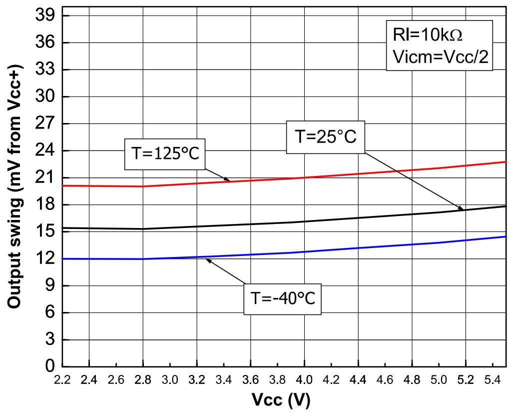


Figure 16: V_{OL} vs supply voltage

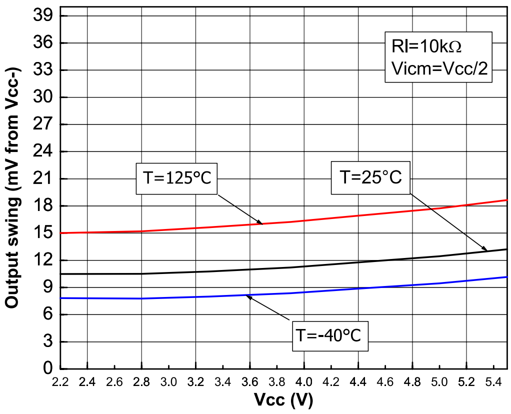


Figure 17: Output current vs output voltage at V_{CC} = 5.5 V

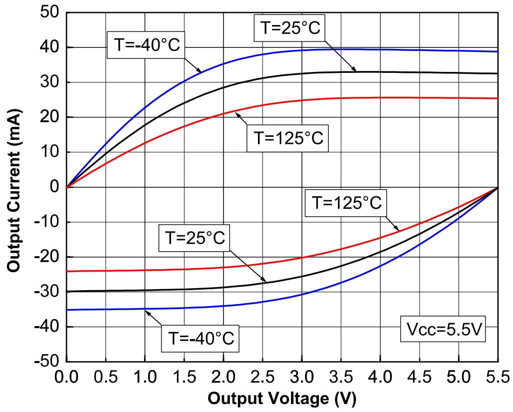


Figure 18: Output current vs output voltage at V_{CC} = 2.2 V

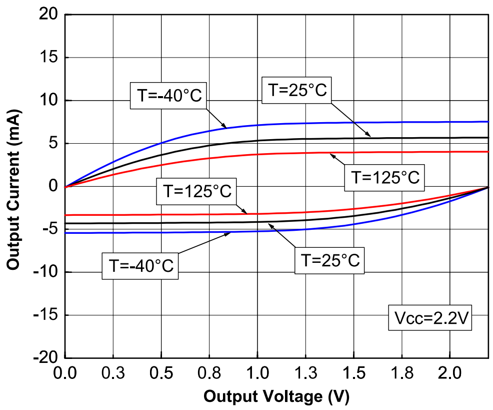


Figure 19: Input bias current vs. common-mode at V_{CC} = 5 V

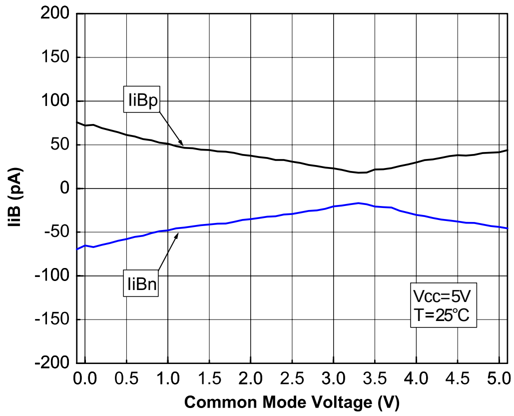


Figure 20: Input bias current vs temperature at V_{CC} = 5 V

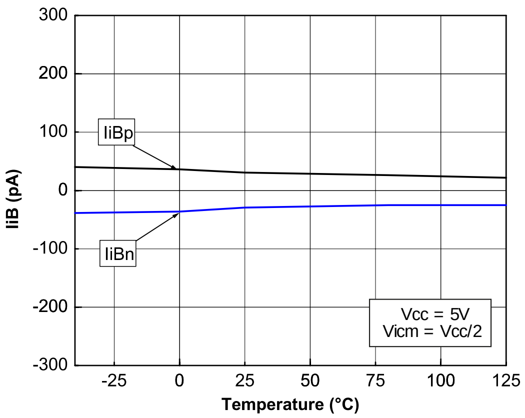


Figure 21: Output rail linearity

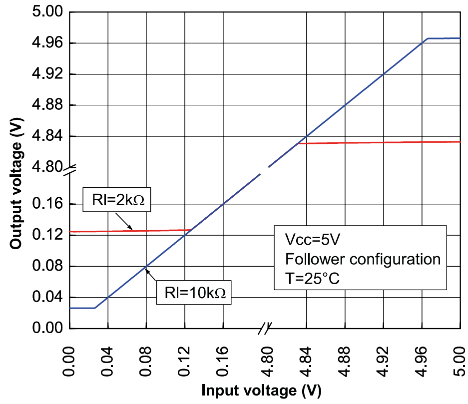


Figure 22: Bode diagram at V_{CC} = 5.5 V

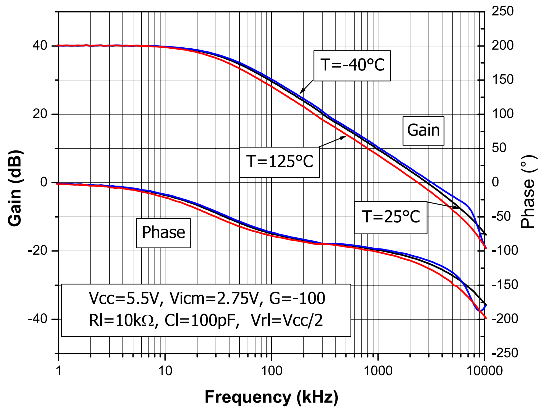


Figure 23: Bode diagram at V_{CC} = 2.2 V

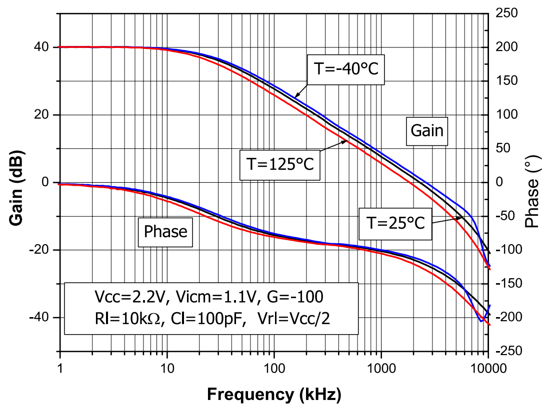


Figure 24: Bode diagram at V_{CC} = 3.3 V

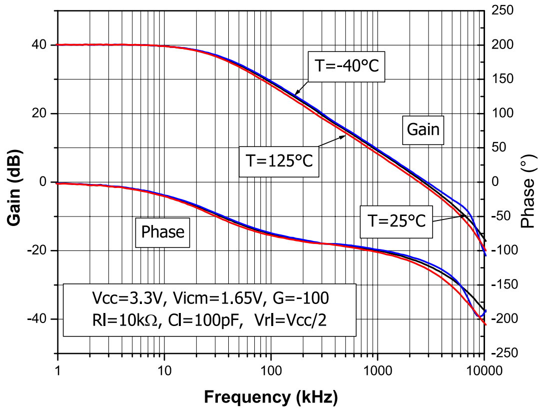


Figure 25: Open loop gain vs frequency

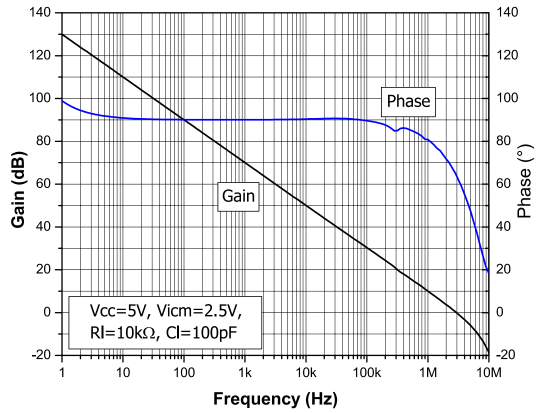


Figure 26: Positive slew rate vs supply voltage

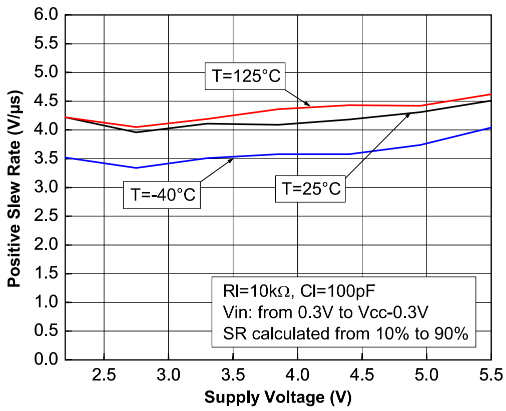


Figure 27: Negative slew rate vs supply voltage

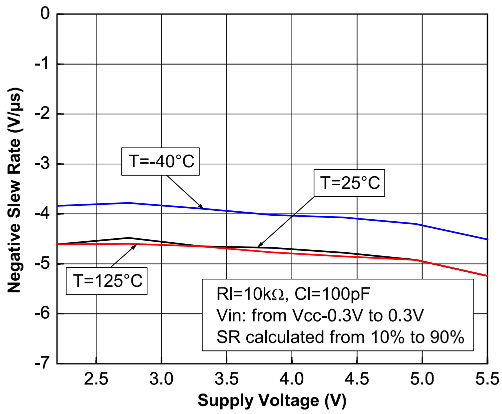


Figure 28: Noise 0.1 - 10 Hz vs time

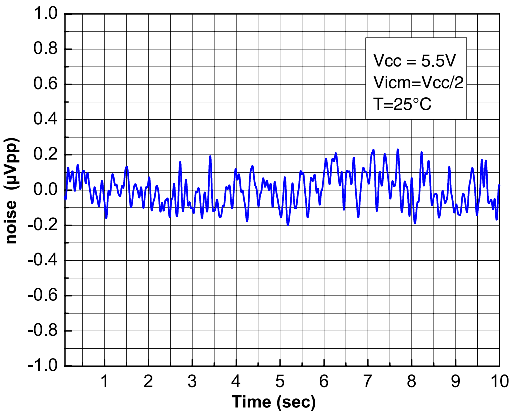


Figure 29: Noise vs frequency

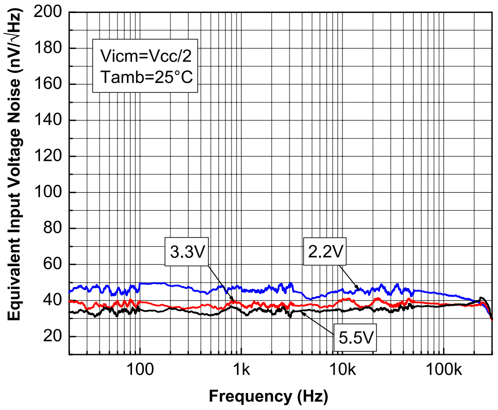


Figure 30: Noise vs frequency and temperature

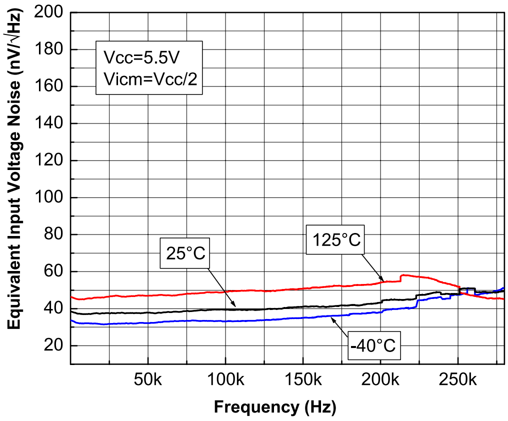


Figure 31: Output overshoot vs load capacitance

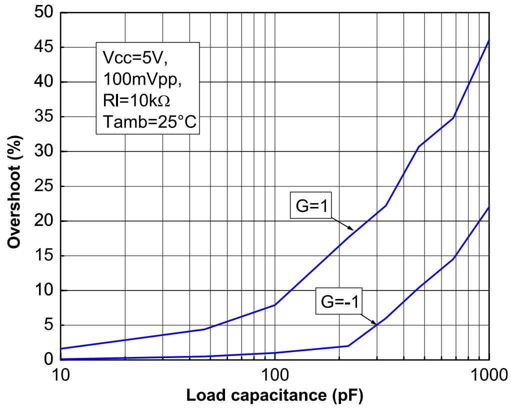


Figure 32: Small signal V_{CC} = 5 V

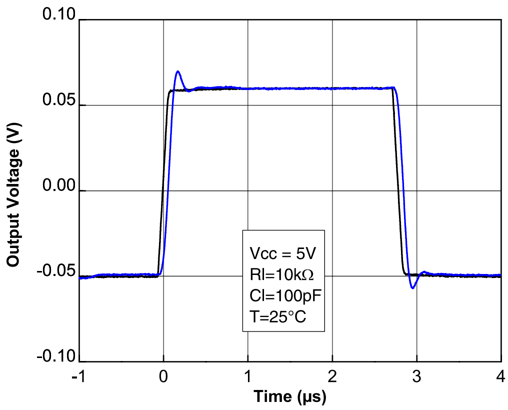


Figure 33: Small signal V_{CC} = 2.2 V

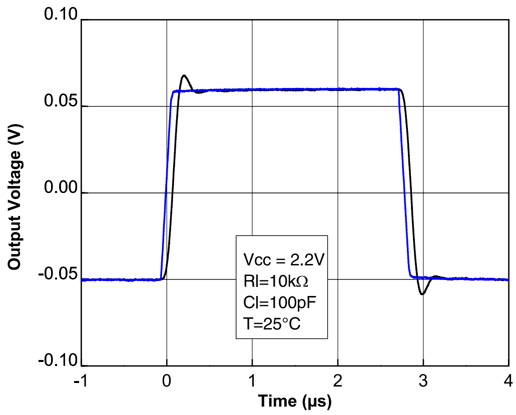


Figure 34: Large signal V_{CC} = 5 V

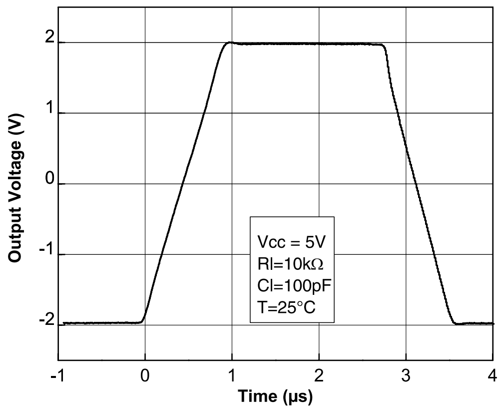


Figure 35: Large signal V_{CC} = 2.2 V

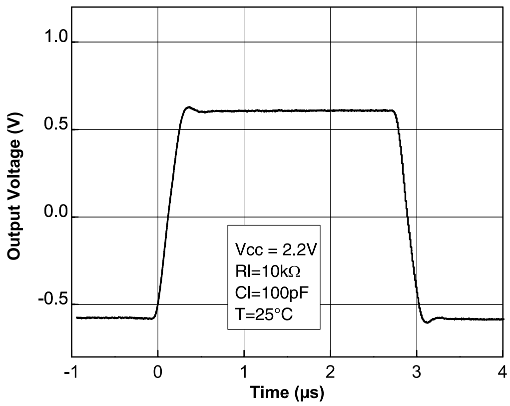


Figure 36: Negative overvoltage recovery V_{CC} = 2.2 V

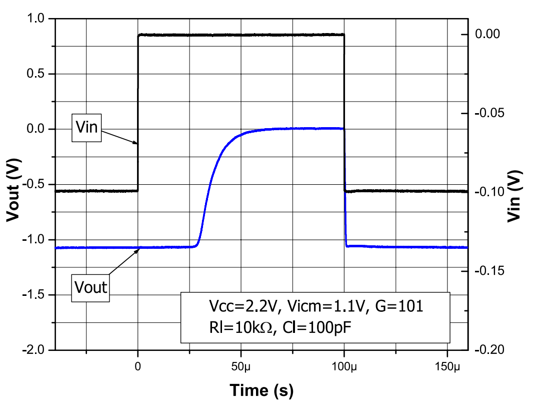


Figure 37: Positive overvoltage recovery V_{CC} = 2.2 V

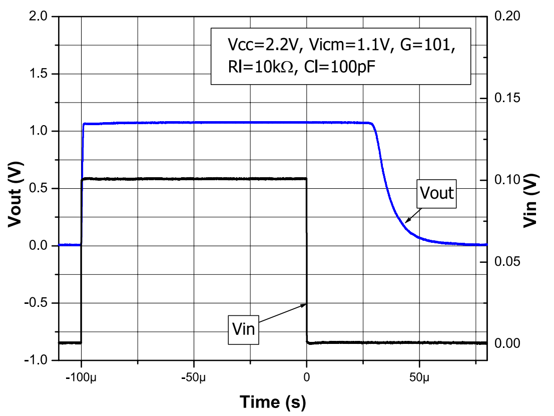


Figure 38: Output impedance vs frequency

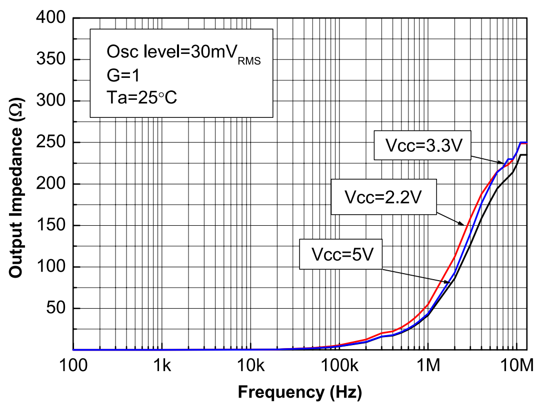


Figure 39: Settling time positive step (-2 V to 0 V)

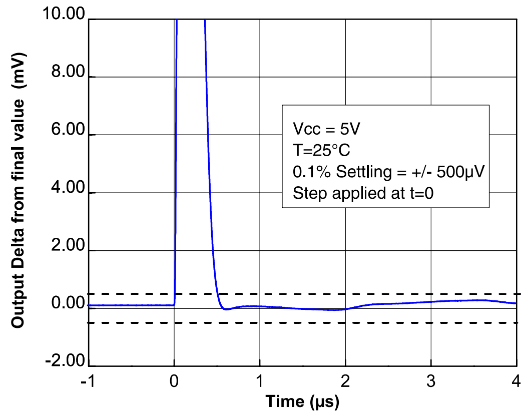


Figure 40: Settling time negative step (2 V to 0 V)

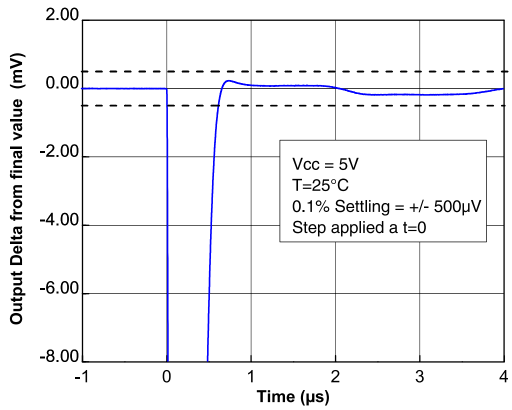


Figure 41: Settling time positive step (-0.8 V to 0 V)

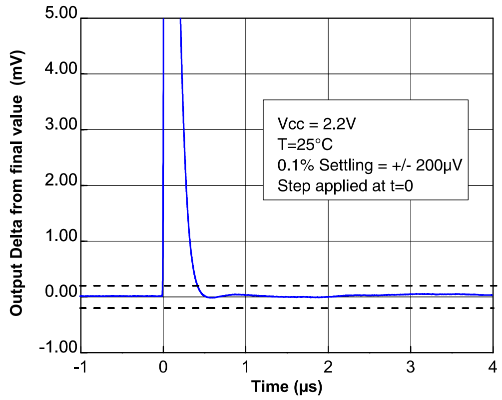


Figure 42: Settling time negative step (0.8 V to 0 V)

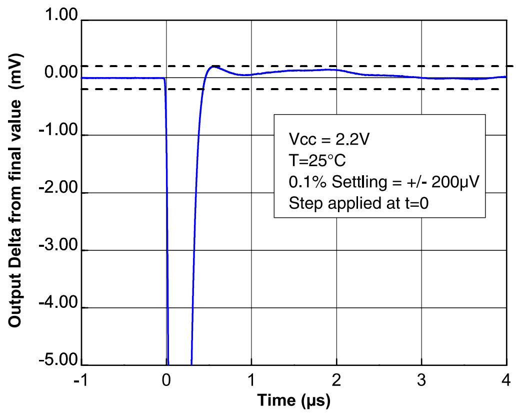


Figure 43: Maximum output voltage vs frequency

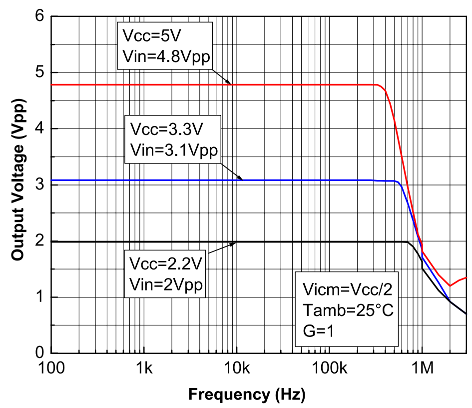


Figure 44: Crosstalk vs frequency

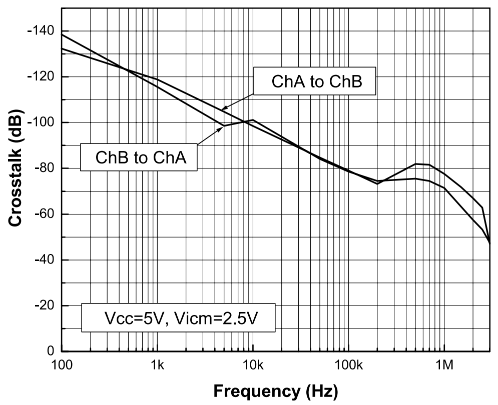
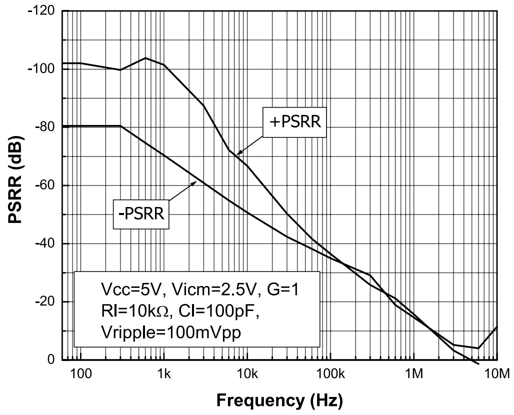


Figure 45: PSRR vs frequency



5 Application information

5.1 Operation theory

The TSZ182 is a high precision CMOS device. It can achieve a low offset drift and no 1/f noise thanks to its chopper architecture. Chopper-stabilized amps constantly correct low-frequency errors across the inputs of the amplifier.

Chopper-stabilized amplifiers can be explained with respect to:

- Time domain
- Frequency domain

5.1.1 Time domain

The basis of the chopper amplifier is realized in two steps. These steps are synchronized thanks to a clock running at 2.4 MHz.

Figure 46: Block diagram in the time domain (step 1)

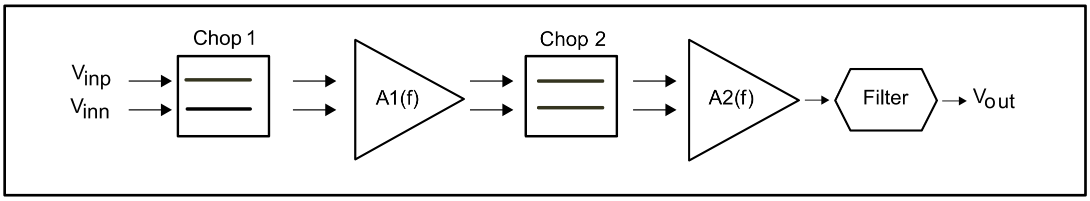


Figure 47: Block diagram in the time domain (step 2)

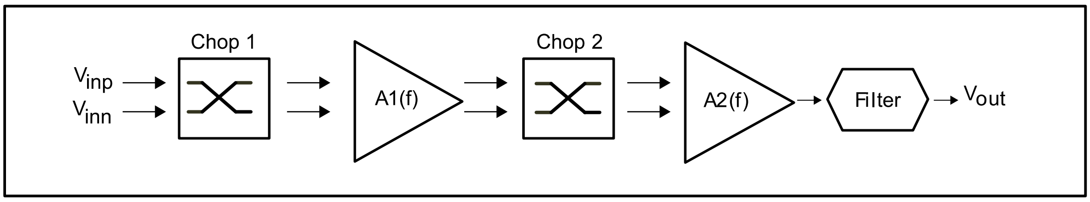


Figure 46: "Block diagram in the time domain (step 1)" shows step 1, the first clock cycle, where V_{io} is amplified in the normal way.

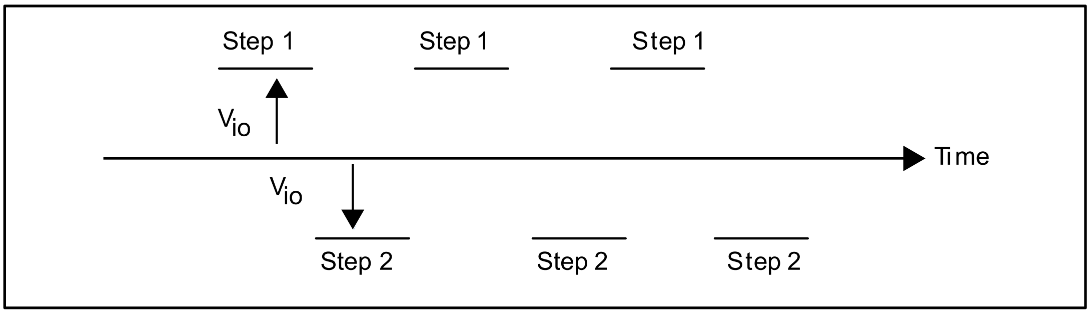
Figure 47: "Block diagram in the time domain (step 2)" shows step 2, the second clock cycle, where Chop1 and Chop2 swap paths. At this time, the V_{io} is amplified in a reverse way as compared to step 1.

At the end of these two steps, the average V_{io} is close to zero.

The A2(f) amplifier has a small impact on the V_{io} because the V_{io} is expressed as the input offset and is consequently divided by A1(f).

In the time domain, the offset part of the output signal before filtering is shown in *Figure 48: "Vio cancellation principle"*.

Figure 48: Vio cancellation principle



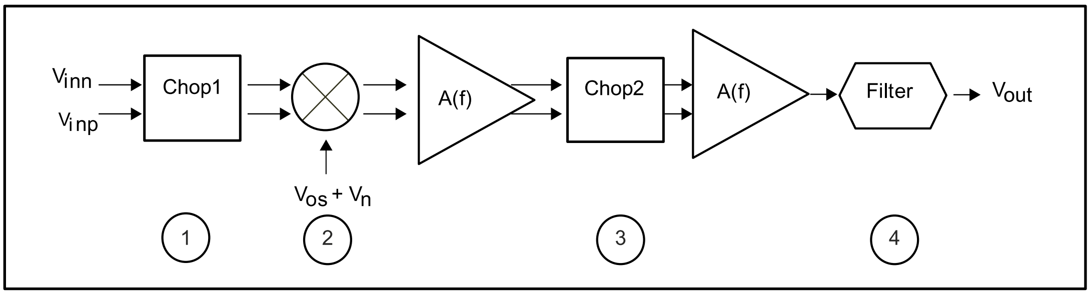
The low pass filter averages the output value resulting in the cancellation of the V_{io} offset.

The 1/f noise can be considered as an offset in low frequency and it is canceled like the V_{io}, thanks to the chopper technique.

5.1.2 Frequency domain

The frequency domain gives a more accurate vision of chopper-stabilized amplifier architecture.

Figure 49: Block diagram in the frequency domain



The modulation technique transposes the signal to a higher frequency where there is no 1/f noise, and demodulate it back after amplification.

1. According to *Figure 49: "Block diagram in the frequency domain"*, the input signal V_{in} is modulated once (Chop1) so all the input signal is transposed to the high frequency domain.
2. The amplifier adds its own error (V_{io} (output offset voltage) + the noise V_n (1/f noise)) to this modulated signal.
3. This signal is then demodulated (Chop2), but since the noise and the offset are modulated only once, they are transposed to the high frequency, leaving the output signal of the amplifier without any offset and low frequency noise. Consequently, the input signal is amplified with a very low offset and 1/f noise.
4. To get rid of the high frequency part of the output signal (which is useless) a low pass filter is implemented.

To further suppress the remaining ripple down to a desired level, another low pass filter may be added externally on the output of the TSZ182.

5.2 Operating voltages

The TSZ182 device can operate from 2.2 to 5.5 V. The parameters are fully specified for 2.2 V, 3.3 V, and 5 V power supplies. However, the parameters are very stable in the full V_{CC} range and several characterization curves show the TSZ182 device characteristics at 2.2 V and 5.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to 125 °C.

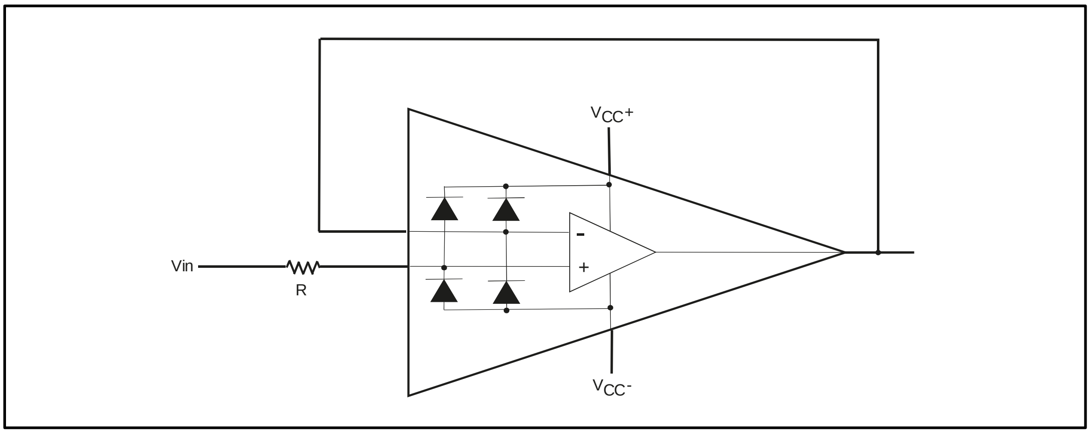
5.3 Input pin voltage ranges

The TSZ182 device has internal ESD diode protection on the inputs. These diodes are connected between the input and each supply rail to protect the input MOSFETs from electrical discharge.

If the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current can flow through them. Without limitation this over current can damage the device.

In this case, it is important to limit the current to 10 mA, by adding resistance on the input pin, as described in *Figure 50: "Input current limitation"*.

Figure 50: Input current limitation



5.4 Rail-to-rail input/output

The TSZ182 has a rail-to-rail input, and the input common mode range is extended from (V_{CC-}) - 0.1 V to (V_{CC+}) + 0.1 V.

The operational amplifier output levels can go close to the rails: to a maximum of 40 mV above and below the rail when connected to a 10 kΩ resistive load to V_{CC}/2.

5.5 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25\,°C)}{T - 25\,°C}\right|$$

Where T = -40 °C and 125 °C.

The TSZ182 datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.6 Capacitive load

Driving large capacitive loads can cause stability problems. Increasing the load capacitance produces gain peaking in the frequency response, with overshoot and ringing in the step response. It is usually considered that with a gain peaking higher than 2.3 dB an op amp might become unstable.

Generally, the unity gain configuration is the worst case for stability and the ability to drive large capacitive loads.

Figure 51: "Stability criteria with a serial resistor at V_{CC} = 5 V", *Figure 52: "Stability criteria with a serial resistor at V_{CC} = 3.3 V"*, and *Figure 53: "Stability criteria with a serial resistor at V_{CC} = 2.2 V"* show the serial resistors that must be added to the output, to make a system stable. *Figure 54: "Test configuration for Riso"* shows the test configuration using an isolation resistor, Riso.

Figure 51: Stability criteria with a serial resistor at V_{CC} = 5 V

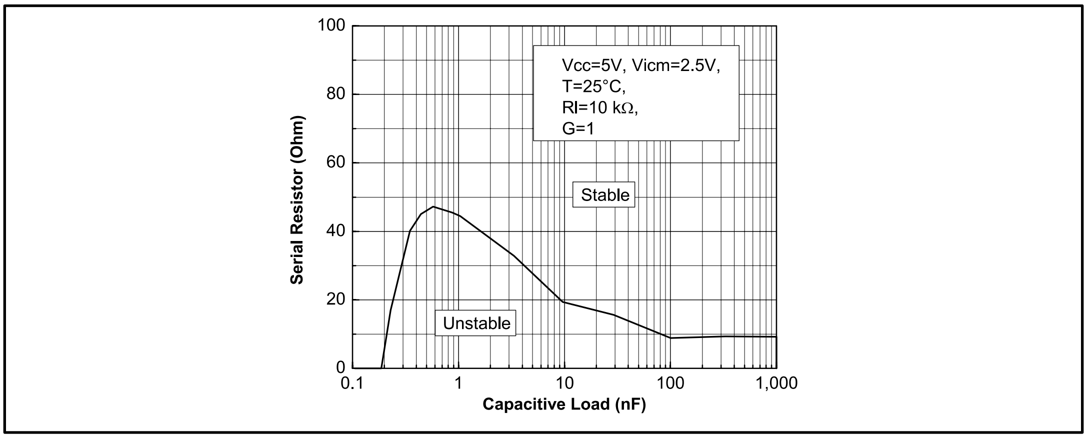


Figure 52: Stability criteria with a serial resistor at V_{CC} = 3.3 V

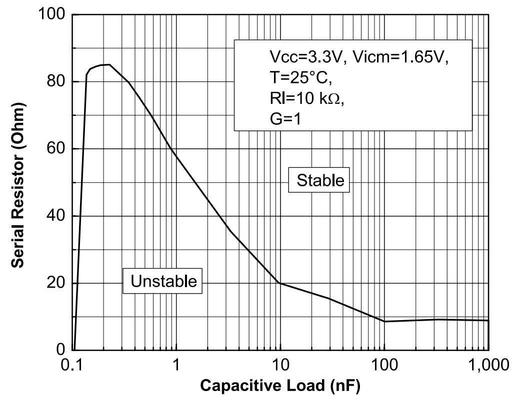


Figure 53: Stability criteria with a serial resistor at V_{CC} = 2.2 V

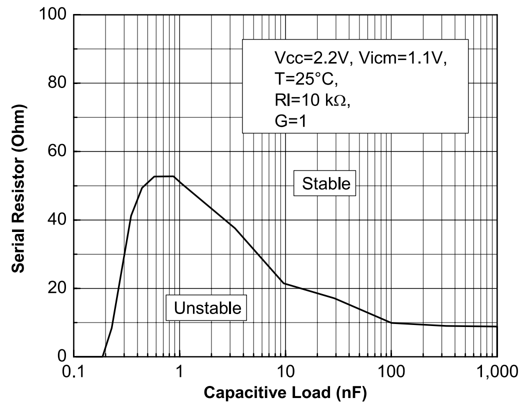
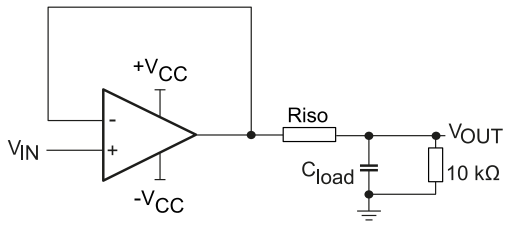


Figure 54: Test configuration for Riso



Note that the resistance Riso is in series with Rload and thus acts as a voltage divider, and reduces the output swing a little. Thanks to the natural good stability of TSZ182, the Riso needed to keep the system stable when the capacitive load exceeds 200pF is lower than 50 Ω (V_{CC} = 5 V), and so the error introduced is generally negligible.

The Riso also modifies the open loop gain of the circuit, and tends to improve the phase margin as described in *Table 6: "Riso impact on stability"*.

Table 6: Riso impact on stability

Capacitive load	100 pF		1 nF		10 nF		100 nF		1 µF	
Riso (Ω)	0	100	47	100	22	47	8	13	10	6
Measured overshoot (%)	20.9	15	23	9	16	8	21	10	12	8
Estimated phase margin (°)	47	53	46	59	52	61	47	58	56	61

5.7 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load and power supply. It is good practice to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

To minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

A ground plane generally helps to reduce EMI, which is why it is generally recommended to use a multilayer PCB and use the ground plane as a shield to protect the internal track. In this case, pay attention to separate the digital from the analog ground and avoid any ground loop.

Place external components as close as possible to the op amp and keep the gain resistances, Rf and Rg, close to the inverting pin to minimize parasitic capacitances.

5.8 Optimized application recommendation

The TSZ182 is based on a chopper architecture. As the device includes internal switching circuitry, it is strongly recommended to place a 0.1 µF capacitor as close as possible to the supply pins.

A good decoupling has several advantages for an application. First, it helps to reduce electromagnetic interference. Due to the modulation of the chopper, the decoupling capacitance also helps to reject the small ripple that may appear on the output.

The TSZ182 has been optimized for use with 10 kΩ in the feedback loop. With this, or a higher value resistance, this device offers the best performance.

5.9 EMI rejection ration (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification.

The TSZ182 has been specially designed to minimize susceptibility to EMIRR and show an extremely good sensitivity. *Figure 55: "EMIRR on IN+ pin"* shows the EMIRR IN+, *Figure 56: "EMIRR on IN- pin"* shows the EMIRR IN- of the TSZ182 measured from 10 MHz up to 2.4 GHz.

Figure 55: EMIRR on IN+ pin

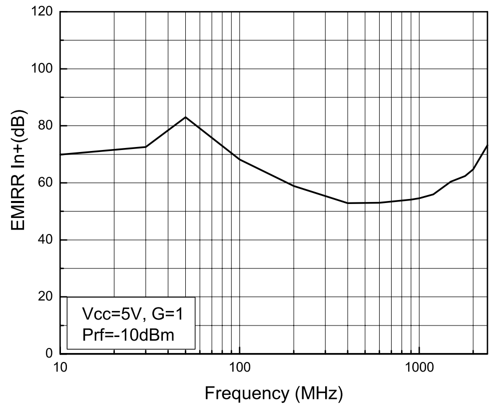
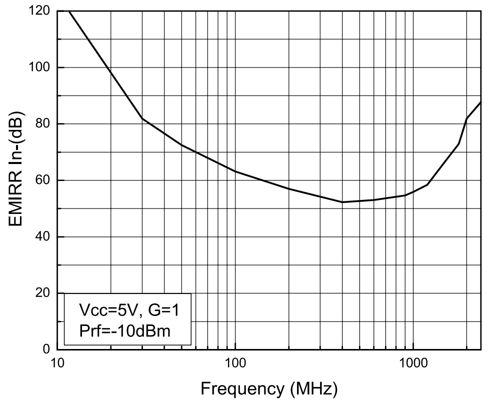


Figure 56: EMIRR on IN- pin



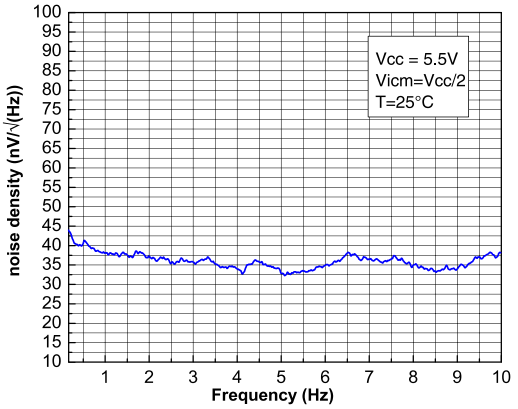
5.10 1/f noise

1/f noise, also known as pink noise or flicker noise, is caused by defects, at the atomic level, in semiconductor devices. The noise is a non-periodic signal and it cannot be calibrated. So for an application requiring precision, it is extremely important to take this noise into account.

1/f noise is a major noise contributor at low frequencies and causes a significant output voltage offset when amplified by the noise gain of the circuit. But, the TSZ182, thanks to its chopper architecture, rejects 1/f noise and thus makes this device an excellent choice for DC high precision applications.

As shown in *Figure 28: "Noise 0.1 - 10 Hz vs time"*, 0.1 Hz to 10 Hz amplifier voltage noise is only 400 nVpp for a V_{CC} = 5 V. *Figure 29: "Noise vs frequency"* and *Figure 30: "Noise vs frequency and temperature"* show the voltage noise density of the amplifier with no 1/f noise on a large bandwith. *Figure 57: "Noise vs frequency between 0.1 and 10 Hz exhibiting no 1/f noise"* below depicts noise vs frequency between 0.1 and 10 Hz exhibiting no 1/f noise.

Figure 57: Noise vs frequency between 0.1 and 10 Hz exhibiting no 1/f noise



5.11 Overload recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state.

The saturation state occurs when the output voltage gets very close to either rail in the application. It can happen due to an excessive input voltage or when the gain setting is too high.

When the output of the TSZ182 enters in saturation state it needs 10 µs to get back to a linear state as shown in *Figure 58: "Negative overvoltage recovery V_{CC} = 5 V"* and *Figure 59: "Positive overvoltage recovery V_{CC} = 5 V"*.

Figure 36: "Negative overvoltage recovery V_{CC} = 2.2 V" and *Figure 37: "Positive overvoltage recovery V_{CC} = 2.2 V"* show the overvoltage recovery for a V_{CC} = 2.2 V.

Figure 58: Negative overvoltage recovery V_{CC} = 5 V

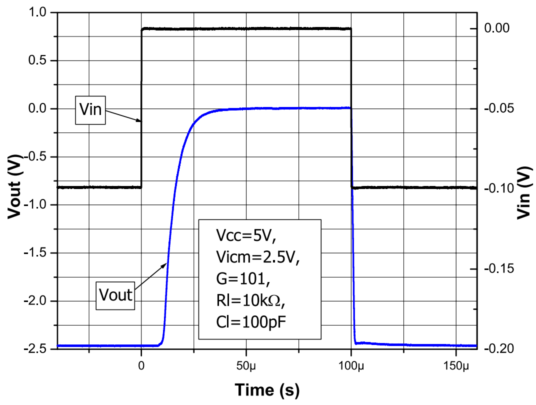
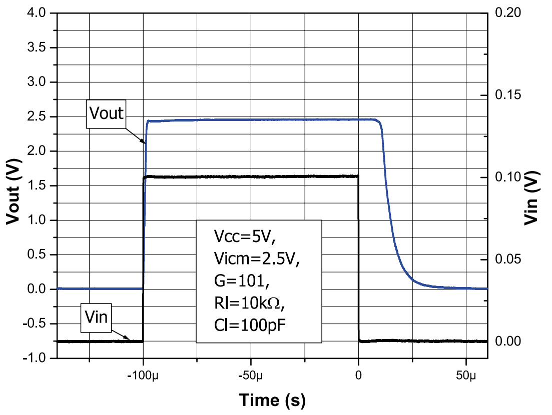


Figure 59: Positive overvoltage recovery V_{CC} = 5 V



5.12 Phase reversal protection

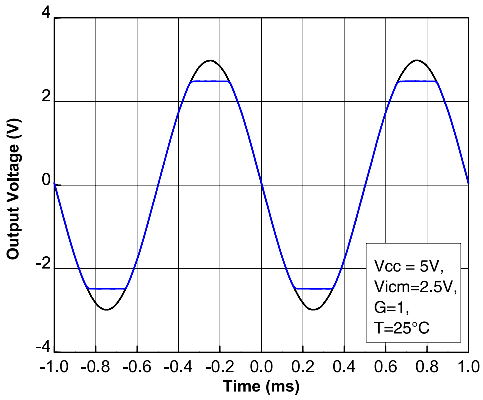
Some op amps can show a phase reversal when the common-mode voltage exceeds the V_{CC} range.

Phase reversal is a specific behavior of an op amp where its output reacts as if the inputs were inverted when at least one input is out of the specified common-mode voltage.

The TSZ182 has been carefully designed to prevent any output phase reversal. The TSZ182 is a rail-to-rail input op amp, therefore, the common-mode range can extend up to the rails. If the input signal goes above the rail it does not cause any inversion of the output signal as shown in *Figure 60: "No phase reversal"*.

If, in the application, the operating common-mode voltage is exceeded please read *Section 5.3: "Input pin voltage ranges"*.

Figure 60: No phase reversal



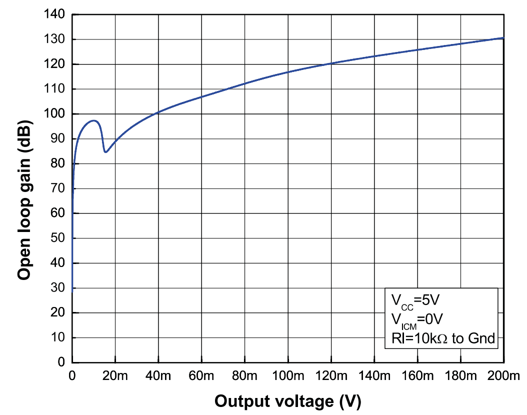
5.13 Open loop gain close to the rail

One of the key parameters of current measurement in low-side applications is precision. Moreover, it is generally interesting to be able to make a measurement when there is no current through the shunt resistance. But, when the output voltage gets close the rail some internal transistors saturate resulting in a loss of open loop gain. Therefore, the output voltage can be as high as several mV while it is expected to be close to 0 V.

The TSZ182 has been designed to keep a high gain even when the op amp output is very close to the rail, to ensure good accuracy at low current.

Figure 61: "Gain vs. output voltage, V_{CC} = 5 V, Rl = 10 kΩ to GND" shows the open loop gain of the TSZ182 vs. output voltage. A single power supply of 5 V and a common-mode voltage of 0 V is used, with a 10 kΩ resistor connected to GND.

Figure 61: Gain vs. output voltage, V_{CC} = 5 V, Rl = 10 kΩ to GND



5.14 Application examples

5.14.1 Measuring gas concentration using the NDIR principle (thermopile)

A thermopile is a serial interconnected array of thermocouples. Based on the Seebeck principle, a thermocouple is able to deliver an output voltage which depends on the temperature difference between a reference junction and an active junction.

An NDIR sensor (non dispersive infrared) is generally composed of an infrared (IR) source, an optical cavity, a dual channel detector, and an internal thermistor. Both channels are made with a thermopile. One channel is considered as a reference and the other is considered as the active channel.

Certain gases absorb IR radiation at a specific wavelength. Each channel has a specific wavelength filter. The active channel has a filter centered on gas absorption while the reference channel has a filter on another wavelength which is still in the IR range.

When a gas enters the optical cavity, the radiation hitting the active channel decreases, whereas it remains the same on the reference channel.

The difference between the reference and active channel gives the concentration of gas present in the optical cavity.

As the thermopile delivers extremely low voltages (hundreds of µV to several mV) the output signal must be amplified with a high gain and a very low offset in order to minimize DC errors.

Moreover, the drift of Vio depending on temperature must be as low as possible not to impact the measurement once the calibration has been made.

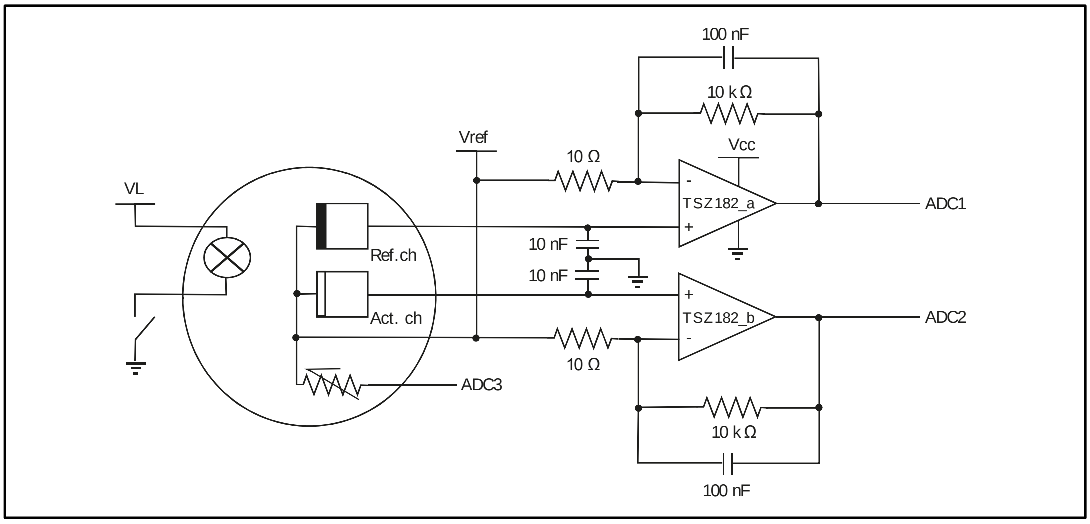
An NDIR sensor generally works at low frequency and the noise of the amplifiers must be as low as possible (0.1-10 Hz $e_{n\text{-}pp}$ = 0.4 µVpp).

Thanks to its chopper architecture, the TSZ182 combines all these specifications, particularly in having a $\Delta V_{io}/\Delta t$ of 0.1 µV/°C, no 1/f noise in low frequency, and a white noise of 37 nV/√Hz.

Figure 62: "Principle schematic" shows an NDIR gas sensing schematic where the active and reference channels are pre-amplified before treatment by an ADC thanks to the TSZ182.

A Vref voltage (in hundreds of mV) can be used to ensure the amplifiers are not saturated when the signal is close to the low rail. A gain of 1000 is used to allow amplification of the signal coming from the NDIR sensor (3 mV).

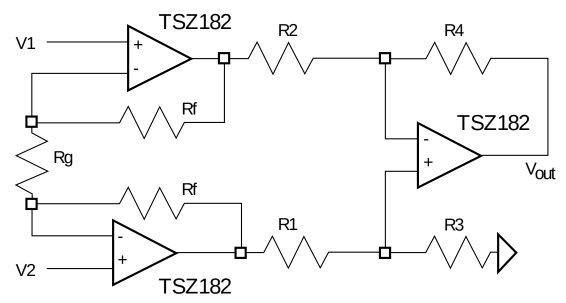
Figure 62: Principle schematic



5.14.2 Precision instrumentation amplifier

The instrumentation amplifier uses three op amps. The circuit, shown in *Figure 63: "Precision instrumentation amplifier schematic"*, exhibits high input impedance, so that the source impedance of the connected sensor has no impact on the amplification.

Figure 63: Precision instrumentation amplifier schematic



The gain is set by tuning the Rg resistor. To have the best performance, it is suggested to have R1 = R2 = R3 = R4. The output is given by *Equation 2*.

Equation 2

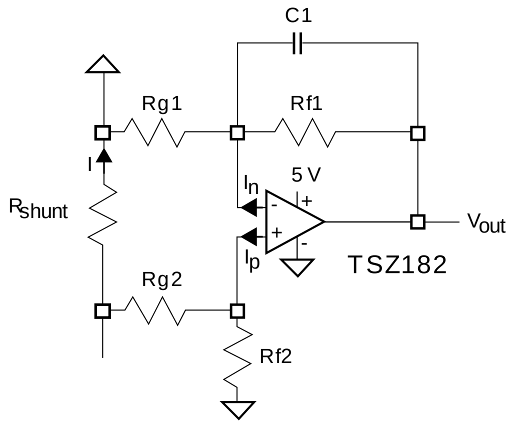
$$V_{out} = (V_2 - V_1)\left[\frac{2R_f}{R_g} + 1\right]$$

The matching of R1, R2 and R3, R4 is important to ensure a good common mode rejection ratio (CMR).

5.14.3 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSZ182 (see *Figure 64: "Low-side current sensing schematic"*).

Figure 64: Low-side current sensing schematic



V_{out} can be expressed as follows:

Equation 3

$$V_{out} = R_{shunt} \times I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right)\left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p\left(\frac{R_{g2} \times R_{f2}}{R_{g2} + R_{f2}}\right) \times \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \times R_{f1} - V_{io}\left(1 + \frac{R_{f1}}{R_{g1}}\right)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, Equation 3 can be simplified as follows:

Equation 4

$$V_{out} = R_{shunt} \times I\left(\frac{R_f}{R_g}\right) - V_{io}\left(1 + \frac{R_f}{R_g}\right) + R_f \times I_{io}$$

The main advantage of using the chopper of the TSZ182 for a low-side current sensing, is that the errors due to V_{io} and I_{io} are extremely low and may be neglected.

Therefore, for the same accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost.

Particular attention must be paid to the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

6.1 DFN8 2x2 package information

Figure 65: DFN8 2x2 package outline

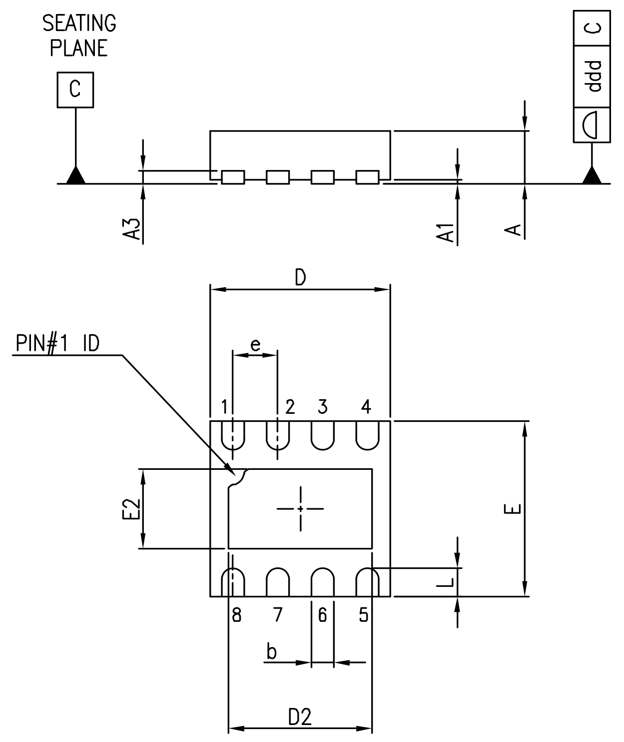
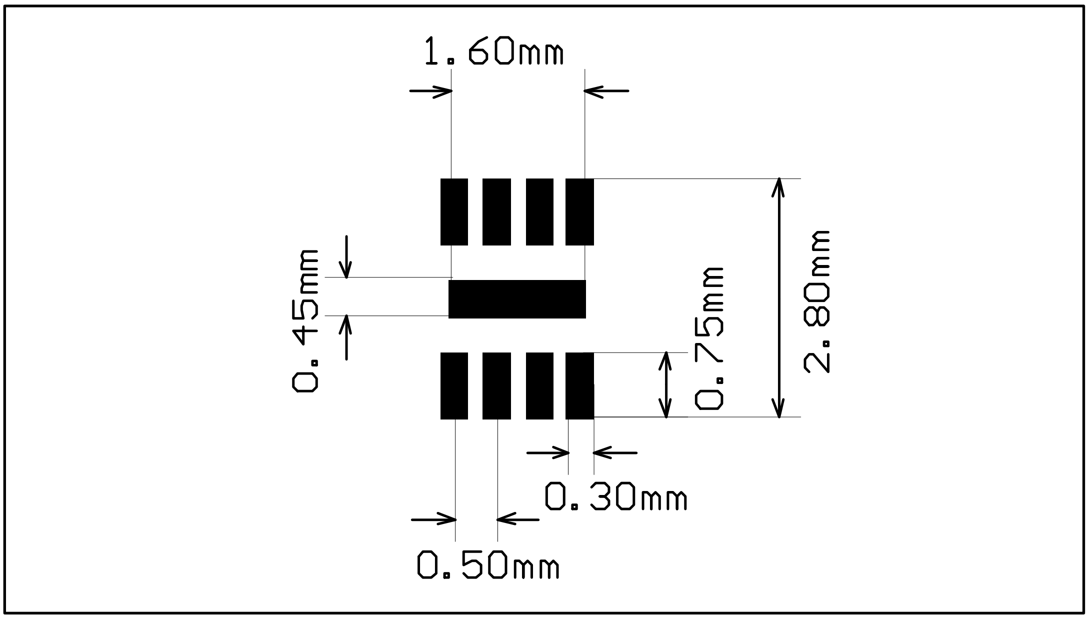


Table 7: DFN8 2x2 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L			0.425			0.017
ddd			0.08			0.003

Figure 66: DFN8 2x2 recommended footprint



6.2 MiniSO8 package information

Figure 67: MiniSO8 package outline

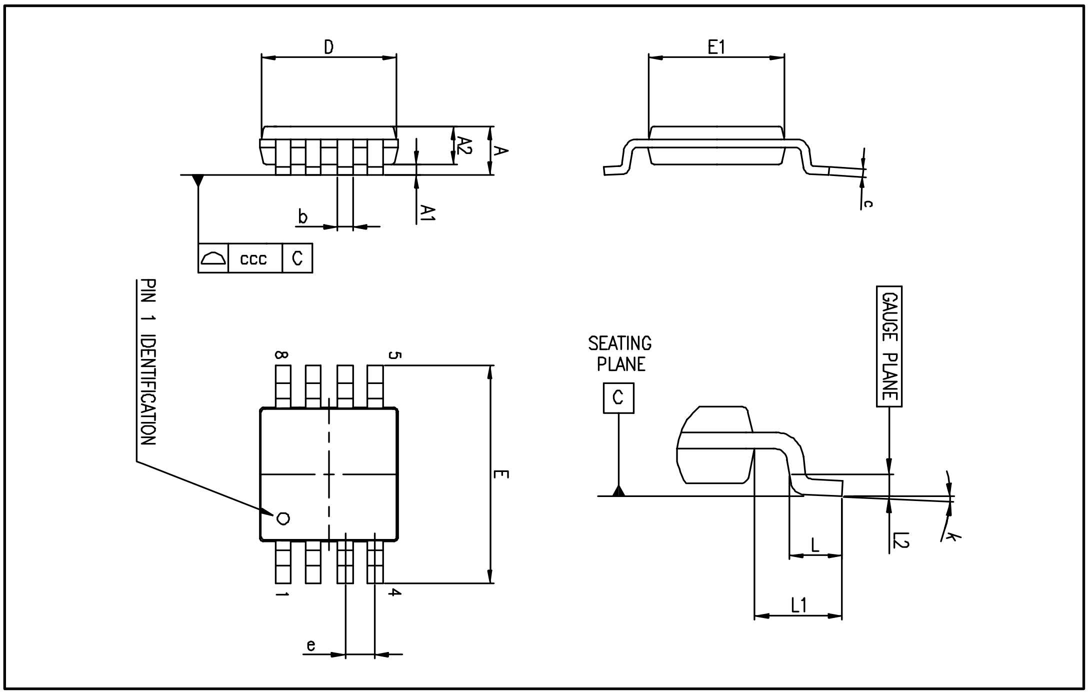


Table 8: MiniSO8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

7 Ordering information

Table 9: Order codes

Order code	Temperature range	Package	Packaging	Marking
TSZ182IQ2T	-40 to 125 °C	DFN8 2x2	Tape and reel	K4G
TSZ182IST	-40 to 125 °C	MiniSO8	Tape and reel	K4G
TSZ182IYST [(1)]	-40 to 125 °C, automotive grade	MiniSO8	Tape and reel	K420

Notes:

[(1)]Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

8 Revision history

Table 10: Document revision history

Date	Revision	Changes
21-Nov-2016	1	Initial release