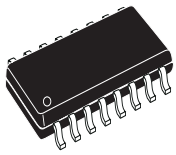
L9610

PWM PowerMOS controller

Features

- High efficiency due to PWM control and PowerMOS driver
- Load dump protection
- Load power limitation
- External PowerMOS protection
- Limited output voltage slew rate



SO16

Description

The L9610C is a monolithic integrated circuit working in PWM mode as controller of an external PowerMOS transistor in high side driver configuration.

Features of the device include controlled slope of the leading and trailing edge of the gate driving voltage, linear current limiting with protection timer, settable switching frequency fo, TTL compatible enable function, protection status ouput pin.

The device is mounted in SO16 micropackage.

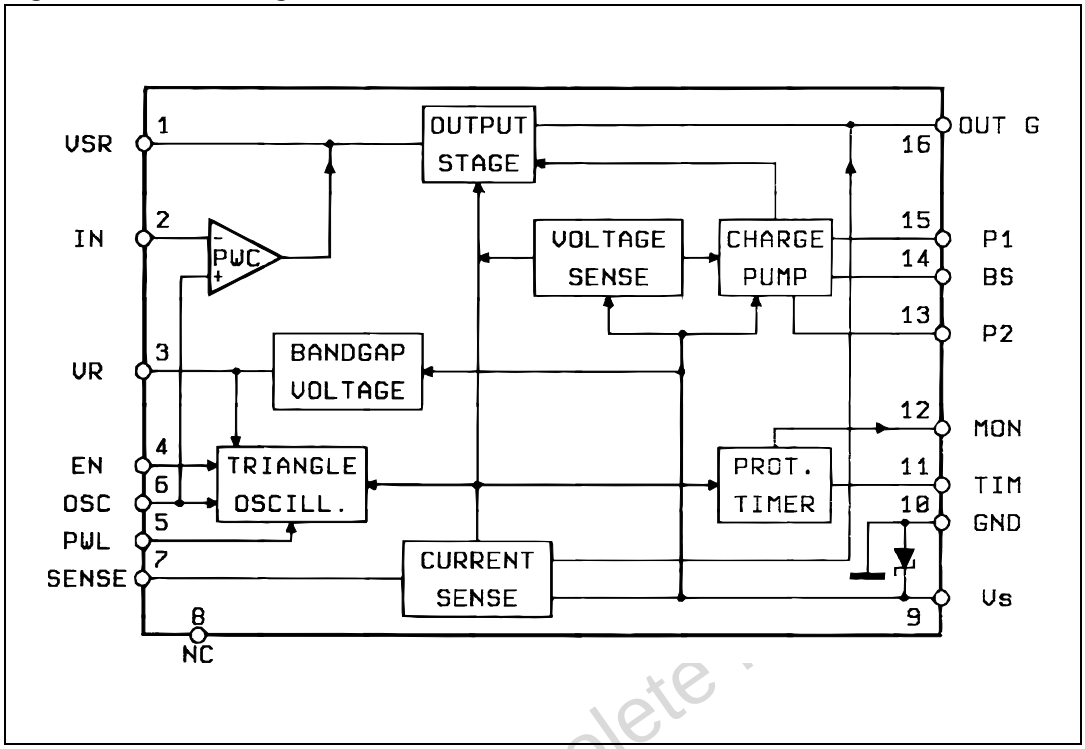
Table 1. Device summary

Order code	Package	Packing
L9610C	SO16N	Tube
L9610C013TR	SO16N	Tape and reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin description

Figure 2. Pin connection (top view)

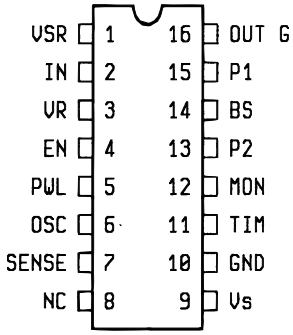


Table 2. Pin functions

Pin	Name	Functions
1	INT	A capacitor connected between this pin and Out$_G$ defines the gate voltage slew rate.
2	IN	Analog input controlling the PWM ratio. The operating range of the input voltage is 0 to V_R.
3	V_R	Output of an internal voltage reference.
4	EN	TTL compatible input for switching off the output.
5	PWL	If this pin is connected to GND and V_S > 13 V, the duty cycle and the frequency f_o are reduced : this allows to transfer a costant power to the load.
6	O_{sc}	Current sink and source stage connection of a triangle oscillator with definite voltage swing.
7	IND	Input of an operational amplifier for short current sensing and regulation.
8	NC	Not connected.
9	V_S	Common supply voltage input.
10	GND	Common ground connection.
11	TIM	A capacitor connected between this pin and GND defines the protection delay time.
12	MON	Open collector monitoring output off the PowerMOS protection.
13, 15	P2, P1	Connection for the charge pump capacitor.
14	BS	The capacitor connected between this pin and the source of the PowerMOS allows to bootstrap the gate driving voltage.
16	Out G	Output for driving the gate of the external PowerMOS.

3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Max. supply voltage	26	V
	Transient peak supply voltage ($R_1 \geq 100\ \Omega$): Load dump: 5 ms ≤ t_{rise} ≤ 10 ms; τ_f Fall time constant = 100 ms; $R_{SOURCE} \geq 0.5\ \Omega$ Field decay: 5 ms ≤ t_{fall} ≤ 10 ms; τ_r Rise time constant = 33 ms; $R_{SOURCE} \geq 10\ \Omega$ Low energy spike: t_{rise} =1 µσ, t_{fall} = 2 ms, $R_{SOURCE} \geq 10\ \Omega$	 60 –80 ±100	 V V V
I_s	Max. supply current (t < 300 ms)	0.3	A
V_{IN}	Input voltage	-0.3 < V_{IN} < V_S - 2.5	V
T_J /T_{stg}	Junction and storage temperature range	-55 to 150	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-alumina	Max.	50	°C/W

3.3 Electrical characteristics

Table 5. Electrical characteristcs
(T_{amb} = -40 °C to 85 °C; 6 V < Vs < 16 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_s	Operating supply voltage		6		16	V
I_q	Quiescent current			2.5	6	mA
V_{SC}	Internal supply voltage clamp	I_S=200 mA	28	32	36	V
V_{SH}	Supply voltage high threshold		16	18.5	21	V
V_{SL}	Supply voltage low threshold		4	5	6	V
V_R	Reference voltage		3.3	3.5	3.7	V
I_R	Reference current	$\Delta V_R \leq 100$ mV			1	mA
V_{INL}	Input low threshold		0.13	0.15	0.2	V_{IN}/V_R

Table 5. Electrical characteristcs (continued)
(T_{amb} = -40 °C to 85 °C; 6 V < Vs < 16 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_F	Oscillator freq. constant	(1)	800		2500	nF/s
K_S	Gate voltage slew rate constant	(2)	3	5	9	nFV/ms
K_T	Protection time delay constant	(3)	0.12		0.44	ms/nF
V_{Si}	Sense input volt.		80	100	120	mV
V_{GON}	Gate driving volt. above V_S	Vs =16 V	8		16	V
V_{GOFF}	Gate voltage in off condition	I_G=100 µA			1.2	V
I_{IN}	Input current		-5	-1		µA
V_{ENL}	Low enable voltage				0.8	V
V_{ENH}	High enable voltage		2.0			V
IEN	Enable input current				2	µA
SR	Slew rate	without C_S		0.5		V/µs
V_{MONsat}	Saturation voltage (pin 12)	$V_{MON = 2.5 mA}$			1.5	V

1. $f_0 = K_F/C_F$
2. $dV_G/(dt) = K_S/C_S$
3. $t_{prot} = K_T C_T$

4 Functional description

4.1 Pulse width comparator

A ground compatible comparator generates the PWM signal which controls the gate of the external PowerMOS. The slopes of the leading and trailing edges of the gate driving signal are defined by the external capacitor C_S according to :

$$dV_G/(dt) = K_S/C_S$$

This feature allows to optimize the switching speed for the power and RFI performance best suited for the application.

The lower limit of the duty cycle is fixed at 15 % of the ratio between the input and the reference voltage (see *Figure 3.*). Input voltages lower than this value disable the internal oscillator signal and therefore the gate driver.

4.2 Ground compatible triangle oscillator

The triangle oscillator provides the switching frequency f_o set by the external capacitor C_F according to:

$$f_0 = K_F/C_F$$

If the pin PWL (power limitation) is connected to ground and Vs is higher than the PWL threshold voltage, the duty cycle and the f_o frequency are reduced: this allows to transfer a costant power to the load (see *Figure 4.*).

4.3 Timer and protection latch

When an overcurrent occurs, the device starts charging the external capacitor C_T ; the protection time is set according to :

$$t_{prot} = K_T \cdot C_T$$

After the overcurrent protection time is reached, the PowerMOS is switched-off ; this condition is latched by setting an internal flip-flop and is externally monitored by the low state of the MON pin.

To reset the latch the supply voltage has to fall below V_{SL} or the device must be switched off.

4.4 Under and overvoltage sense with load dump protection

The undervoltage detection feature resets the timer and switches off the output driving signal when the supply voltage is less than V_{SL}.

If the supply voltage exceeds the max operating supply voltage value, an internal comparator disables the charge pump, the oscillator and the external PowerMOS.

In both cases the thresholds are provided with suitable hysteresis values.

The load dump protection function allows the device to withstand, for a limited time, high overvoltages. It consists of an active clamping diode which limits the circuit supply voltage to

V_{CLAMP} and an external current limiting resistor R_1. The maximum pulse supply current (see abs. max. ratings is equal to 0.3 A. Therefore the maximum load dump voltage is given by:

$$V_{DUMP} = V_{SC} + 0.3R_1$$

In this condition the gate of the PowerMOS is held at the GND pin potential and thus the load voltage is :

$$V_L = V_S - V_{CLAMP} - V_{GS}$$

Figure 3. Typical transfer curve

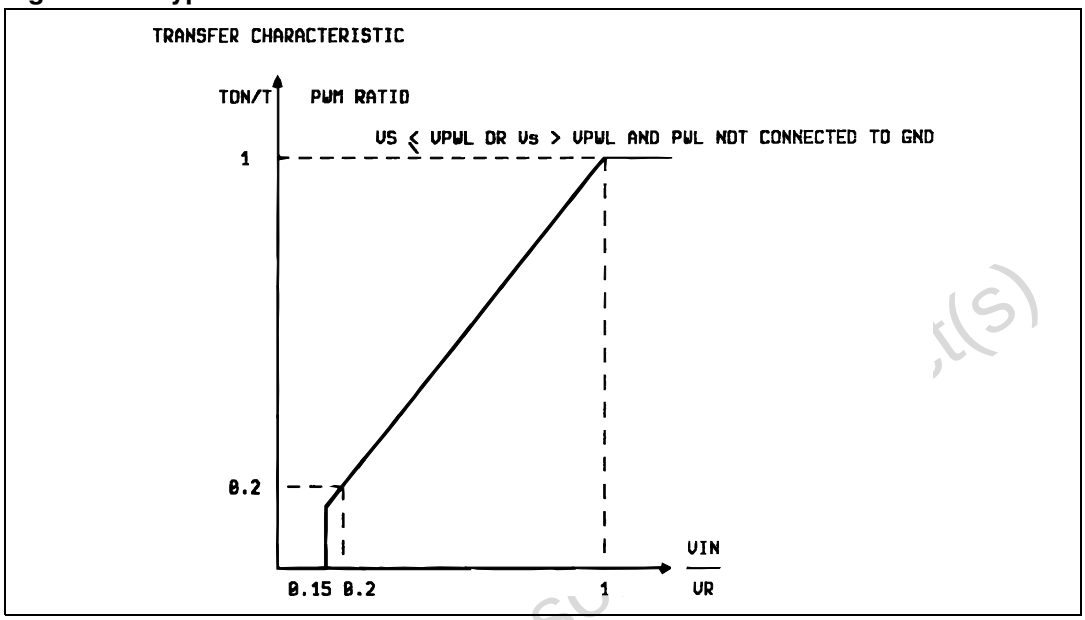
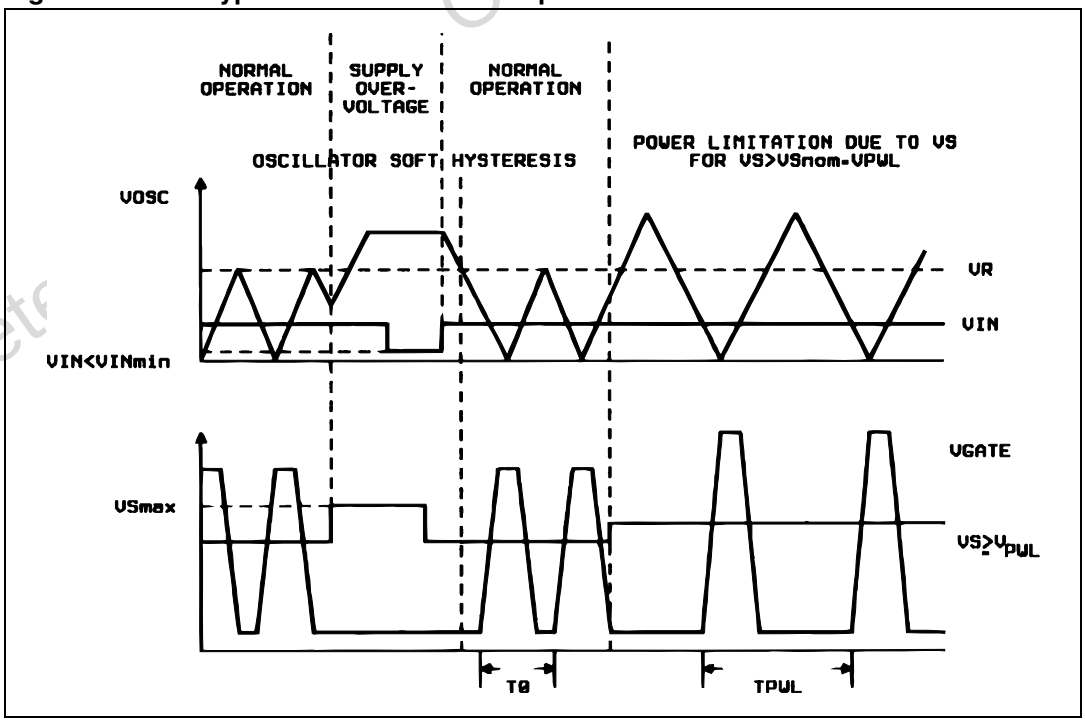


Figure 4. The typical waveforms for the power limitation function



4.5 Short circuit current regulation

The maximum load current in the short circuit condition can be chosen by the value of the current sensing resistor R_S according to :

$$I_{SC} = V_{SI} / R_S$$

Two identical V_S compatible comparators are provided to realize the short circuit protection.

After reaching the lower threshold voltage (typical value V_{SI}-10 mV), the first comparator enables the timer and the gate is driven with the full continuous pump voltage : when the upper threshold voltage value is reached the second comparator maintains the chosen I_{SC} driving the NMOS gate in continuous mode.

This function, showed in *Figure 5.*, speeds up the switch on phase for a lamp as a load.

4.6 Bandgap voltage reference

The circuit provides a reference voltage which may be used as control input voltage through a resistive divider. This reference is protected against the short circuit current.

4.7 Charge pump

The charge pump circuit holds the N-MOS gate above the supply voltage during the ON phase. This circuit consists of an RC astable which drives a comparator with a push-pull output stage. The external charge pump capacitor C_P must be at least equal to the NMOS parasitic input capacitance.

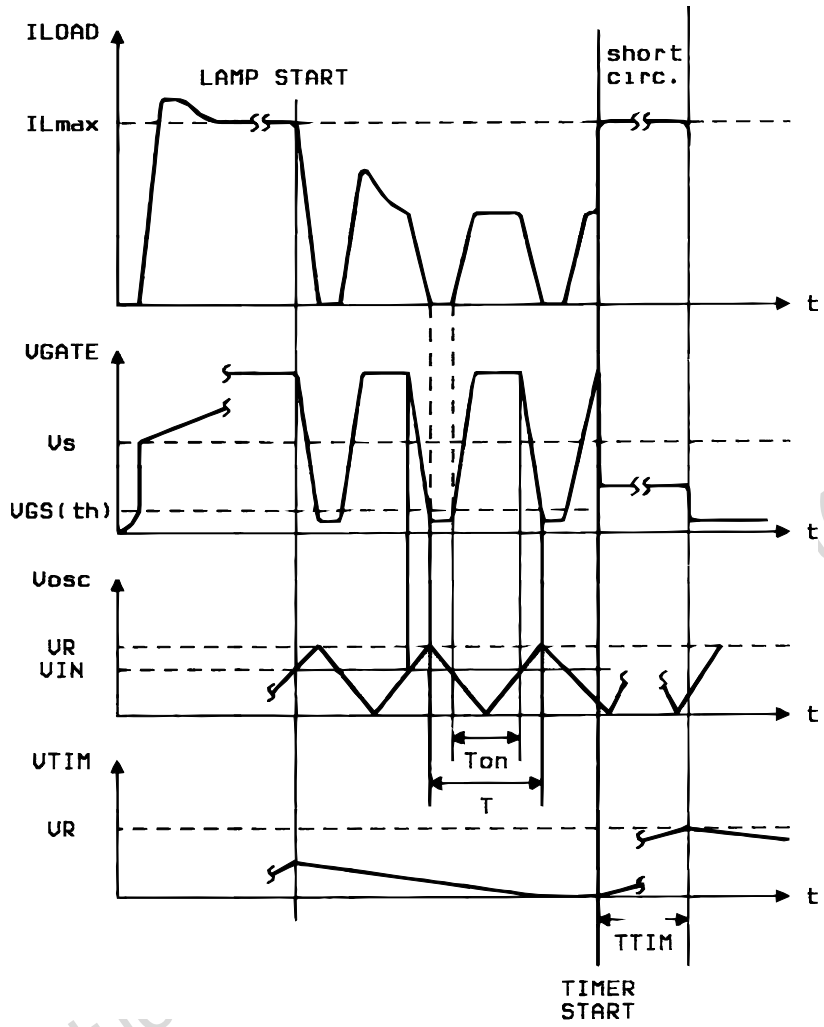
For fast gate voltage variation C_P must be increased or the bootstrap function can be used. The bootstrap capacitor should be at least 10 times greater than the PowerMOS parasitic capacitance.

The charge pump voltage V_{PUMP} can reach to :

$$V_{PUMP} = 2V_S - V_{BE} - V_{CESAT}$$

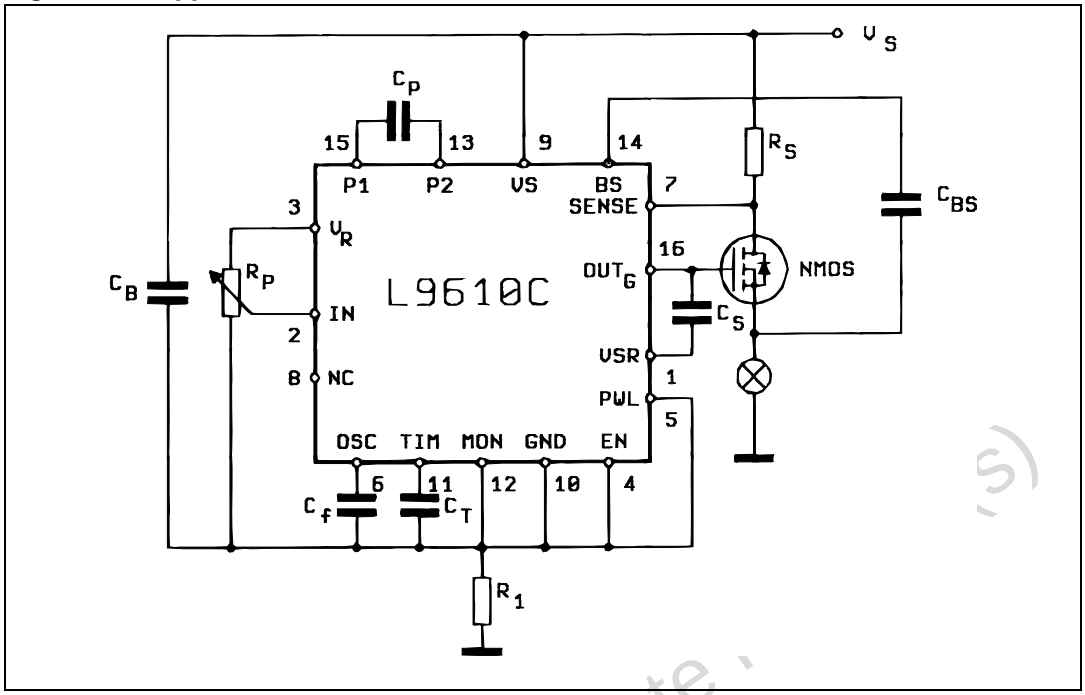
The circuit is disabled if the supply voltage is higher than V_{SH}.

Figure 5. Typical waveforms for short circuit current condition.



5 Application circuit

Figure 6. Application circuit



1. All node voltages are referred to ground pin (GND).
2. The currents flowing in the arrow direction are assumed positive
without C_{BS} : C_P = 1 nF
without C_{BS} : C_{BS} must be at least 10 times higher than the gate capacitance : C_P = 100 pF.

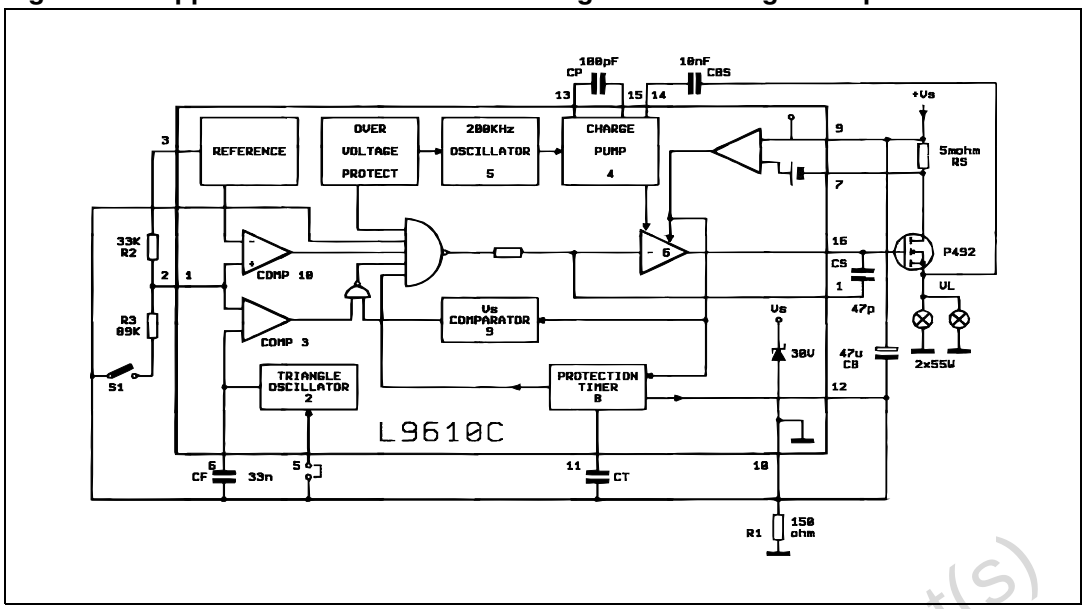
5.1 Controlling a 120 W halogen lamp with the L9610C dimmer

The L9610C lamp dimmer is used to control the brightness of vehicle headlamps using H4 type lamps (see *Figure 7.*). With switch S1 open the full supply voltage is applied to the lamps: closing the switch it is a possible to reduce the average lamp voltage as desired:

$$VL = VS\frac{R3}{R2 + R3}$$

If pin 5 is connected to ground the average lamp voltage is constant, even for supply voltages in excess of 13 V.

Figure 7. Application circuit with controlling a 120 W halogen lamp



The sensing resistor R_S and timing capacitor C_t should be dimensioned according to :

$$R_S = \frac{V_{Si}}{2Inom(@V_S = 14V)}$$

$$C_t = \frac{2 \times \text{limitation time}}{K_T}$$

In normal conditions (V_{CC} = 14 V, maximum brightness) the voltage drop across the sense resistor must be 50 mV. The current limiter intervenes attwice the nominal current, I_{nom}.

The timing capacitor C_t (V_{ct} = 3.5 V) must be chosen so that the delay before intervention is twice the duration of the current limitation at power-on.

The optimal value of the oscillator frequency, taking tolerances into account, must be slightly higher than the frequency at which lamp flicker is noticable (min 60 Hz).

The switching times are a compromise between possible EMI and switching power losses. The recommended value for C_s is 47 pF.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

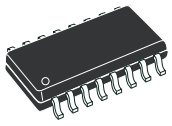
ECOPACK® is an ST trademark.

Figure 8. SO16 narrow mechanical data and package dimensions

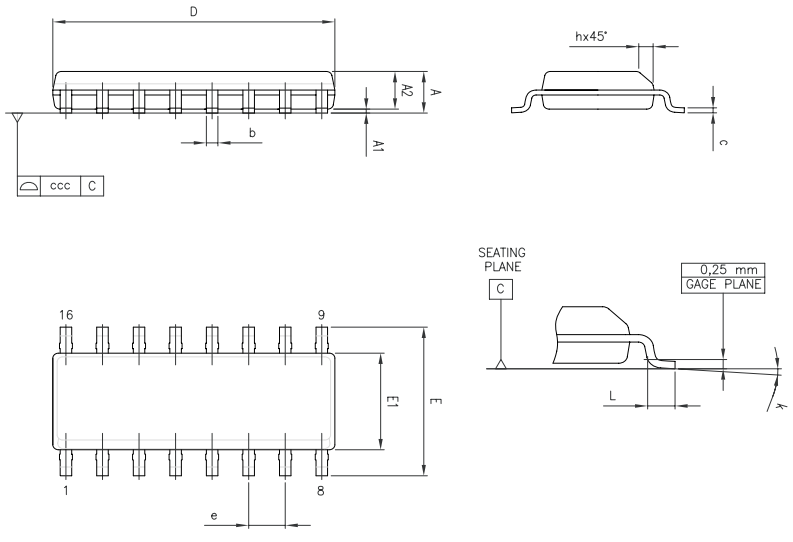
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.750			0.0689
A1	0.100		0.250	0.0039		0.0098
A2	1.250			0.0492		
b	0.310		0.510	0.0122		0.0201
c	0.170		0.250	0.0067		0.0098
D	9.800	9.900	10.000	0.3858	0.3898	0.3937
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1	3.800	3.900	4.000	0.1496	0.1535	0.1575
e		1.270			0.0500	
h	0.250		0.500	0.0098		0.0197
L	0.400		1.270	0.0157		0.0500
k			8.000			0.3150
ccc			0.100			0.0039

"D" do not include mold flash or protrusions
Mold flash, protrusions or gate burrs shall not exceed 0.15mm in total (both side).

OUTLINE AND MECHANICAL DATA



SO16 (Narrow)



7 Revision history

Table 6. Document revision history

Date	Revision	Changes
09-Oct-2000	1	Initial release.
18-Feb-2009	2	Document reformatted. Added *Table 1: Device summary on page 1*. Updated *Section 6: Package information on page 13*.

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