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# 74VHC4040

## 12-Stage Binary Counter

### Features

- High speed;  $f_{MAX} = 210\text{MHz}$  at  $V_{CC} = 5\text{V}$
- Low power dissipation:  $I_{CC} = 4\mu\text{A}$  (Max.) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Power down protection is provided on all inputs
- Wide operating voltage range:  $V_{CC}$  (Opr.) =  $2\text{V} - 5.5\text{V}$
- Low noise:  $V_{OLP} = 0.8\text{V}$  (Max.)
- Pin and function compatible with 74HC4040

### General Description

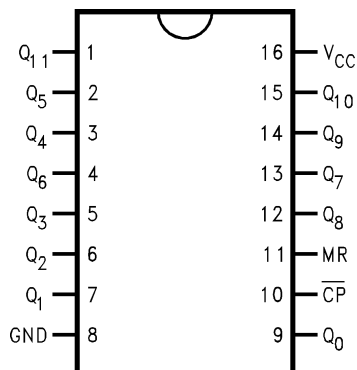
The VHC4040 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC4040 is a 12-stage counter which increments on the negative edge of the input clock and all outputs are reset to a low level by applying a logical high on the reset input. An input protection circuit insures that 0V to 7V can be applied to the inputs without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

### Ordering Information

Order Number	Package Number	Package Description
74VHC4040M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC4040MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

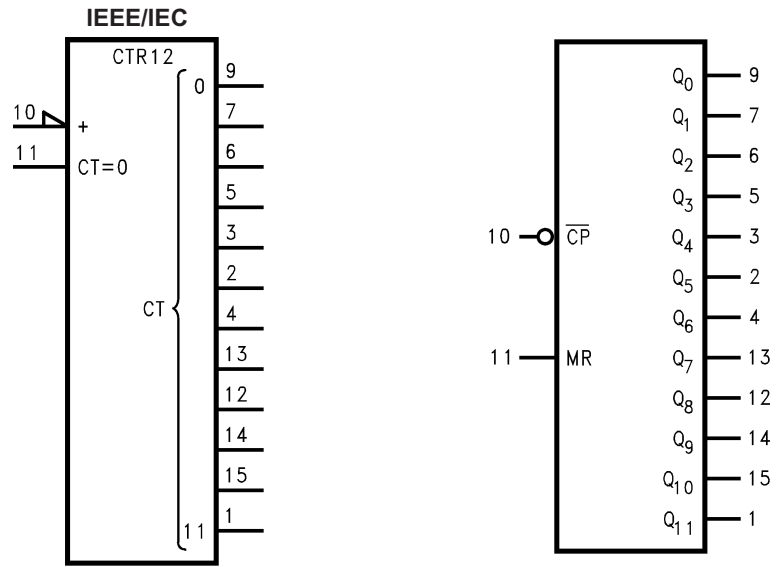
### Connection Diagram



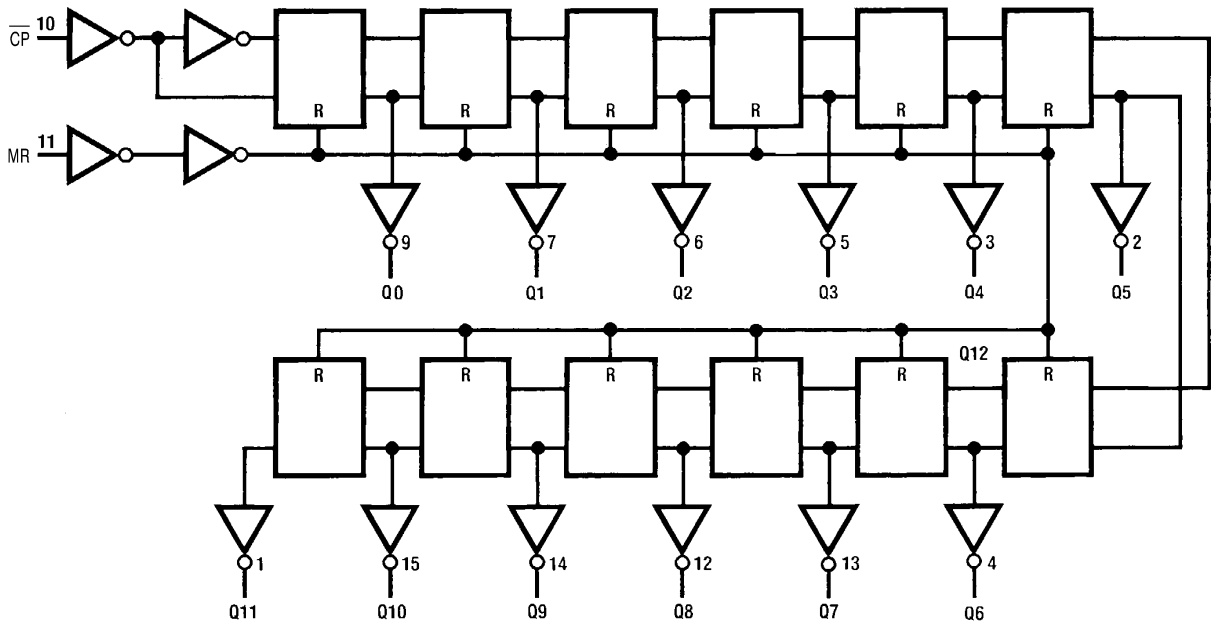
### Pin Descriptions

Pin Names	Description
$Q_0 - Q_{11}$	Flip-Flop Outputs
$\overline{CP}$	Negative Edged Triggered Clock
MR	Master Reset

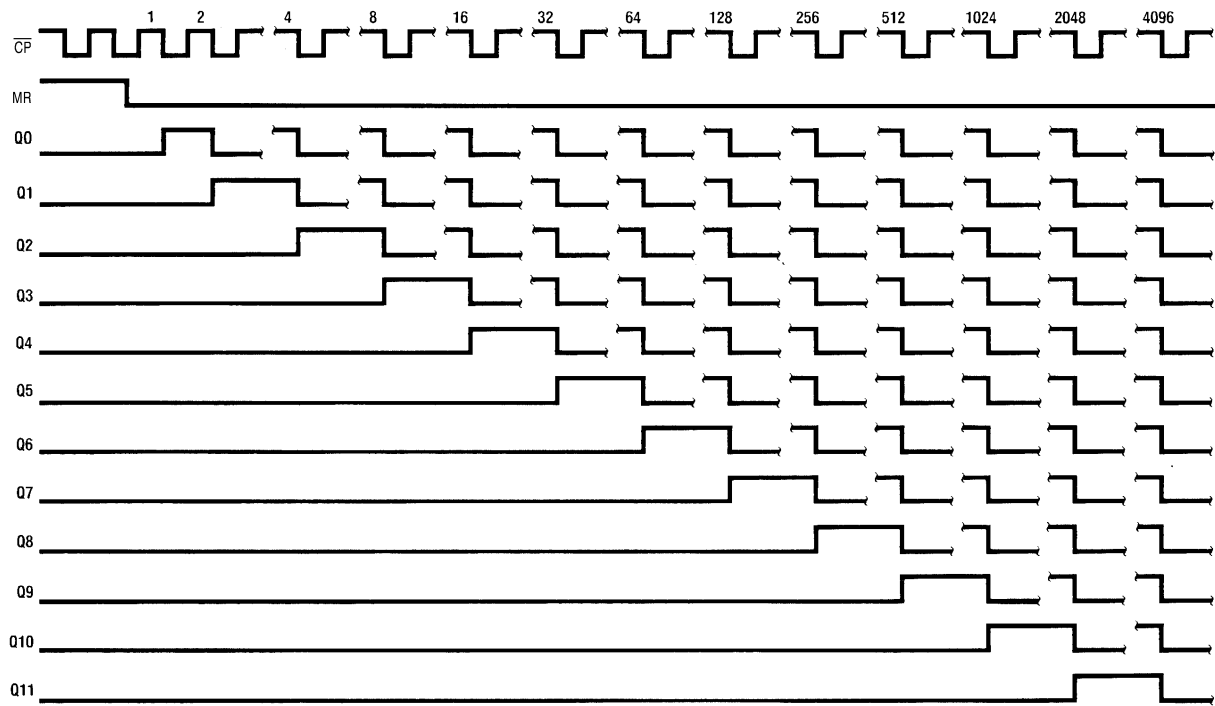
Logic Symbols



Logic Diagram



### Timing Diagram



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$V_{IN}$	DC Input Voltage	-0.5V to +7.0V
$V_{OUT}$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{IK}$	Input Diode Current	-20mA
$I_{OK}$	Output Diode Current	$\pm 20mA$
$I_{OUT}$	DC Output Current	$\pm 25mA$
$I_{CC}$	DC $V_{CC}$ /GND Current	$\pm 75mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to +5.5V
$V_{IN}$	Input Voltage	0V to +5.5V
$V_{OUT}$	Output Voltage	0V to $V_{CC}$
$T_{OPR}$	Operating Temperature	-40°C to +85°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0 ~ 100ns/V 0 ~ 20ns/V

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units		
				Min.	Typ.	Max.	Min.	Max.			
V <sub>IH</sub>	HIGH Level Input Voltage	2.0		1.50			1.50		V		
		3.0 – 5.5		0.7 x V <sub>CC</sub>			0.7 x V <sub>CC</sub>				
V <sub>IL</sub>	LOW Level Input Voltage	2.0				0.50		0.50	V		
		3.0 – 5.5				0.3 x V <sub>CC</sub>		0.3 x V <sub>CC</sub>			
V <sub>OH</sub>	HIGH Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	1.9	2.0		1.9		V	
		3.0			2.9	3.0		2.9			
		4.5			4.4	4.5		4.4			
		3.0			I <sub>OH</sub> = -4mA	2.58			2.48		
		4.5			I <sub>OH</sub> = -8mA	3.94			3.80		
V <sub>OL</sub>	LOW Level Output Voltage	2.0	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA		0.0	0.1		0.1	V	
		3.0				0.0	0.1		0.1		
		4.5				0.0	0.1		0.1		
		3.0			I <sub>OL</sub> = 4mA			0.36			0.44
		4.5			I <sub>OL</sub> = 8mA			0.36			0.44
I <sub>IN</sub>	Input Leakage Current	0 – 5.5	V <sub>IN</sub> = 5.5V or GND				±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND			4.0		40.0		μA	

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time to Q <sub>1</sub>	3.3 ± 0.3	C <sub>L</sub> = 15pF		7.5	11.9	1.0	14.0	ns
			C <sub>L</sub> = 50pF		10.0	15.4	1.0	17.5	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		4.8	7.3	1.0	8.5	ns
			C <sub>L</sub> = 50pF		6.3	9.3	1.0	10.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time between Stages from Q <sub>n</sub> to Q <sub>n+1</sub>	3.3 ± 0.3	C <sub>L</sub> = 15pF						ns
			C <sub>L</sub> = 50pF		2.4	4.4	1.0	5.0	
		5.0 ± 0.5	C <sub>L</sub> = 15pF						ns
			C <sub>L</sub> = 50pF		1.6	3.1	1.0	3.5	
t <sub>PHL</sub>	Propagation Delay Time MR-Q <sub>n</sub>	3.3 ± 0.3	C <sub>L</sub> = 15pF		8.3	12.8	1.0	15.0	ns
			C <sub>L</sub> = 50pF		10.8	16.3	1.0	18.5	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		5.6	8.6	1.0	10.0	ns
			C <sub>L</sub> = 50pF		7.1	10.6	1.0	12.0	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3 ± 0.3	C <sub>L</sub> = 15pF	90	140		75	MHz	
			C <sub>L</sub> = 50pF	55	80		50		
		5.0 ± 0.5	C <sub>L</sub> = 15pF	150	210		125	MHz	
			C <sub>L</sub> = 50pF	95	125		80		
C <sub>IN</sub>	Input Capacitance		V <sub>CC</sub> = Open		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance		(2)		21				pF

## Note:

2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

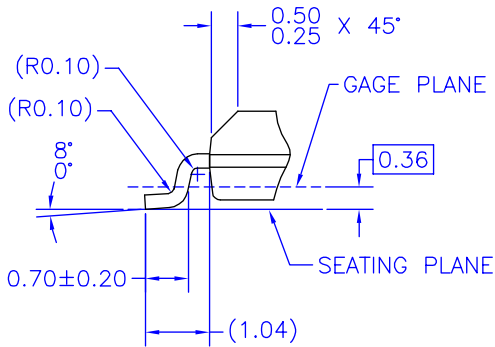
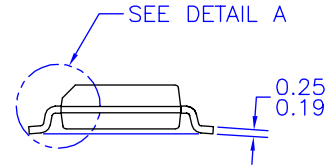
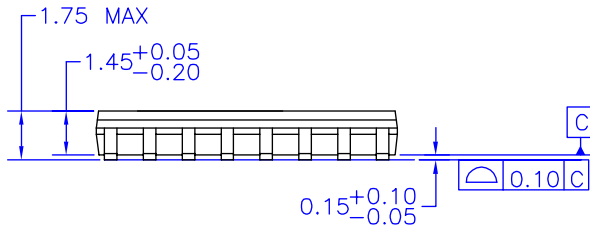
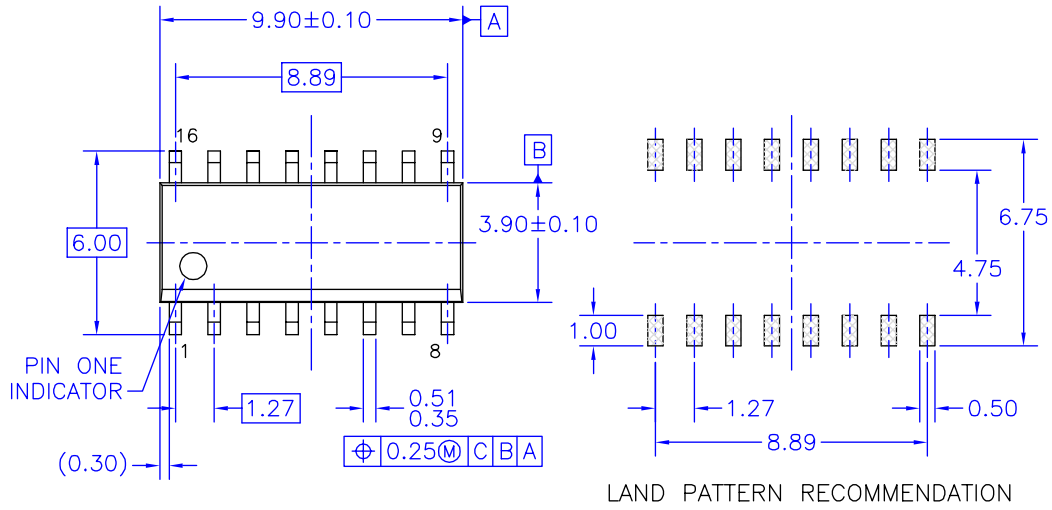
$$I_{CC} (\text{Opr.}) = C_{PD} \cdot V_{CC} \cdot f_N + I_{CC}$$

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to +85°C	Units
			Typ.	Guaranteed Minimum		
t <sub>w(L)</sub> , t <sub>w(H)</sub>	Minimum Pulse Width ( $\overline{CP}$ )	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
t <sub>w(L)</sub>	Minimum Pulse Width (MR)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
t <sub>REC</sub>	Minimum Removal Time (MR)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	

### Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:  
200 MICRONS / 5.08 MICRONS MIN.  
LEAD/TIN (SOLDER) ON COPPER.

DETAIL A  
SCALE: 2:1

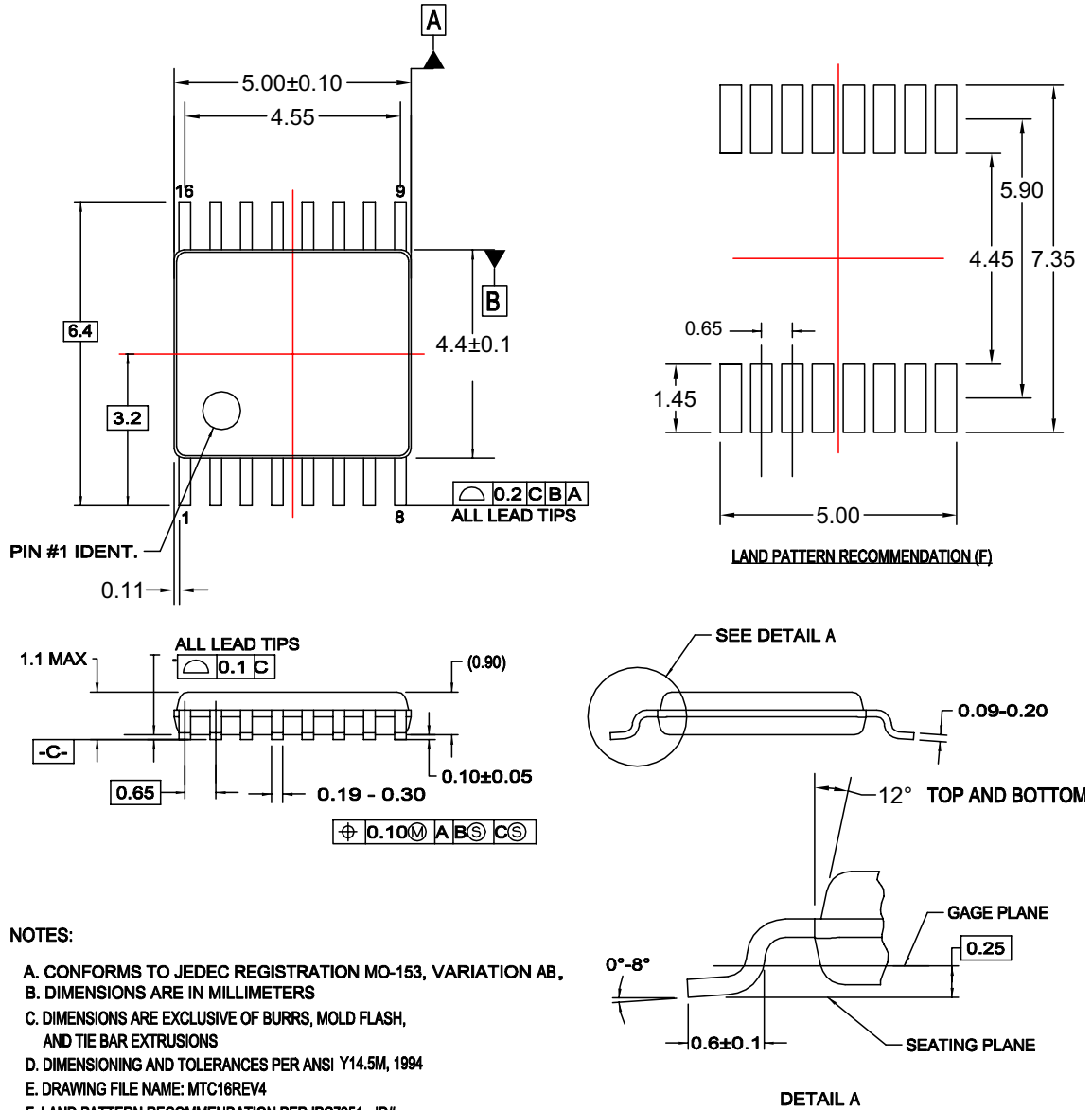
M16AREVK

**Figure 1. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**



**Physical Dimensions** (Continued)

Dimensions are in millimeters unless otherwise noted.



**NOTES:**


- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
- E. DRAWING FILE NAME: MTC16REV4
- F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

**Figure 2. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16**

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