CY14B116K/CY14B116M

16-Mbit (2048 K × 8/1024 K × 16) nvSRAM with Real Time Clock

Features

- 16-Mbit nonvolatile static random access memory (nvSRAM)
  - 25-ns and 45-ns access times
  - Internally organized as 2048 K × 8 (CY14B116K), 1024 K × 16 (CY14B116M)
  - Hands-off automatic STORE on power-down with only a small capacitor
  - STORE to QuantumTrap nonvolatile elements is initiated by software, device pin, or AutoStore on power-down
  - RECALL to SRAM initiated by software or power-up
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- Sleep mode operation
- Full-featured real time clock (RTC)
  - Watchdog timer
  - Clock alarm with programmable interrupts
  - Backup power fail indication
  - Square wave output with programmable frequency (1 Hz, 512 Hz, 4096 Hz, 32.768 kHz)
  - Capacitor or battery backup for RTC
  - Backup current of 0.45 μA (typical)
- Low power consumption
  - Active current of 75 mA at 45 ns
  - Standby mode current of 750 μA
  - Sleep mode current of 10 μA
- Operating voltage: V_{CC} = 2.7 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- Packages
  - 44-pin thin small-outline package (TSOP II)
  - 54-pin thin small-outline package (TSOP II)
  - 165-ball fine-pitch ball grid array (FBGA) package
- Restriction of hazardous substances (RoHS) compliant

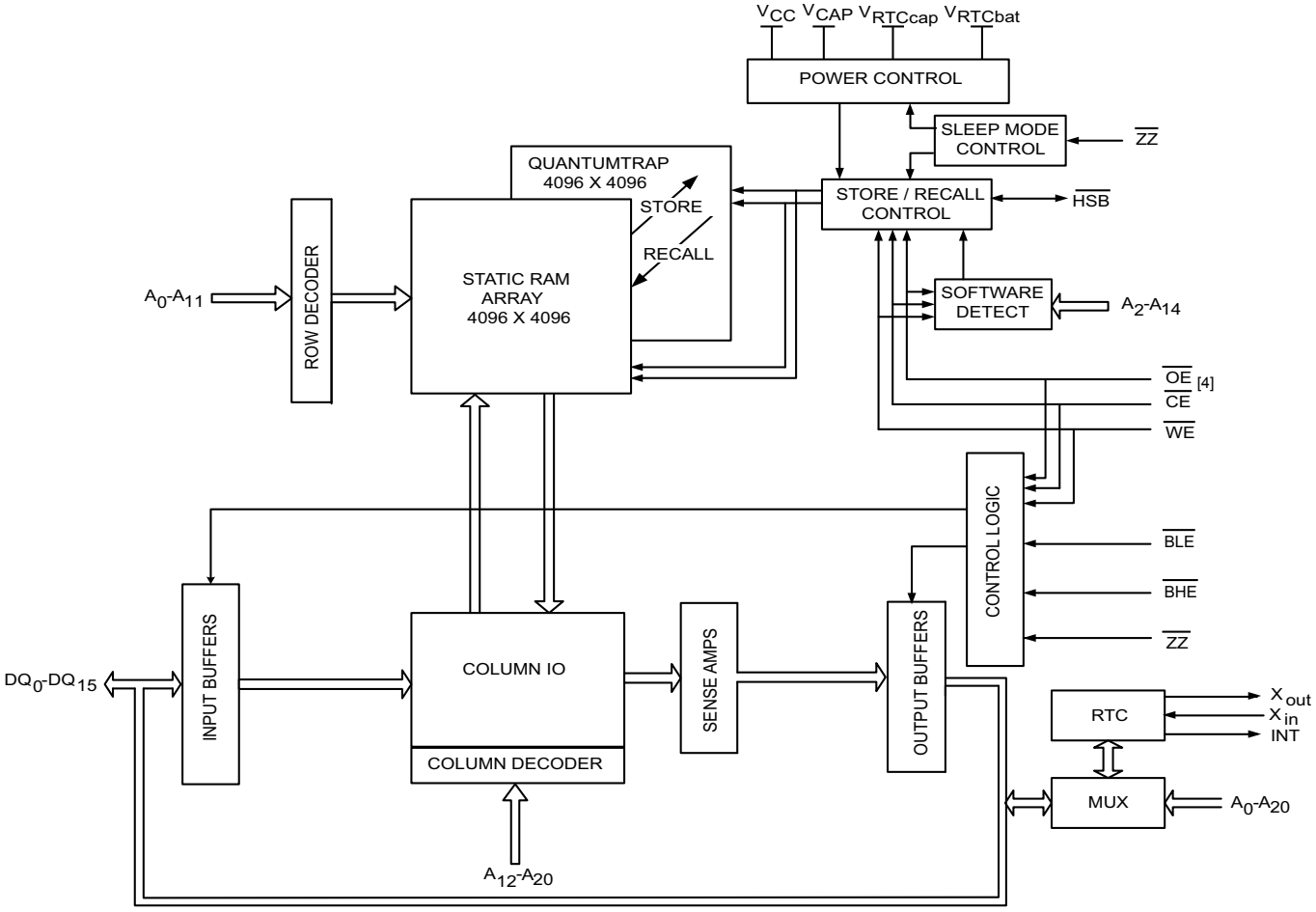
Functional Description

The Cypress CY14B116K/CY14B116M combines a 16-Mbit nvSRAM with a full-featured RTC in a monolithic integrated circuit. The nvSRAM is a fast SRAM with a nonvolatile element in each memory cell. The memory is organized as 2048 K bytes of 8 bits each or 1024 K words of 16 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM can be read and written an infinite number of times. The nonvolatile data residing in the nonvolatile elements do not change when data is written to the SRAM. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

The RTC function provides an accurate clock with leap year tracking and a programmable, high-accuracy oscillator. The alarm function is programmable for periodic minutes, hours, days, or months alarms. There is also a programmable watchdog timer.

For a complete list of related documentation, click here.

Logic Block Diagram[1, 2, 3]



Notes

1. Address A_0–A_{20} for ×8 configuration and address A_0–A_{19} for ×16 configuration.
2. Data DQ_0–DQ_7 for ×8 configuration and data DQ_0–DQ_{15} for ×16 configuration.
3. $\overline{BLE}$, $\overline{BHE}$ are applicable for x16 configuration.
4. TSOP II package is offered in single $\overline{CE}$ and BGA package is offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH.

Contents

Pinouts

Figure 1. Pin Diagram: 44-Pin TSOP II (×8)

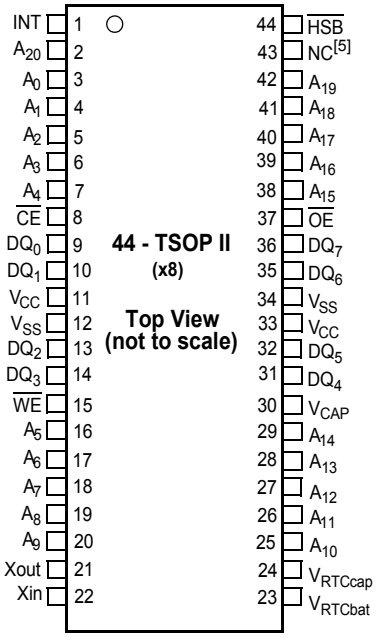


Figure 2. Pin Diagram: 54-Pin TSOP II (×16)

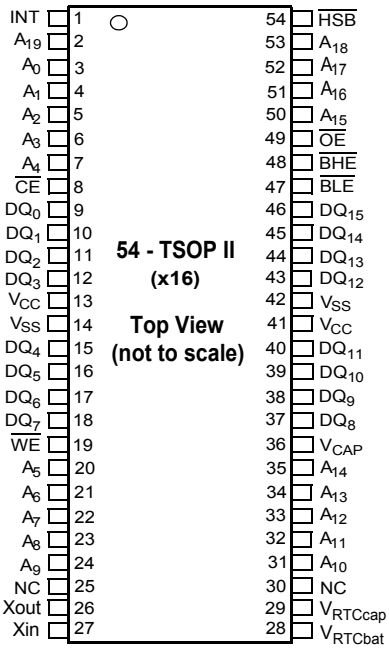


Figure 3. Pin Diagram: 165-Ball FBGA (×16)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A_6	A_8	$\overline{WE}$	$\overline{BLE}$	$\overline{CE}_1$	NC	$\overline{OE}$	A_5	A_3	NC
B	NC	DQ_0	DQ_1	A_4	$\overline{BHE}$	CE_2	NC	A_2	NC	NC	NC
C	$\overline{ZZ}$	NC	NC	V_{SS}	A_0	A_7	A_1	V_{SS}	NC	DQ_{15}	DQ_{14}
D	NC	DQ_2	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	X_{in}	NC	NC
E	NC	V_{CAP}	NC	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	X_{out}	DQ_{13}	NC
F	NC	DQ_3	NC	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	DQ_{12}
G	$\overline{HSB}$	NC	NC	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	NC
H	NC	NC	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	NC	NC
J	NC	NC	NC	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	DQ_8	NC
K	NC	NC	DQ_4	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	NC	NC	NC
L	NC	DQ_5	NC	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	NC	NC	DQ_9
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ_{10}	NC
N	INT	DQ_6	DQ_7	V_{SS}	A_{11}	A_{10}	A_9	V_{SS}	NC	NC	NC
P	NC	NC	NC	A_{13}	A_{19}	V_{RTCbat}	A_{18}	A_{12}	NC	DQ_{11}	NC
R	NC	NC	A_{15}	NC	A_{17}	V_{RTCcap}	A_{16}	NC[5]	A_{14}	NC	NC

Note
5. Address expansion for the 32-Mbit. NC pin not connected to die.

Table 1. Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{20}	Input	Address inputs. Used to select one of the 2,097,152 bytes of the nvSRAM for the ×8 configuration.
A_0–A_{19}		Address inputs. Used to select one of the 1,048,576 words of the nvSRAM for the ×16 configuration.
DQ_0–DQ_7	Input/Output	**Bidirectional data I/O lines for the ×8 configuration**. Used as input or output lines depending on operation.
DQ_0–DQ_{15}		**Bidirectional data I/O lines for the ×16 configuration**. Used as input or output lines depending on operation.
$\overline{WE}$	Input	**Write Enable input, Active LOW**. When selected LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	**Chip Enable input in TSOP II package, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{CE}_1$, CE_2		**Chip Enable input in FBGA package.** The device is selected and a memory access begins on the falling edge of $\overline{CE}_1$ (while CE_2 is HIGH) or the rising edge of CE_2 (while $\overline{CE}_1$ is LOW).
$\overline{OE}$	Input	**Output Enable, Active LOW.** The Active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tristate.
$\overline{BLE}$	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_7–DQ_0.
$\overline{BHE}$	Input	**Byte Enable, Active LOW**. When selected LOW, enables DQ_{15}–DQ_8.
$\overline{ZZ}$[6]	Input	**Sleep Mode Enable.** When the $\overline{ZZ}$ pin is pulled LOW, the device enters a low-power Sleep mode and consumes the lowest power. Since this input is logically AND'ed with $\overline{CE}$, $\overline{ZZ}$ must be HIGH for normal operation.
X_{out}[7]	Output	**Crystal connection**. Drives crystal on start-up.
X_{in}[7]	Input	**Crystal connection.** For 32.768-KHz crystal.
V_{RTCcap}[7]	Power Supply	**Capacitor supplied backup RTC supply voltage**. Left unconnected if V_{RTCbat} is used.
V_{RTCbat}[7]	Power Supply	**Battery supplied backup RTC supply voltage**. Left unconnected if V_{RTCcap} is used.
INT[7]	Output	**Interrupt output/calibration/square wave**. Programmable to respond to the clock alarm, the watchdog timer, and the power monitor. In addition, programmable to be either Active HIGH (push or pull) or LOW (open drain). In the Calibration mode, a 512-Hz square wave is driven out. In the Square Wave mode, you can select a frequency of 1 Hz, 512 Hz, 4,096 Hz, or 32,768 Hz to be used as a continuous output.
V_{CC}	Power Supply	**Power supply inputs to the device**.
V_{SS}	Power Supply	**Ground for the device**. Must be connected to ground of the system.
$\overline{HSB}$	Input/Output	**Hardware STORE Busy ($\overline{HSB}$)**.When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW external to the chip, it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation, HSB is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V_{CAP}	Power Supply	**AutoStore capacitor**. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	NC	**No Connect**. Die pads are not connected to the package pin.

Notes
6. Sleep mode feature is offered only in the 165-ball FBGA package.
7. Left unconnected if RTC feature is not used.

Device Operation

The CY14B116K/CY14B116M nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) automatically at power-down, or from the nonvolatile cell to the SRAM (the RECALL operation) on power-up. Both the STORE and RECALL operations are also available under software control. Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14B116K/CY14B116M supports infinite reads and writes to the SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See the Truth Table For SRAM Operations on page 33 for a complete description of read and write modes.

SRAM Read

The CY14B116K/CY14B116M performs a read cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW, and $\overline{WE}$, $\overline{ZZ}$, and $\overline{HSB}$ are HIGH. The address specified on pins A_0–A_{20} or A_0–A_{19} determines which of the 2,097,152 data bytes or 1,048,576 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_0–DQ_{15} is written into the memory if it is valid t_{SD} before the end of a $\overline{WE}$-controlled write or before the end of a $\overline{CE}$-controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written, in the case of 16-bit words. Keep $\overline{OE}$ HIGH during the entire write cycle to avoid data bus contention on the common I/O lines. If $\overline{OE}$ is left LOW, the internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation (Power-Down)

The CY14B116K/CY14B116M stores data to the nonvolatile QuantumTrap cells using one of the three storage operations. These three operations are: Hardware STORE, activated by the $\overline{HSB}$; Software STORE, activated by an address sequence; AutoStore, on device power-down. The AutoStore operation is a unique feature of nvSRAM and is enabled by default on the CY14B116K/CY14B116M.

During normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a STORE operation during power-down. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC} and a STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If the capacitor is not connected to the V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in the section Preventing AutoStore on page 9. If AutoStore is enabled without a capacitor on the V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the STORE. This corrupts the data stored in the nvSRAM.

Figure 4. AutoStore Mode

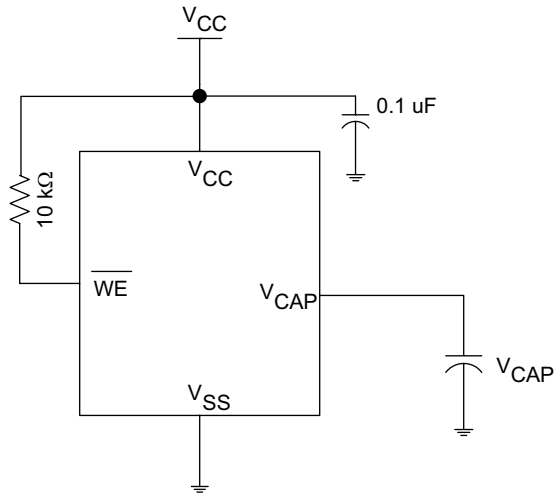


Figure 4 shows the proper connection of the storage capacitor (V_{CAP}) for the automatic STORE operation. Refer to DC Electrical Characteristics on page 22 for the size of the V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{VCAP} by a regulator on the chip. A pull-up resistor should be placed on $\overline{WE}$ to hold it inactive during power-up. This pull-up resistor is only effective if the $\overline{WE}$ signal is in tristate during power-up. When the nvSRAM comes out of power-up-RECALL, the host microcontroller must be active or the $\overline{WE}$ held inactive until the host microcontroller comes out of reset.

To reduce unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place (which sets a write latch) since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place.

Hardware STORE ($\overline{HSB}$) Operation

The CY14B116K/CY14B116M provides the $\overline{HSB}$ pin to control and acknowledge the STORE operations. The $\overline{HSB}$ pin is used to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the device conditionally initiates a STORE operation after t_{DELAY}. A STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver (an internal 100-kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation, $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by an internal 100-kΩ pull-up resistor.

SRAM write operations that are in progress when $\overline{HSB}$ is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after $\overline{HSB}$ goes LOW are inhibited until $\overline{HSB}$ returns HIGH. If the write latch is not set, $\overline{HSB}$ is not driven LOW by the device. However, any of the SRAM read and write cycles are inhibited until $\overline{HSB}$ is returned HIGH by the host microcontroller or another external source.

During any STORE operation, regardless of how it is initiated, the device continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after the $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ unconnected if it is not used.

Hardware RECALL (Power-Up)

During power-up, or after any low-power condition ($V_{CC} < V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on power-up, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the $\overline{HSB}$ pin is driven LOW by the $\overline{HSB}$ driver and all reads and writes to nvSRAM are inhibited.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. A Software STORE cycle is initiated by executing sequential $\overline{CE}$ or $\overline{OE}$ controlled read cycles from six specific address locations in exact order. During the STORE cycle, the previous nonvolatile data is first erased, followed by a store into the nonvolatile elements. After a STORE cycle is initiated, further reads and writes are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence. Otherwise, the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with $\overline{CE}$-controlled reads or $\overline{OE}$-controlled reads, with $\overline{WE}$ kept HIGH for all the six read sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. $\overline{HSB}$ is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operations.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, perform the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Sleep Mode

In Sleep mode, the device consumes the lowest power supply current (I_{ZZ}). The device enters a low-power sleep mode after asserting the $\overline{ZZ}$ pin LOW. After the Sleep mode is registered, the nvSRAM does a STORE operation to secure the data to the nonvolatile memory and then enters the low-power mode. The device starts consuming I_{ZZ} current after t_{SLEEP} time from the instance when the Sleep mode is initiated. When the $\overline{ZZ}$ pin is LOW, all input pins are ignored except the $\overline{ZZ}$ pin. The nvSRAM is not accessible for normal operations while it is in Sleep mode.

When the device enters Sleep mode, the RTC circuit power supply switches to backup power (V_{RTCcap} or V_{RTCbat}) and the crystal oscillator circuit runs into the low-power mode, which is similar to the power-off condition. Whenever the device comes out of Sleep mode, the RTC circuit power switches back to V_{CC} power and will be driven by the main supply (V_{CC}) source.

When the $\overline{ZZ}$ pin is de-asserted (HIGH), there is a delay t_{WAKE} before the user can access the device. If Sleep mode is not used, the $\overline{ZZ}$ pin should be tied to V_{CC}.

Note When nvSRAM enters Sleep mode, it initiates a nonvolatile STORE cycle, which results in losing one endurance cycle for every Sleep mode entry unless data was not written to the nvSRAM since the last nonvolatile STORE/RECALL operation.

Note If the $\overline{ZZ}$ pin is LOW during power-up, the device will not be in Sleep mode. However, the I/Os are in tristate until the $\overline{ZZ}$ pin is de-asserted (HIGH).

Figure 5. Sleep Mode ($\overline{ZZ}$) Flow Diagram

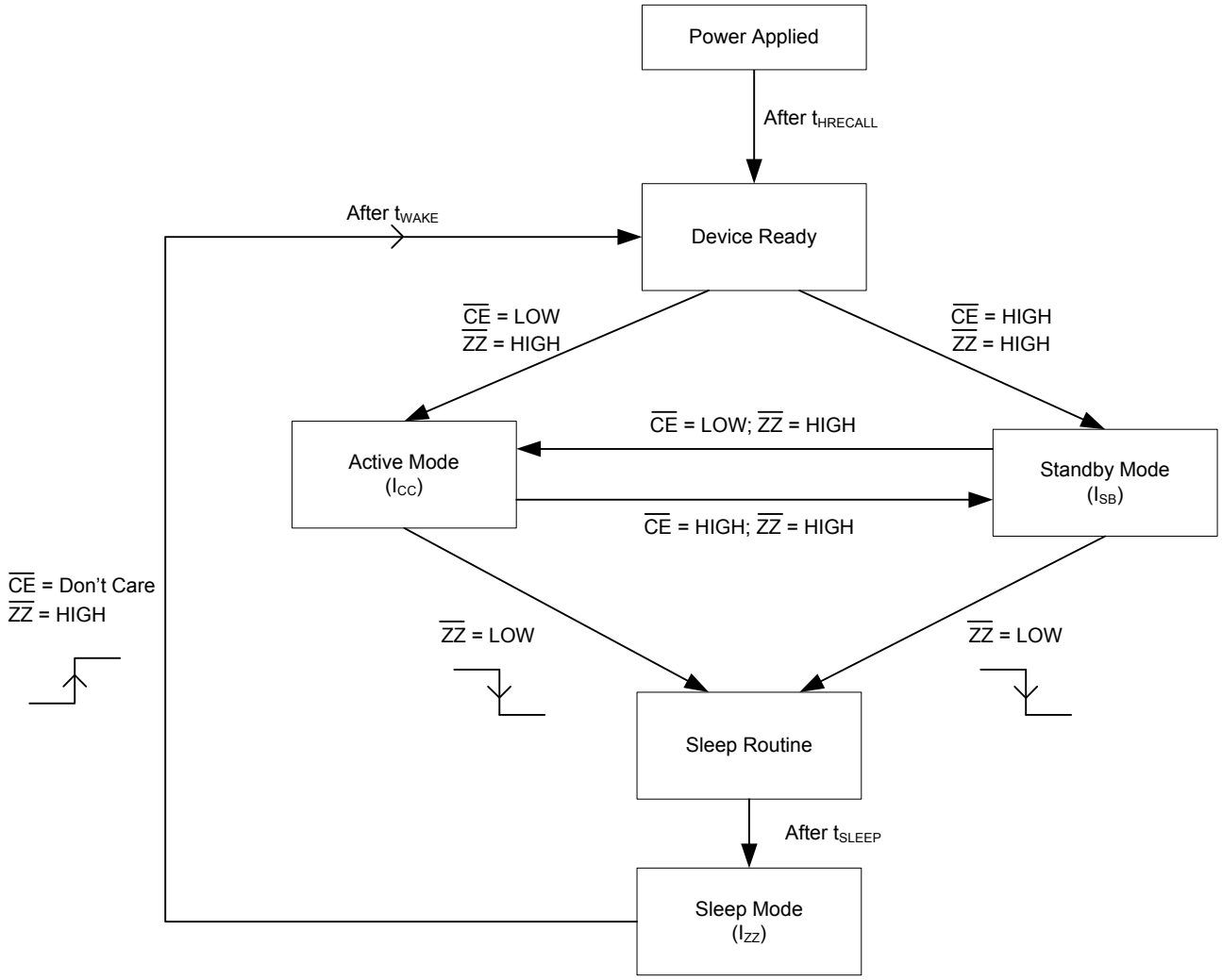


Table 2. Mode Selection

$\overline{CE}$[8]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$, $\overline{BLE}$[9]	A_{15} - A_0[10]	Mode	I/O	Power
H	X	X	X	X	Not selected	Output High Z	Standby
L	H	L	L	X	Read SRAM	Output Data	Active
L	L	X	L	X	Write SRAM	Input Data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[11]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[11]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}[11]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[11]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x8B45 AutoStore Disable

AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ or $\overline{OE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid Read
2. Read address 0xB1C7 Valid Read
3. Read address 0x83E0 Valid Read
4. Read address 0x7C1F Valid Read
5. Read address 0x703F Valid Read
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual software STORE operation must be performed to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

Notes

8. TSOP II package is offered in single $\overline{CE}$ and the BGA package is offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).
9. $\overline{BLE}$, $\overline{BHE}$ are applicable for the x16 configuration only.
10. While there are 21 address lines on the CY14B116K (20 address lines on the CY14B116M), only 13 address lines (A_{14}–A_2) are used to control software modes. The remaining address lines are don't care.
11. The six consecutive address locations must be in the order listed. $\overline{WE}$ must be HIGH during all six cycles to enable a nonvolatile operation.

Data Protection

The CY14B116K/CY14B116M protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14B116K/CY14B116M is in a Write mode at power-up (both $\overline{CE}$ and $\overline{WE}$ are LOW), after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} ($\overline{HSB}$ to output active). This protects against inadvertent writes during power-up or brown out conditions.

Real Time Clock Operation

nvTime Operation

The CY14B116K/CY14B116M offers internal registers that contain clock, alarm, watchdog, interrupt, and control functions. RTC registers use the last 16 address locations of the SRAM. Internal double buffering of the clock and timer information registers prevents accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or the clock accuracy of the internal clock when accessing clock data. Clock and alarm registers store data in BCD format.

RTC functionality is described with respect to CY14B116K in the following sections. The same description applies to CY14B116M, except for the RTC register addresses. The RTC register addresses for CY14B116K range from 0x1FFFF0 to 0x1FFFFF, and for CY14B116M,they range from 0xFFFF0 to 0xFFFFF. Refer to Table 6 on page 17 and Table 7 on page 18 for a detailed Register Map description.

Clock Operations

The clock registers maintain time up to 9,999 years in one-second increments. The time can be set to any calendar time and the clock automatically keeps track of days of the week and month, leap years, and century transitions. There are eight registers dedicated to the clock functions, which are used to set time with a write cycle and to read time during a read cycle. These registers contain the time of day in the BCD format. Bits defined as ‘0’ are currently not used and are reserved for future use by Cypress.

Reading the Clock

The double-buffered RTC register structure reduces the chance of reading incorrect data from the clock. Internal updates to the CY14B116K time-keeping registers are stopped when the read bit ‘R’ (in the Flags register at 0x1FFFF0) is set to ‘1’ before reading clock data to prevent reading of data in transition. Stopping the register updates does not affect clock accuracy.

When a read sequence of the RTC device is initiated, the update of the user time-keeping registers stops and does not restart until a ‘0’ is written to the read bit ‘R’ (in the Flags register at 0x1FFFF0). After the end of a read sequence, all the RTC registers are simultaneously updated within 20 ms.

Setting the Clock

A write access to the RTC device stops updates to the time keeping registers and enables the time to be set when the write bit ‘W’ (in the Flags register at 0x1FFFF0) is set to ‘1’. The correct day, date, and time is then written into the registers and must be in the 24-hour BCD format. The time written is referred to as the “Base Time”. This value is stored in nonvolatile registers and used in the calculation of the current time. When the write bit ‘W’ is cleared by writing ‘0’ to it, the values of timekeeping registers are transferred to the actual clock counters after which the clock resumes normal operation.

If the time written to the time-keeping registers is not in the correct BCD format, each invalid nibble of the RTC registers continues counting to 0xF before rolling over to 0x0, after which RTC resumes normal operation.

Note After the ‘W’ bit is set to ‘0’, values written into the time-keeping, alarm, calibration, and interrupt registers are transferred to the RTC time keeping counters in t_{RTCp} time. These counter values must be saved to nonvolatile memory either by initiating a Software/Hardware STORE or AutoStore operation. While working in the AutoStore Disabled mode, perform a STORE operation after t_{RTCp} after writing into the RTC registers for the modifications to be correctly recorded.

Backup Power

The RTC in the CY14B116K is intended for a permanently powered operation. The V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When the primary power, V_{CC}, fails and drops below V_{SWITCH} the device switches to the backup power supply.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of the clock operation with the primary source removed, the data stored in the nvSRAM is secure, having been stored in the nonvolatile elements when power was lost.

During the backup operation, the CY14B116K consumes 0.45 μA (Typical) at room temperature. Choose the capacitor or battery values according to your application.

Backup time values based on maximum current specifications are shown in the following table. Nominal backup times are approximately two times longer.

Table 3. RTC Backup Time

Capacitor Value	Backup Time (CY14B116K)
0.1F	2.5 days
0.47F	12 days
1.0F	25 days

Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up. If a battery is used, a 3-V lithium battery is recommended and the CY14B116K sources current only from the battery when the primary power is removed. However, the battery is not recharged at any time by the CY14B116K. The battery capacity must be chosen for total anticipated cumulative down time required over the life of the system.

Stopping and Starting the Oscillator

The OSCEN bit in the calibration register at 0x1FFFF8 controls enabling and disabling of the oscillator. This bit is nonvolatile and is shipped to customers in the “enabled” (set to ‘0’) state. To preserve the battery life when the system is in storage, OSCEN must be set to ‘1’. This turns off the oscillator circuit, extending the battery life. If the OSCEN bit goes from disabled to enabled, it takes approximately one second (two seconds maximum) for the oscillator to start.

While the system power is off, if the voltage on the backup supply (V_{RTCcap} or V_{RTCbat}) falls below their respective minimum levels, the oscillator may fail. The CY14B116K can detect oscillator failure when system power is restored. This is recorded in the Oscillator Fail Flag (OSCF) of the Flags register at the address 0x1FFFF0. When the device is powered on (V_{CC} goes above V_{SWITCH}), the OSCEN bit is checked for the ‘enabled’ status. If the OSCEN bit is enabled and the oscillator is not active within the first 5 ms, the OSCF bit is set to ‘1’. The system must check for this condition and then write ‘0’ to clear the flag.

Note that in addition to setting the OSCF flag bit, the time registers are reset to the ‘Base Time’, which is the value last written to the timekeeping registers. The control or calibration registers and the OSCEN bit are not affected by the ‘oscillator failed’ condition.

The value of OSCF must be reset to ‘0’ when the time registers are written for the first time. This initializes the state of this bit, which may have been set when the system was first powered on.

To reset OSCF, set the write bit ‘W’ (in the Flags register at 0x1FFFF0) to a ‘1’ to enable writes to the Flags register. Write a ‘0’ to the OSCF bit and then reset the write bit to ‘0’ to disable writes.

Calibrating the Clock

The RTC is driven by a quartz-controlled crystal with a nominal frequency of 32.768 kHz. The clock accuracy depends on the quality of the crystal and calibration. The crystals available in the market typically have an error of $\pm$20 ppm to $\pm$35 ppm. However, CY14B116K employs a calibration circuit that improves the accuracy to +1/–2 ppm at any given temperature. This implies an error of +2.5 seconds to –5 seconds per month.

The calibration circuit adds or subtracts counts from the oscillator divider circuit to achieve this accuracy. The number of pulses that are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the Calibration register at 0x1FFFF8. The calibration bits occupy the five lower order bits in the Calibration register. These bits are set to represent any value between ‘0’ and 31 in binary form. Bit D5 is a sign bit, where a ‘1’ indicates positive calibration and a ‘0’ indicates negative calibration. Adding counts speeds the clock up and subtracting counts slows the clock down. If a binary ‘1’ is loaded into the register, it corresponds to an adjustment of 4.068 or –2.034-ppm offset in oscillator error, depending on the sign.

Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once every minute, have one second shortened by 128 or lengthened by 256 oscillator cycles. If a binary ‘1’ is loaded into the register, only the first two minutes of the 64-minute cycle are modified. If a binary 6 is loaded, the first 12 are affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is, 4.068 or –2.034 ppm of adjustment for every calibration step in the Calibration register.

To determine the required calibration, the CAL bit in the Flags register (0x1FFFF0) must be set to ‘1’. This causes the INT pin to toggle at a nominal frequency of 512 Hz. Any deviation measured from 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.01024 Hz indicates a +20-ppm error. Hence, a decimal value of –10 (001010b) must be loaded into the Calibration register to offset this error.

Note Setting or changing the Calibration register does not affect the test output frequency.

To set or clear CAL, set the write bit ‘W’ (in the flags register at 0x1FFFF0) to ‘1’ to enable writes to the flags register. Write a value to CAL, and then reset the write bit to ‘0’ to disable writes.

Alarm

The alarm function compares user-programmed values of alarm time and date (stored in the registers 0x1FFFF2-0x1FFFF5) with the corresponding time of day and date values. When a match occurs, the alarm interrupt flag (AF) is set and an interrupt is generated on the INT pin if the Alarm Interrupt Enable (AIE) bit is set.

There are four alarm match fields – date, hours, minutes, and seconds. Each of these fields has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to ‘0’ indicates that the corresponding field is used in the match process. Depending on the match bits, the alarm occurs as specifically as once a month or as frequently as once every minute. Selecting none of the match bits (all 1s) indicates that no match is required and therefore, the alarm is disabled. Selecting all match bits (all 0s) causes an exact time and date match.

There are two ways to detect an alarm event: by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0x1FFFF0 indicates that a date or time match has occurred. The AF bit is set to ‘1’ when a match occurs. Reading the flags register clears the alarm flag bit (and all of the register bits). A hardware interrupt pin may also be used to detect an alarm event.

To set, clear or enable an alarm, set the 'W' bit (in Flags Register – 0x1FFFF0) to '1' to enable writes to Alarm Registers. After writing the alarm value, clear the 'W' bit back to '0' for the changes to take effect.

Note CY14B116K requires the alarm match bit for seconds (bit 'D7' in Alarm-Seconds register 0x1FFFF2) to be set to '0' for proper operation of Alarm Flag and Interrupt.

Watchdog Timer

The Watchdog Timer is a free-running down counter that uses the 32 Hz (31.25 ms period) clock derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the Watchdog Timer register 0x1FFFF7.

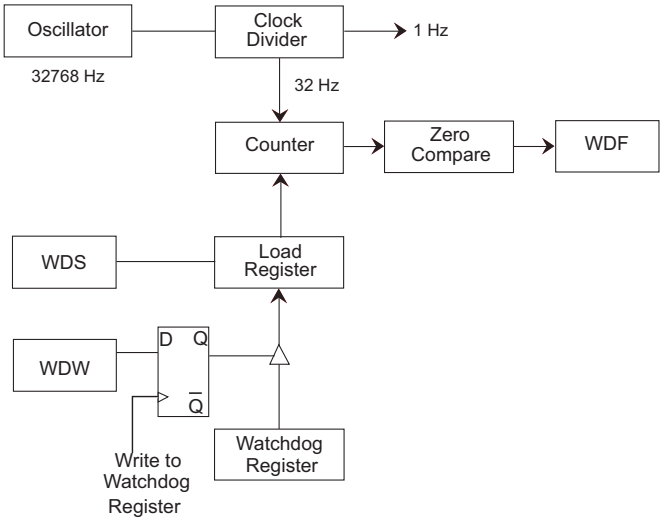
Note Since the Watchdog Timer uses a free-running 32-Hz (31.25 ms period) clock, the start of countdown has a delay between 0 ms and 31.25 ms.

The timer consists of a loadable register and a free-running counter. On power-up, the watchdog timeout value in register 0x1FFFF7 is loaded in the Counter Load register, which is shown in Figure 6. Counting begins on power-up and restarts from the loadable value any time the Watchdog Strobe (WDS) bit is set to '1'. The counter is compared to the terminal value of '0'. If the counter reaches this value, it causes an internal flag and an optional interrupt output. You can prevent the timeout interrupt by setting the WDS bit to '1' prior to the counter reaching '0'. This causes the counter to reload with the watchdog timeout value and to be restarted. If you set the WDS bit prior to the counter reaching the terminal value, the interrupt does not occur and the watchdog timer flag is not set.

New timeout values are written by setting the Watchdog Write (WDW) bit to '0'. When the WDW is '0', new writes to the watchdog timeout value bits D5–D0 are enabled to modify the timeout value. When WDW is '1', writes to bits D5–D0 are ignored. The WDW function enables you to set the WDS bit, without concern that the watchdog timer value is modified. A logical diagram of the watchdog timer is shown in Figure 6. Note that setting the watchdog timeout value to '0' disables the watchdog function.

The output of the watchdog timer is the flag bit WDF that is set if the watchdog is allowed to time out. If the Watchdog Interrupt Enable (WIE) bit in the Interrupt register is set, a hardware interrupt on the INT pin is also generated on watchdog timeout. The flag and the hardware interrupt are both cleared when you read the Flags register.

Figure 6. Watchdog Timer Block Diagram



Programmable Square Wave Generator

The square wave generator block uses the crystal output to generate a desired frequency on the INT pin of the device. The output frequency can be programmed to be one of the following:

1. 1 Hz
2. 512 Hz
3. 4096 Hz
4. 32768 Hz

The square wave output is not generated while the device is running on backup power.

Power Monitor

The CY14B116K provides a power management scheme with power fail interrupt capability. It also controls the internal switch to back up power for the clock and protects the memory from low V_{CC} access. The power monitor is based on an internal bandgap reference circuit that compares the V_{CC} voltage to V_{SWITCH} threshold.

When V_{SWITCH} is reached, as V_{CC} decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source, read and write operations to nvSRAM are inhibited and the RTC functions are not available to the user. The RTC clock continues to operate in the background. The updated RTC time keeping registers are available to the user after V_{CC} is restored to the device (see "AutoStore/Power-Up RECALL Characteristics" on page 29).

Backup Power Monitor

The CY14B116K provides a backup power monitoring system that detects the backup power (either battery or capacitor backup) failure. The backup power fail flag (BPF) is issued on the next power-up if the backup power fails. The BPF flag is set in the event of backup voltage falling lower than $V_{BAKFAIL}$. The backup power is monitored even while the RTC is running in the backup mode. Low voltage detected during the backup mode is flagged through the BPF flag. BPF can hold the data only until a defined low level of the back up voltage (V_{DR}).

Interrupts

The CY14B116K has a Flags register, Interrupt register, and Interrupt logic that can signal interrupt to the microcontroller. There are three potential sources for interrupt: watchdog timer, power monitor, and alarm timer. Each of these can be individually enabled to drive the INT pin by appropriate setting in the Interrupt register (0x1FFFF6). In addition, each has an associated flag bit in the Flags register (0x1FFFF0) that the host processor uses to determine the cause of the interrupt. The INT pin driver has two bits that specify its behavior when an interrupt occurs.

An Interrupt is raised only if both a flag is raised by one of the three sources and the respective interrupt enable bit in the Interrupts register is enabled (set to ‘1’). After an interrupt source is active, two programmable bits, H/L and P/L, determine the behavior of the output pin driver on the INT pin. These two bits are located in the Interrupt register and can be used to drive Level or Pulse mode output from the INT pin. In the Pulse mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In the Level mode, the pin goes to its active polarity until you read the Flags register. This mode is used as an interrupt to a host microcontroller. The control bits are summarized in the following section.

Interrupts are only generated while working on normal power and are not triggered when the system runs in the backup power mode.

Note CY14B116K generates valid interrupts only after the Powerup RECALL sequence is completed. All events on the INT pin must be ignored for $t_{HRECALL}$ duration after power-up.

Interrupt Register

Watchdog Interrupt Enable (WIE). When set to ‘1’, the watchdog timer drives the INT pin and an internal flag when a watchdog timeout occurs. When WIE is set to ‘0’, the watchdog timer only affects the WDF flag in Flags register.

Alarm Interrupt Enable (AIE). When set to ‘1’, the alarm match drives the INT pin and an internal flag. When AIE is set to ‘0’, the alarm match only affects the AF flag in the Flags register.

Power Fail Interrupt Enable (PFE). When set to ‘1’, the power fail monitor drives the INT pin and an internal flag. When PFE is set to ‘0’, the power fail monitor only affects the PF flag in the Flags register.

Square Wave Enable (SQWE). When set to ‘1’, a square wave of programmable frequency is generated on the INT pin. The frequency is decided by the SQ1 and SQ0 bits of the interrupts register. This bit is nonvolatile and survives the power cycle. The SQWE bit overrides all other interrupts. However, the CAL bit will take precedence over the square wave generator. This bit defaults to ‘0’ from the factory.

High/Low (H/L). When set to ‘1’, the INT pin is active HIGH and the driver mode is push pull. The INT pin drives HIGH only when V_{CC} is greater than V_{SWITCH}. When set to ‘0’, the INT pin is active LOW and the Drive mode is open drain. The INT pin must be pulled up to V_{CC} by a 10-kΩ resistor while using the interrupt in active LOW mode.

Pulse/Level (P/L). When set to ‘1’ and an interrupt occurs, the INT pin is driven active (determined by H/L) for approximately 200 ms. When P/L is set to ‘0’, the INT pin is driven HIGH or LOW (determined by H/L) until the Flags or Control register is read.

SQ1 and SQ0. These bits are used together to fix the frequency of the square wave on the INT pin output when the SQWE bit is set to ‘1’. These bits are nonvolatile and survive the power cycle. The output frequency is decided as illustrated in the following table.

Table 4. Square Wave Output Selection

SQ1	SQ0	Frequency	Comment
0	0	1 Hz	1 Hz signal
0	1	512 Hz	512 Hz clock output
1	0	4096 Hz	4 KHz clock output
1	1	32768 Hz	Oscillator output frequency

While using more than one of the interrupt sources and an interrupt source activates the INT pin, the external host must read the Flags Register to determine the cause of the interrupt. Remember that all the flags are cleared when the Flags register is read. If the INT pin is programmed for the Level mode, then reading the flag clears the flag and the INT pin returns to its inactive state. If the pin is programmed for the Pulse mode, then reading the flag clears the flag and the pin. The pulse does not complete its specified duration if the Flags register is read. If the INT pin is used as a host reset, then the Flags or Control register is not read during a reset.

Setting the calibration bit CAL = ‘1’ or SQWE = ‘1’ enables square wave output on the INT pin. In this situation, the CAL bit setting gets priority over the SQWE bit and enables the 512-Hz digital clock output on the INT pin for calibration. The CAL bit does not survive the power cycle and resets to zero during the next power-up cycle. The setting of SQWE, SQ0 and SQ1, requires AutoStore or software STORE to keep the setting of these bits nonvolatile and enable them to survive the power cycle. When multiple sources are set to drive the interrupt pin (INT), then the following priority will be followed to resolve ambiguity as to which cause drives the INT pin.

Following is a summary table that shows the state of the INT pin,

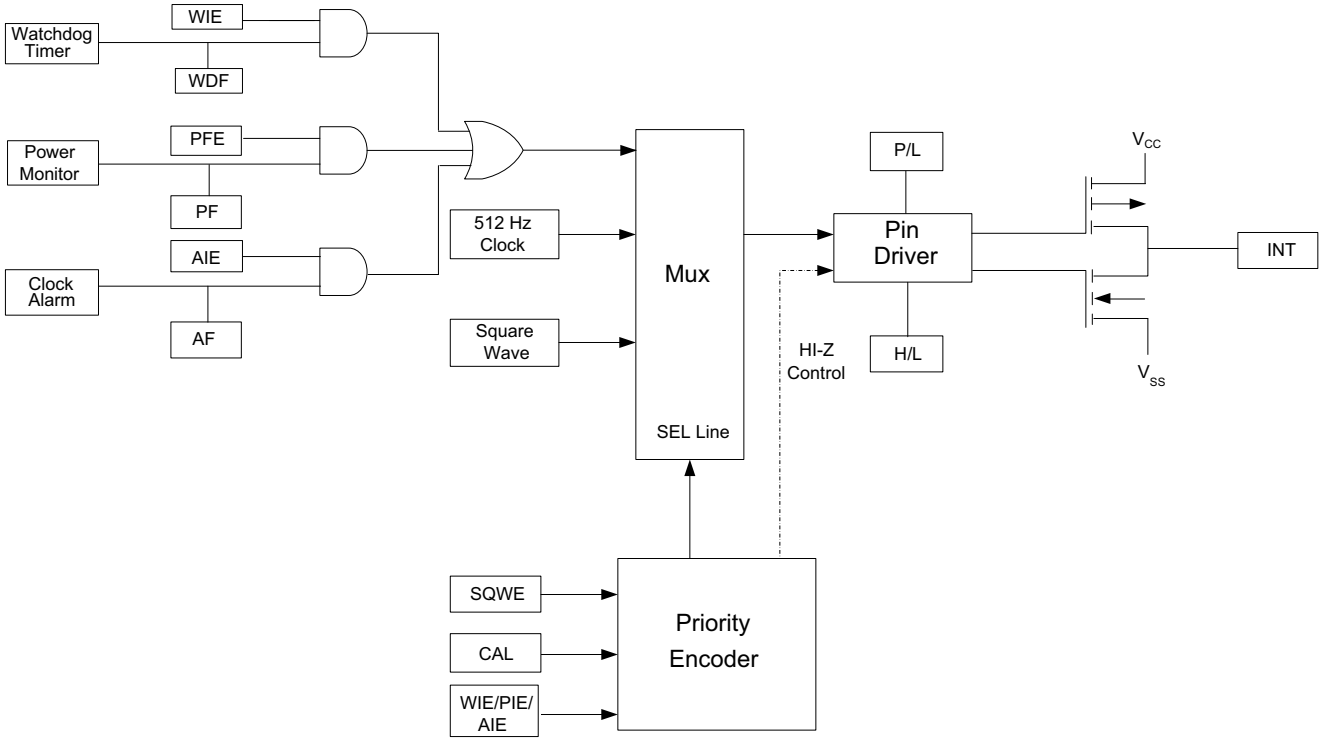
Table 5. State of the INT pin

CAL	SQWE	WIE/AIE/PFE	INT Pin Output
1	X	X	512 Hz
0	1	X	Square wave output
0	0	1	Alarm
0	0	0	HI-Z

Flags Register

The Flags register has three flag bits: WDF, AF, and PF, which can be used to generate an interrupt. They are set by the watchdog timeout, alarm match, or power fail monitor respectively. The processor can either poll this register or enable interrupts when a flag is set. These flags are automatically reset when the register is read. The flags register is automatically loaded with the value 0x00 on power-up (except for the OSCF bit. See Stopping and Starting the Oscillator on page 11).

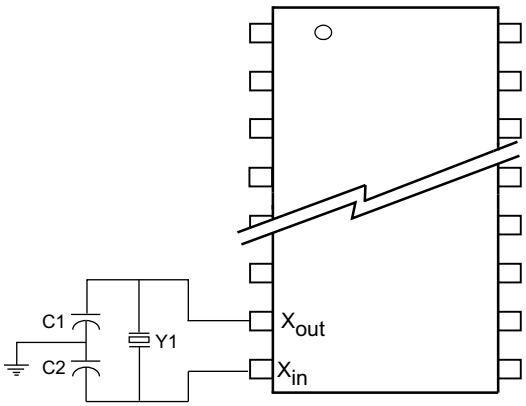
Figure 7. Interrupt Block Diagram



RTC External Components

The RTC requires connecting an external 32.768-kHz crystal and C_1, C_2 load capacitance as shown in the Figure 8. The figure shows the recommended RTC external component values. The load capacitances, C_1 and C_2, are inclusive of parasitic of the printed circuit board (PCB). The PCB parasitic includes the capacitance due to land pattern of crystal pads/pins, X_{in}/X_{out} pads, and copper traces connecting the crystal and device pins.

Figure 8. RTC Recommended Component Configuration[12]



Recommended Values

Y_1 = 32.768 kHz (12.5 pF)
C_1 = 12 pF
C_2 = 69 pF

Note The recommended values for C1 and C2 include board trace capacitance.

PCB Design Considerations for RTC

The RTC crystal oscillator is a low-current circuit with high-impedance nodes on their crystal pins. Due to the low operating current of the RTC circuit, the crystal connections are very sensitive to noise on the board. Hence, it is necessary to isolate the RTC circuit from other signals on the board.

It is also critical to minimize the stray capacitance on the PCB. Stray capacitances add to the overall crystal load capacitance and, therefore, cause oscillation frequency errors. Proper bypassing and careful layout are required to achieve the optimum RTC performance.

Layout Requirements

The board layout must adhere to (but not limited to) the following guidelines during routing RTC circuitry because they help you achieve optimum performance from the RTC design.

- Place the crystal as close as possible to the X_{in} and X_{out} pins. Keep the trace lengths between the crystal and RTC equal in length and as short as possible to reduce the probability of noise coupling.
- Keep X_{in} and X_{out} trace width below 8 mils. A wider trace width leads to larger trace capacitance. The larger these bond pads and traces are, the more likely it is that noise can couple from adjacent signals.
- Shield the X_{in} and X_{out} signals by providing a guard ring around the crystal circuitry. This guard ring prevents noise coupling from neighboring signals.
- Take care while routing any other high-speed signal in the vicinity of RTC traces. The more the crystal is isolated from other signals on the board, the less likely it is that noise is coupled into the crystal. Maintain a minimum of 200 mil separation between the $X_{in}$and X_{out} traces, and any other high speed signal on the board.
- No signals should run underneath crystal components on the same PCB layer.
- Create an isolated solid copper ground plane on the adjacent PCB layer and underneath the crystal circuitry to prevent unwanted noise coupled from traces routed on the other signal layers of the PCB. The local ground plane should be separated by at least 40 mils from the neighboring plane on the same PCB layer. The solid ground plane should only be in the vicinity of RTC components and its perimeter should be kept equal to the guard ring perimeter. The isolated ground plane should be connected to system ground. Figure 9 shows the recommended layout for the RTC circuit.

Note
12. For nonvolatile static random access memory (nvSRAM) real time clock (RTC) design guidelines and best practices, see application note AN61546.

Figure 9. Recommended Layout for RTC

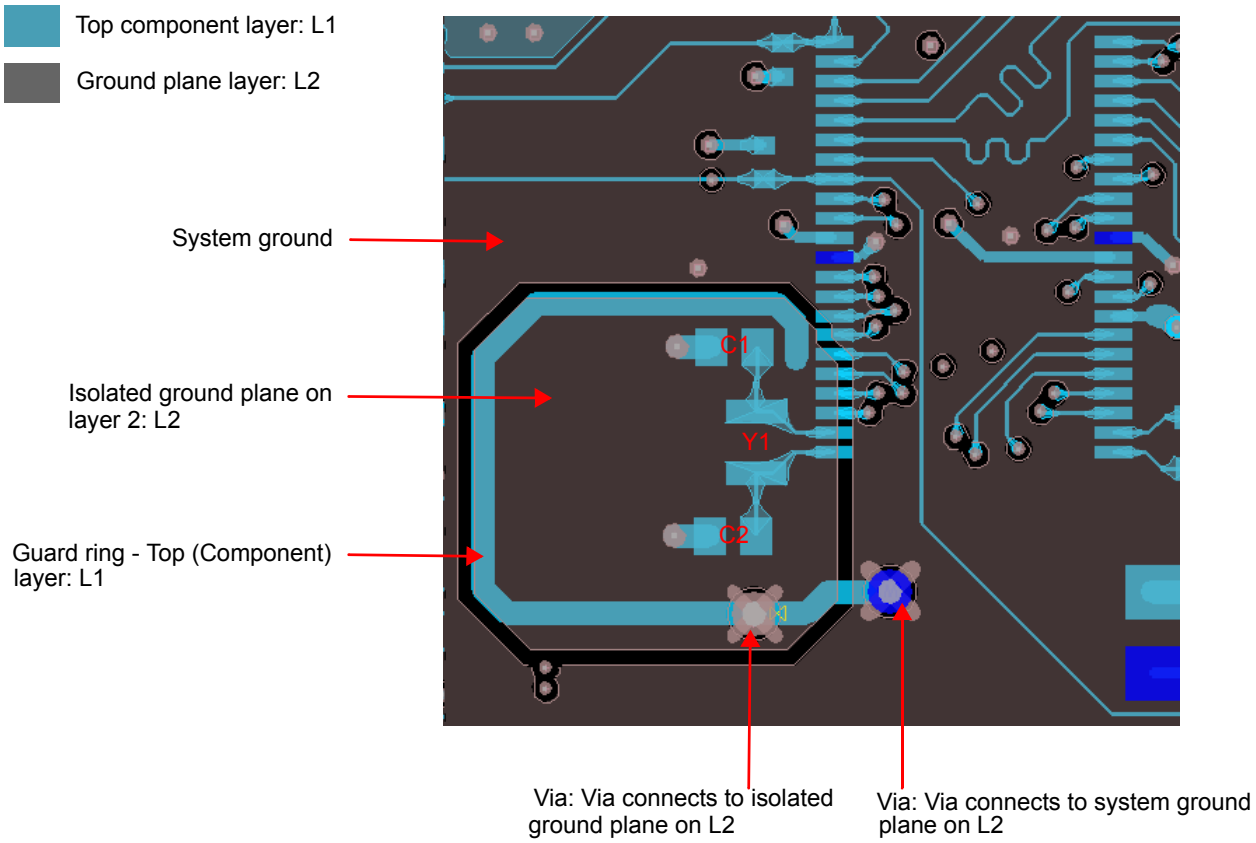


Table 6. RTC Register Map[13]

Register		BCD Format Data[14]								Function/Range
CY14B116K	CY14B116M	D7	D6	D5	D4	D3	D2	D1	D0	
0x1FFFFF	0xFFFFF	10s years				Years				Years: 00–99
0x1FFFFE	0xFFFFE	0	0	0	10s months	Months				Months: 01–12
0x1FFFFD	0xFFFFD	0	0	10s day of month		Day of month				Day of month: 01–31
0x1FFFFC	0xFFFFC	0	0	0	0	0	Day of week			Day of week: 01–07
0x1FFFFB	0xFFFFB	0	0	10s hours		Hours				Hours: 00–23
0x1FFFFA	0xFFFFA	0	10s minutes			Minutes				Minutes: 00–59
0x1FFFF9	0xFFFF9	0	10s seconds			Seconds				Seconds: 00–59
0x1FFFF8	0xFFFF8	OSCEN (0)	0	Cal sign (0)	Calibration (00000)					Calibration values[15]
0x1FFFF7	0xFFFF7	WDS (0)	WDW (0)	WDT (000000)						Watchdog timer[15]
0x1FFFF6	0xFFFF6	WIE (0)	AIE (0)	PFE (0)	SQWE (0)	H/L (1)	P/L (0)	SQ1 (0)	SQ0 (0)	Interrupts[15]
0x1FFFF5	0xFFFF5	M (1)	0	10s alarm day of month		Alarm, day of month				Alarm, day of month: 01–31
0x1FFFF4	0xFFFF4	M (1)	0	10s alarm hours		Alarm, hours				Alarm, hours: 00–23
0x1FFFF3	0xFFFF3	M (1)	10s alarm minutes			Alarm, minutes				Alarm, minutes: 00–59
0x1FFFF2	0xFFFF2	M (1)	10s alarm seconds			Alarm, seconds				Alarm, seconds: 00–59
0x1FFFF1	0xFFFF1	10s centuries				Centuries				Centuries: 00–99
0x1FFFF0	0xFFFF0	WDF	AF	PF	OSCF[16]	BPF[16]	CAL (0)	W (0)	R (0)	Flags[15]

Notes
13. Upper Byte D_{15}-D_8 (CY14B116M) of RTC registers are reserved for future use.
14. ( ) designates values shipped from the factory.
15. This is a binary value, not a BCD value.
16. When you reset OSCF and BPF flag bits, the flags register will be updated after t_{RTCp} time.

Table 7. Register Map Detail

Register		Description							
CY14B116K	CY14B116M								
0x1FFFFF	0xFFFFF	**Time Keeping - Years**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		10s years				Years			
		Contains the lower two BCD digits of the year. Lower nibble (four bits) contains the value for years; upper nibble (four bits) contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99.							
0x1FFFFE	0xFFFFE	**Time Keeping - Months**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	0	10s month	Months			
		Contains the BCD digits of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12.							
0x1FFFFD	0xFFFFD	**Time Keeping - Day of month**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	10s day of month		Day of month			
		Contains the BCD digits for the date of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the 10s digit and operates from 0 to 3. The range for the register is 1–31. Leap years are automatically adjusted for.							
0x1FFFFC	0xFFFFC	**Time Keeping - Day of week**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	0	0	0	Day of week		
		Lower nibble (three bits) contains a value that correlates to the of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, because the day is not integrated with the date.							
0x1FFFFB	0xFFFFB	**Time Keeping - Hours**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	0	10s hours		Hours			
		Contains the BCD value of hours in 24 hour format. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23.							
0x1FFFFA	0xFFFFA	**Time Keeping - Minutes**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	10s minutes			Minutes			
		Contains the BCD value of minutes. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59.							
0x1FFFF9	0xFFFF9	**Time Keeping - Seconds**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		0	10s seconds			Seconds			
		Contains the BCD value of seconds. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper digit and operates from 0 to 5. The range for the register is 0–59.							
0x1FFFF8	0xFFFF8	**Calibration/Control**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Table 7. Register Map Detail (continued)

Register		Description							
CY14B116K	CY14B116M								
		OSCEN	0	Calibration sign	Calibration				
OSCEN		Oscillator enable. When set to ‘1’, the oscillator is stopped. When set to ‘0’, the oscillator runs. Disabling the oscillator saves battery or capacitor power during storage.							
Calibration Sign		Determines if the calibration adjustment is applied as an addition (1) to or as a subtraction (0) from the time-base.							
Calibration		These five bits control the calibration of the clock.							
0x1FFFF7	0xFFFF7	**Watchdog Timer**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WDS	WDW	WDT					
WDS		Watchdog strobe. Setting this bit to ‘1’ reloads and restarts the watchdog timer. Setting the bit to ‘0’ has no effect. The bit is cleared automatically after the watchdog timer is reset. The WDS bit is write only. Reading it always returns a 0.							
WDW		Watchdog write enable. Setting this bit to ‘1’ disables any write to the watchdog timeout value (D5–D0). This allows you to set the watchdog strobe bit without disturbing the timeout value. Setting this bit to ‘0’ allows bits D5–D0 to be written to the watchdog register when the next write cycle is complete. This function is explained in more detail in Watchdog Timer on page 12.							
WDT		Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32-Hz count (31.25 ms). The range of timeout value is 31.25 ms (a setting of 01h) to 2 seconds (setting of 3Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the WDW bit was set to ‘0’ on a previous cycle. **Note** Since the Watchdog Timer uses a free-running 32-Hz (31.25 ms period) clock, the set time interval has an additional time between 0 ms and 31.25 ms.							
0x1FFFF6	0xFFFF6	**Interrupt Status/Control**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		WIE	AIE	PFE	SQWE	H/L	P/L	SQ1	SQ0
WIE		Watchdog interrupt enable. When set to ‘1’ and a watchdog timeout occurs, the watchdog timer drives the INT pin and the WDF flag. When set to ‘0’, the watchdog timeout affects only the WDF flag.							
AIE		Alarm interrupt enable. When set to ‘1’, the alarm match drives the INT pin and the AF flag. When set to ‘0’, the alarm match only affects the AF flag.							
PFE		Power fail enable. When set to ‘1’, the power fail monitor drives the INT pin and the PF flag. When set to ‘0’, the power fail monitor affects only the PF flag.							
SQWE		Square wave enable. When set to ‘1’, a square wave is driven on the INT pin with frequency programmed using SQ1 and SQ0 bits. The square wave output takes precedence over interrupt logic. If the SQWE bit is set to ‘1’. when an enabled interrupt source becomes active, only the corresponding flag is raised and the INT pin continues to drive the square wave.							
H/L		HIGH/LOW. When set to 1, the INT pin is driven active HIGH. When set to 0, the INT pin is open drain, active LOW.							
P/L		Pulse/Level. When set to ‘1’, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to ‘0’, the INT pin is driven to an active level (as set by H/L) until the flags register is read.							
SQ1, SQ0		SQ1, SQ0. These bits are used to decide the frequency of the square wave on the INT pin output when SQWE bit is set to ‘1’. The following is the frequency output for each combination of SQ1, SQ0: (0, 0) - 1 Hz (0, 1) - 512 Hz (1, 0) - 4096 Hz (1, 1) - 32768 Hz							

Table 7. Register Map Detail (continued)

Register		Description							
CY14B116K	CY14B116M								
0x1FFFF5	0xFFFF5	**Alarm - Day of month**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	0	10s alarm day of month		Alarm day of month			
		Contains the alarm value for the date of the month and the match bit to select or deselect the date value.							
M		Match. When this bit is set to '0', the date value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the date value.							
0x1FFFF4	0xFFFF4	**Alarm - Hours**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	0	10s alarm hours		Alarm hours			
		Contains the alarm value for the hours and the match bit to select or deselect the hours value.							
M		Match. When this bit is set to '0', the hours value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the hours value.							
0x1FFFF3	0xFFFF3	**Alarm - Minutes**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	10s alarm minutes			Alarm minutes			
		Contains the alarm value for the minutes and the match bit to select or deselect the minutes value.							
M		Match. When this bit is set to '0', the minutes value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the minutes value.							
0x1FFFF2	0xFFFF2	**Alarm - Seconds**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		M	10s alarm seconds			Alarm seconds			
		Contains the alarm value for the seconds and the match bit to select or deselect the second's value.							
M		Match. When this bit is set to '0', the seconds value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the seconds value.							
0x1FFFF1	0xFFFF1	**Time Keeping - Centuries**							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
		10s centuries				Centuries			
		Contains the BCD value of centuries. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 9. The range for the register is 0-99 centuries.							

Table 7. Register Map Detail (continued)

Register		Description							
CY14B116K	CY14B116M								
0x1FFFF0	0xFFFF0	Flags							
		D7	D6	D5	D4	D3	D2	D1	D0
		WDF	AF	PF	OSCF	BPF	CAL	W	R
WDF		Watchdog timer flag. This read-only bit is set to '1' when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags register is read or on power-up							
AF		Alarm flag. This read-only bit is set to '1' when the time and date match the values stored in the alarm registers with the match bits = 0. It is cleared when the Flags register is read or on power-up.							
PF		Power fail flag. This read-only bit is set to '1' when power falls below the power fail threshold V_{SWITCH}. It is cleared when the Flags register is read.							
OSCF		Oscillator fail flag. Set to '1' on power-up if the oscillator is enabled and not running in the first 5 ms of operation. This indicates that RTC backup power failed and clock value is no longer valid. This bit survives the power cycle and is never cleared internally by the chip. The user must check for this condition and write 0 to clear this flag. When user resets OSCF flag bit, the bit will be updated after t_{RTCp} time.							
BPF		Backup power fail flag. Set to '1' on power-up if the backup power (battery or capacitor) failed. The backup power fail condition is determined by the voltage falling below their respective minimum specified voltage. BPF can hold the data only till a defined low level of the back up voltage (V_{DR}). User must reset this bit to clear this flag. When user resets BPF flag bit, the bit will be updated after t_{RTCp} time.							
CAL		Calibration mode. When set to '1', a 512-Hz square wave is output on the INT pin. When set to '0', the INT pin resumes normal operation. This bit takes priority over SQ0/SQ1 and other functions. This bit defaults to 0 (disabled) on power-up.							
W		Write enable: Setting the 'W' bit to '1' freezes updates of the RTC registers. You can then write to RTC registers, alarm registers, calibration register, interrupt register and flags register. Setting the 'W' bit to '0' causes the contents of the RTC registers to be transferred to the time keeping counters if the time has changed. This transfer process takes t_{RTCp} time to complete. This bit defaults to 0 on power-up.							
R		Read enable: Setting 'R' bit to '1', stops clock updates to user RTC registers so that clock updates are not seen during the reading process. Set 'R' bit to '0' to resume clock updates to the holding register. Setting this bit does not require 'W' bit to be set to '1'. This bit defaults to 0 on power-up.							

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature ..... 1000 h

At 85 °C ambient temperature..... ..... 20 Years

Maximum junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS} .....–0.5 V to +4.1 V

Voltage applied to outputs in high-Z state.....–0.5 V to V_{CC} + 0.5 V

Input voltage .....–0.5 V to Vcc + 0.5 V

Transient voltage (<20 ns) on any pin to ground potential .....–2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... .1.0 W

Surface mount lead soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 140 mA

Operating Range

Product	Range	Ambient Temperature (T_A)	V_{CC}
CY14B116K/ CY14B116M	Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ[17]	Max	Unit
V_{CC}	Power supply			2.7	3.0	3.6	V
I_{CC1}	Average V_{CC} current	Values obtained without output loads (I_{OUT} = 0 mA)	t_{RC} = 25 ns	–	–	95	mA
			t_{RC} = 45 ns	–	–	75	mA
ICC2	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = V_{CC}(Max). Average current for duration t_{STORE}		–	–	10	mA
I_{CC3}	Average V_{CC} current at t_{RC} = 200 ns, V_{CC}(Typ), 25 °C	All inputs cycling at CMOS Levels. Values obtained without output loads (I_{OUT} = 0 mA).		–	50	–	mA
I_{CC4}[18]	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}		–	–	6	mA
I_{SB}	V_{CC} standby current	$\overline{CE}$ ≥ (V_{CC} – 0.2 V). V_{IN} ≤ 0.2 V or ≥ (V_{CC} – 0.2 V). 'W' and 'R' bit set to '0'. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	t_{RC} = 25 ns	–	–	750	µA
			t_{RC} = 45 ns	–	–	600	µA
I_{ZZ}	Sleep mode current	All inputs are static at CMOS Level; RTC running on backup power supply.		–	–	10	µA
I_{IX}[19]	Input leakage current (except $\overline{HSB}$)	V_{CC} = V_{CC}(Max), V_{SS} ≤ V_{IN} ≤ V_{CC}		–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)	V_{CC} = V_{CC}(Max), V_{SS} ≤ V_{IN} ≤ V_{CC}		–100	–	+1	µA
I_{OZ}	Off state output leakage current	V_{CC} = V_{CC}(Max), V_{SS} ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ or $\overline{OE}$ ≥ V_{IH} or $\overline{BLE}$/$\overline{BHE}$ ≥ V_{IH} or $\overline{WE}$ ≤ V_{IL}		–1	–	+1	µA

Notes

17. Typical values are at 25 °C, V_{CC} = V_{CC}(Typ). Not 100% tested.
18. This parameter is only guaranteed by design and is not tested.
19. The $\overline{HSB}$ pin has I_{OUT} = -2 uA for V_{OH} of 2.4 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ[17]	Max	Unit
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V
V_{CAP}[20]	Storage capacitor	Between V_{CAP} pin and V_{SS}	19.8	22.0	82.0	µF
V_{VCAP}[21, 22]	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} = V_{CC} (max)	–	–	5.0	V

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000,000	Cycles

Capacitance

In the following table, the capacitance parameters are listed. [22]

Parameter	Description	Test Conditions	Max (All packages except 165-FBGA)	Max (165-FBGA package)	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC} (Typ)	8	10	pF
C_{IO}	Input/Output capacitance		8	10	pF
C_{OUT}	Output capacitance		8	10	pF

Thermal Resistance

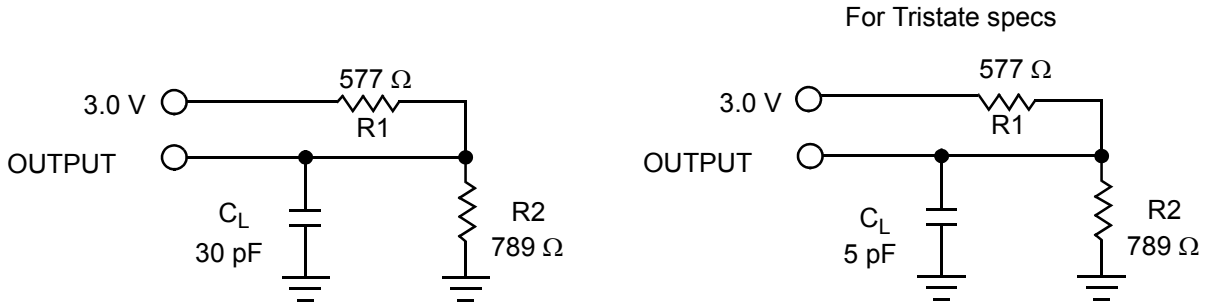
In the following table, the thermal resistance parameters are listed.[22]

Parameter	Description	Test Conditions	44-TSOP II	54-TSOP II	165-FBGA	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	44.6	41.1	15.6	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		2.4	4.6	2.9	°C/W

Notes

20. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore, it is always recommended to use a capacitor within the specified min and max limits.
21. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage
22. These parameters are only guaranteed by design and are not tested.

Figure 10. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels.....0 V to 3 V

Input rise and fall times (10% - 90%)..... ≤ 3 ns

Input and output timing reference levels..... 1.5 V

RTC Characteristics

Over the Operating Range

Parameters	Description		Min	Typ[23]	Max	Units
V_{RTCbat}	RTC battery pin voltage		1.8	3.0	3.6	V
I_{BAK}[24]	RTC backup current	T_A = –40 °C	–	–	0.45	µA
		T_A = 25 °C	–	0.45	–	µA
		T_A = 85 °C	–	–	0.60	µA
V_{RTCcap}[25]	RTC capacitor pin voltage	T_A = –40 °C	1.6	–	3.6	V
		T_A = 25 °C	1.5	3.0	3.6	V
		T_A = 85 °C	1.4	–	3.6	V
$V_{BAKFAIL}$	Backup failure threshold		1.8	–	2.2	V
V_{DR}	BPF flag retention voltage		1.6	–	-	V
tOCS	RTC oscillator time to start		–	1	2	sec
t_{RTCp}	RTC processing time from end of ‘W’ bit set to ‘0’		–	–	1	ms
R_{BKCHG}	RTC backup capacitor charge current-limiting resistor		350	–	850	Ω

Notes

23. Typical values are at 25 °C, V_{CC} = V_{CC}(Typ). Not 100% tested.
24. From either V_{RTCcap} or V_{RTCbat}.
25. If V_{RTCcap} > 0.5 V or if no capacitor is connected to V_{RTCcap} pin, the oscillator starts in tOCS time. If a backup capacitor is connected and V_{RTCcap} < 0.5 V, the capacitor must be allowed to charge to 0.5 V for oscillator to start.

AC Switching Characteristics

Over the Operating Range[26]

Parameters		Description	25 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{ACE}	t_{ACS}	Chip enable access time	–	25	–	45	ns
t_{RC} [27]	t_{RC}	Read cycle time	25	–	45	-	ns
t_{AA} [28]	t_{AA}	Address access time	–	25	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	12	–	20	ns
t_{OHA} [28]	t_{OH}	Output hold after address change	3	–	3	–	ns
t_{LZCE} [29]	t_{LZ}	Chip enable to output active	3	–	3	–	ns
t_{HZCE} [29, 30]	t_{HZ}	Chip disable to output inactive	–	10	–	15	ns
t_{LZOE} [29]	t_{OLZ}	Output enable to output active	0	–	0	–	ns
t_{HZOE} [29, 30]	t_{OHZ}	Output disable to output inactive	–	10	–	15	ns
t_{PU} [29]	t_{PA}	Chip enable to power active	0	–	0	–	ns
t_{PD} [29]	t_{PS}	Chip disable to power standby	–	25	–	45	ns
t_{DBE}		Byte enable to data valid	–	12	–	20	ns
t_{LZBE} [29]		Byte enable to output active	0	–	0	–	ns
t_{HZBE} [29, 30]		Byte disable to output inactive	–	10	–	15	ns
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	25	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	20	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	20	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	10	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	20	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	ns
t_{HZWE} [29, 30, 31]	t_{WZ}	Write enable to output disable	–	10	–	15	ns
t_{LZWE} [29]	t_{OW}	Output active after end of write	3	–	3	–	ns
t_{BW}		Byte enable to end of write	20	–	30	–	ns

Notes

26. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC}(Typ), and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as shown in Figure 10 on page 24.
27. $\overline{WE}$ must be HIGH during SRAM read cycles.
28. Device is continuously selected with $\overline{CE}$, $\overline{OE}$ and $\overline{BLE}$, $\overline{BHE}$ LOW.
29. These parameters are only guaranteed by design and are not tested.
30. t_{HZCE}, t_{HZOE}, t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF. Transition is measured ±200 mV from the steady state output voltage.
31. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.

Figure 11. SRAM Read Cycle 1: Address Controlled[32, 33, 34]

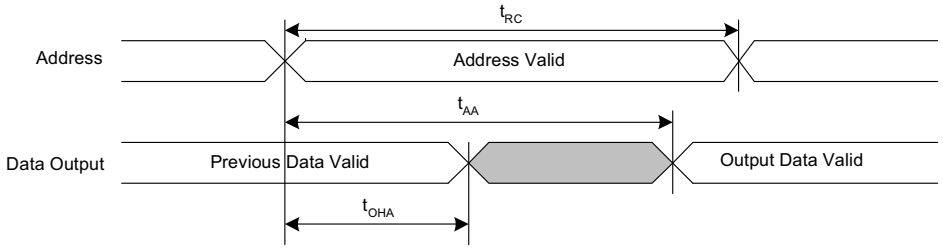
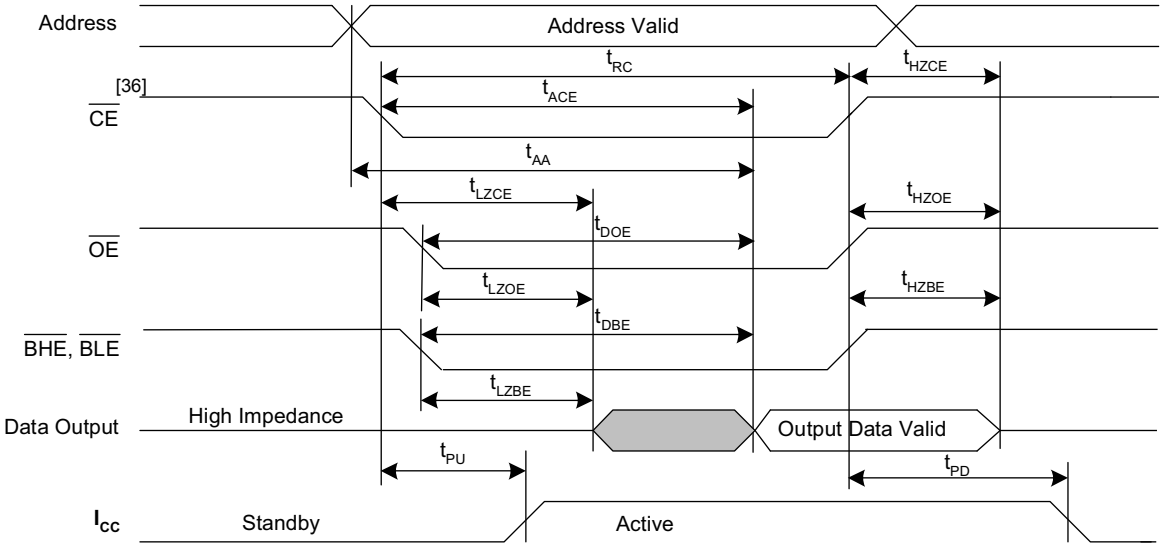


Figure 12. SRAM Read Cycle 2: $\overline{CE}$ and $\overline{OE}$ Controlled[32, 34, 35]



Notes

32. $\overline{WE}$ must be HIGH during SRAM read cycles.
33. Device is continuously selected with $\overline{CE}$, $\overline{OE}$ and $\overline{BLE}$, $\overline{BHE}$ LOW.
34. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
35. $\overline{BLE}$, $\overline{BHE}$ are applicable for x16 configuration only.
36. TSOP II package is offered in single $\overline{CE}$ and BGA package is offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE_1}$ and CE_2 such that when $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE_1}$ and CE_2 for the dual chip enable device).

Figure 13. SRAM Write Cycle 1: $\overline{WE}$ Controlled[37, 38, 39, 40]

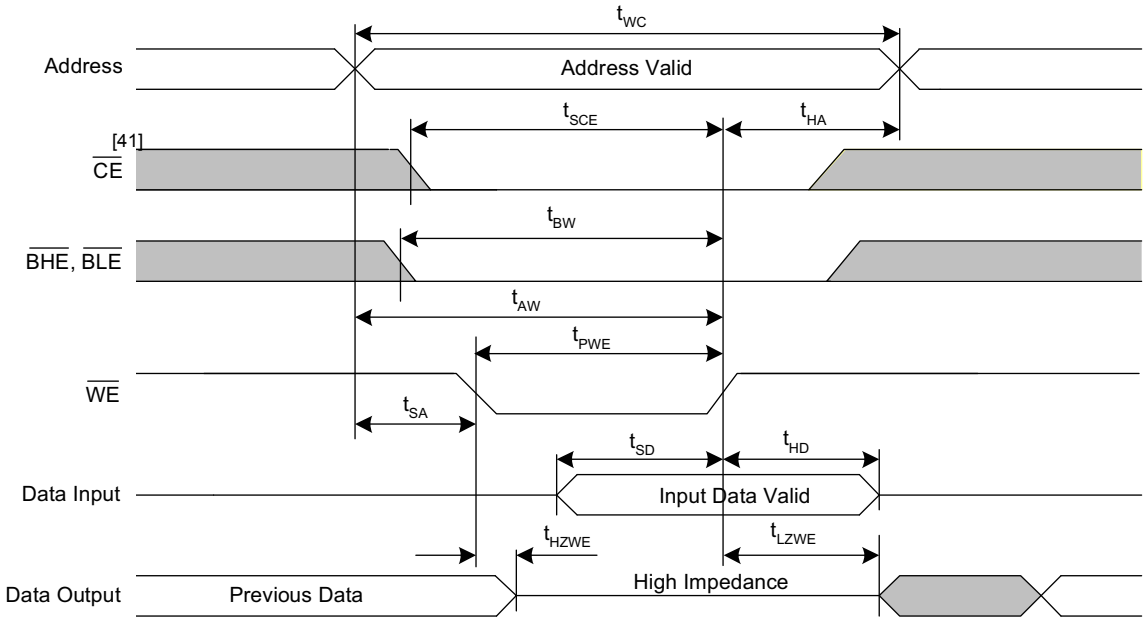
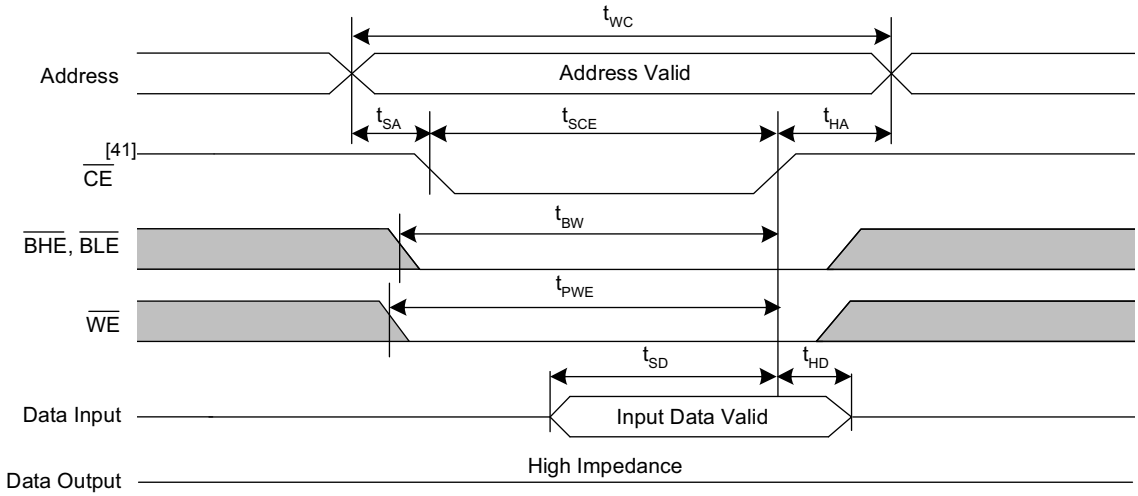


Figure 14. RAM Write Cycle 2: $\overline{CE}$ Controlled[37, 38, 39, 40]



Notes
37. BLE, BHE are applicable for x16 configuration only.
38. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.
39. HSB must remain HIGH during Read and Write cycles.
40. CE or WE must be $\geq V_{IH}$ during address transitions.
41. TSOP II package is offered in single CE and BGA package is offered in dual CE options. In this datasheet, for a dual CE device, CE refers to the internal logical combination of CE_1 and CE_2 such that when CE_1 is LOW and CE_2 is HIGH, CE is LOW. For all other cases CE is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins (CE for the single chip enable device; CE_1 and CE_2 for the dual chip enable device).

Figure 15. SRAM Write Cycle 2: $\overline{CE}$ Controlled[42, 43, 44, 45]

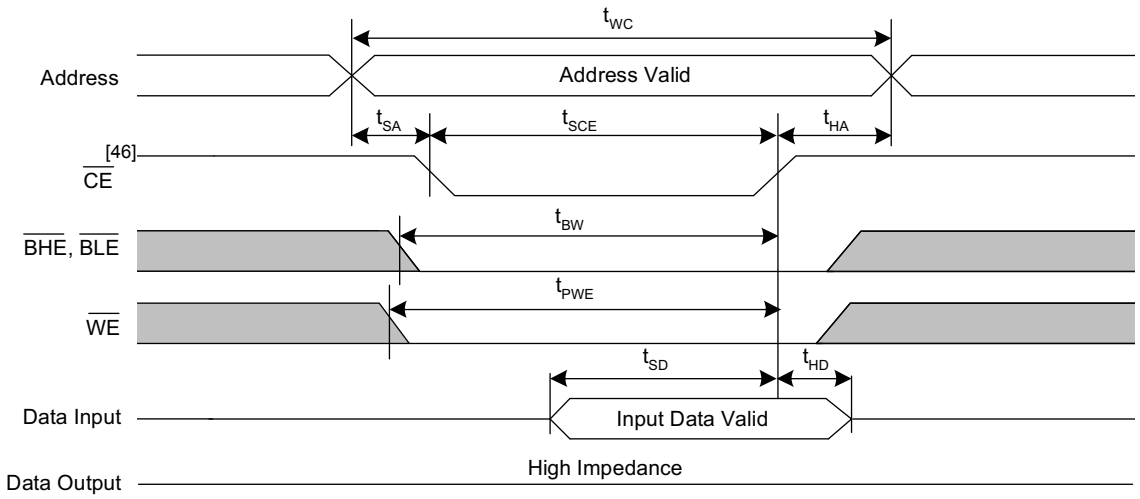
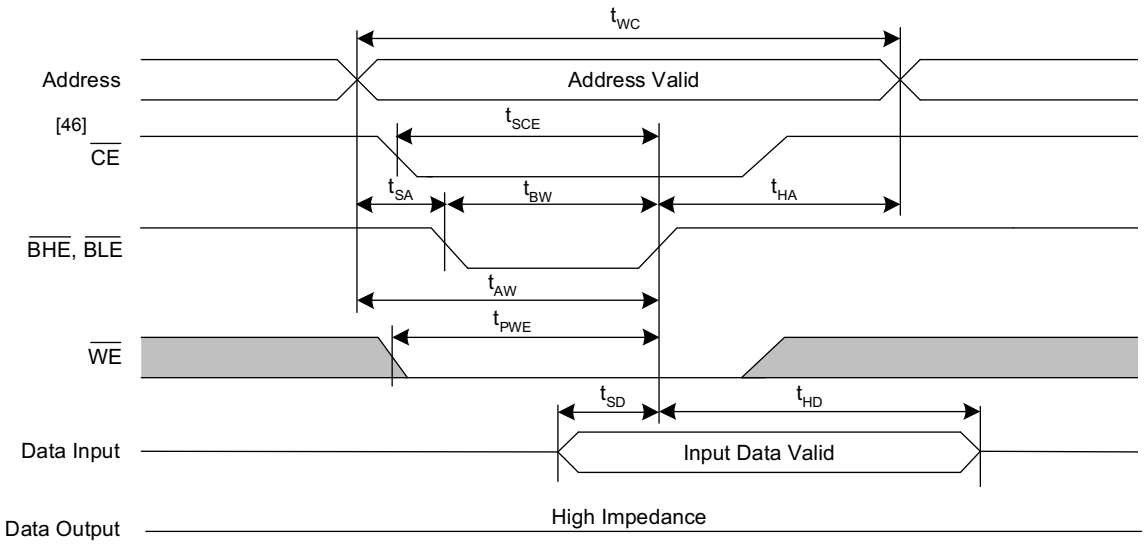


Figure 16. SRAM Write Cycle 3: $\overline{BHE}$, $\overline{BLE}$ Controlled[42, 43, 44, 45, 47]

(Not applicable for RTC register writes)



Notes

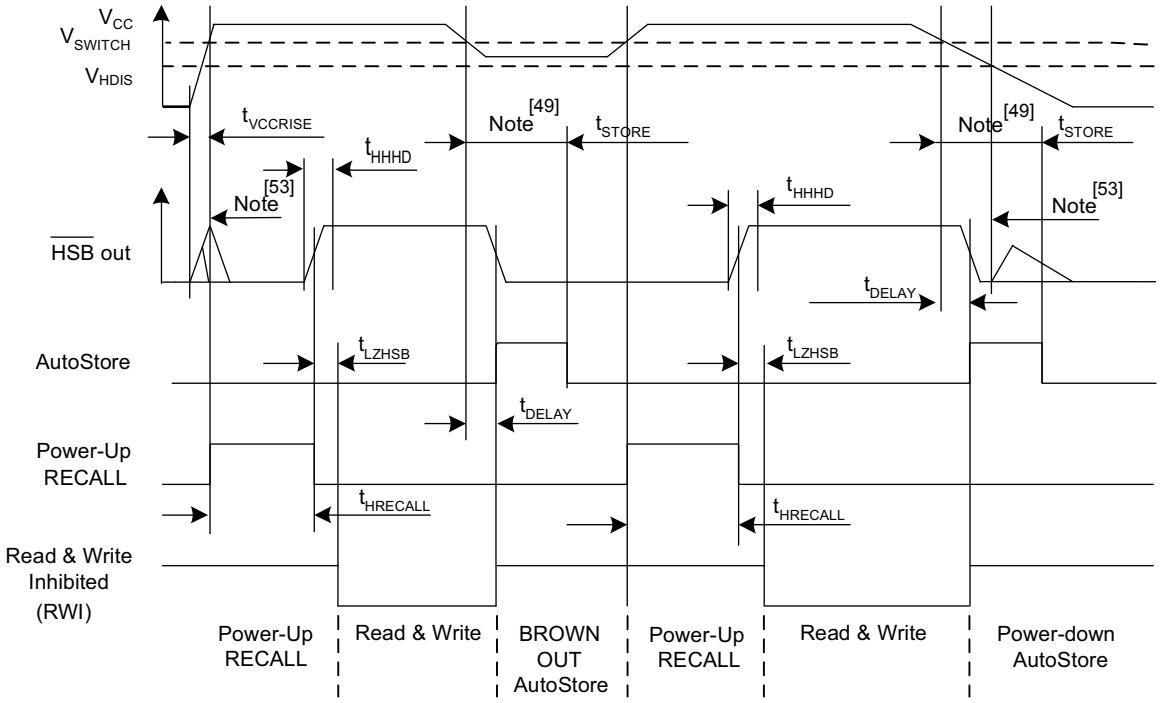
42. $\overline{BLE}$, $\overline{BHE}$ are applicable for x16 configuration only.
43. If $\overline{WE}$ is LOW when $\overline{CE}$ goes LOW, the outputs remain in the high impedance state.
44. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
45. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.
46. TSOP II package is offered in single $\overline{CE}$ and BGA package is offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).
47. Only $\overline{CE}$ and $\overline{WE}$ controlled writes to RTC registers are allowed. $\overline{BLE}$ pin must be held LOW before $\overline{CE}$ or $\overline{WE}$ pin goes LOW for writes to RTC register.

AutoStore/Power-Up RECALL Characteristics

Over the Operating Range

Parameter	Description	CY14B116K/CY14B116M		Unit
		Min	Max	
$t_{HRECALL}$ [48]	Power-Up RECALL duration	–	30	ms
t_{STORE} [49]	STORE cycle duration	–	8	ms
t_{DELAY} [50, 51]	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	2.65	V
$t_{VCCRISE}$ [51]	V_{CC} rise time	150	–	µs
V_{HDIS} [51]	$\overline{HSB}$ output disable voltage	–	1.9	V
t_{LZHSB} [51]	$\overline{HSB}$ to output active time	–	5	µs
t_{HHHD} [51]	$\overline{HSB}$ HIGH active time	–	500	ns

Figure 17. AutoStore or Power-Up RECALL[52]



Notes

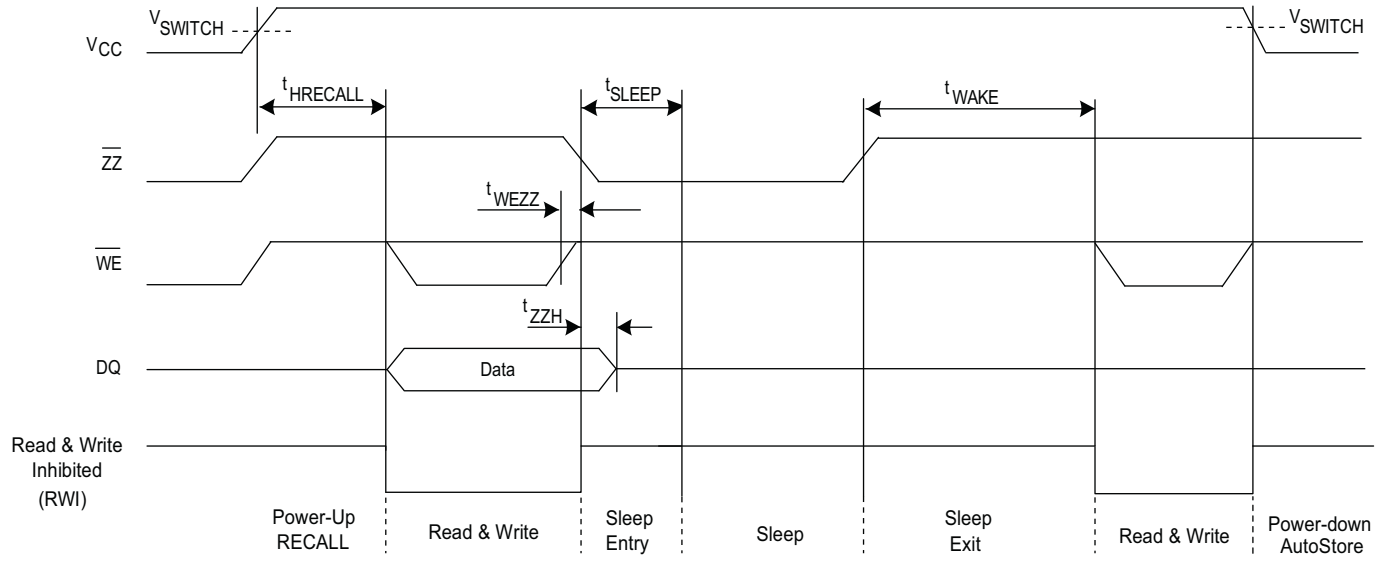
48. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
49. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
50. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
51. These parameters are only guaranteed by design and are not tested.
52. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
53. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Sleep Mode Characteristics

Over the Operating Range

Parameter	Description	CY14B116K/CY14B116M		Unit
		Min	Max	
t_{WAKE}	Sleep mode exit time ($\overline{ZZ}$ HIGH to first access after wakeup)	–	30	ms
t_{SLEEP}	Sleep mode enter time ($\overline{ZZ}$ LOW to $\overline{CE}$ don't care)	–	8	ms
t_{ZZL}	$\overline{ZZ}$ active LOW time	50	–	ns
t_{WEZZ}	Last write to Sleep mode entry time	0	–	µs
t_{ZZH}	$\overline{ZZ}$ active to DQ Hi-Z time	–	70	ns

Figure 18. Sleep Mode[54]



Note
54. Device initiates sleep routine and enters into Sleep mode after t_{SLEEP} duration.

Software Controlled STORE and RECALL Characteristics

Over the Operating Range[55, 56]

Parameter	Description	25 ns		45 ns		Unit
		Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	25	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	ns
t_{CW}	Clock pulse width	20	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	600	–	600	µs
t_{SS} [57, 58]	Soft sequence processing time	–	500	–	500	µs

Figure 19. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE and RECALL Cycle[56]

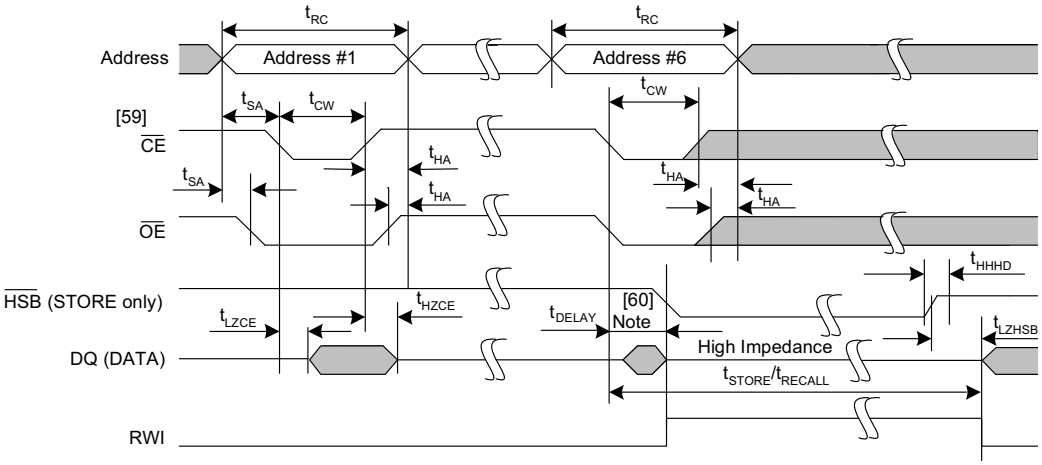
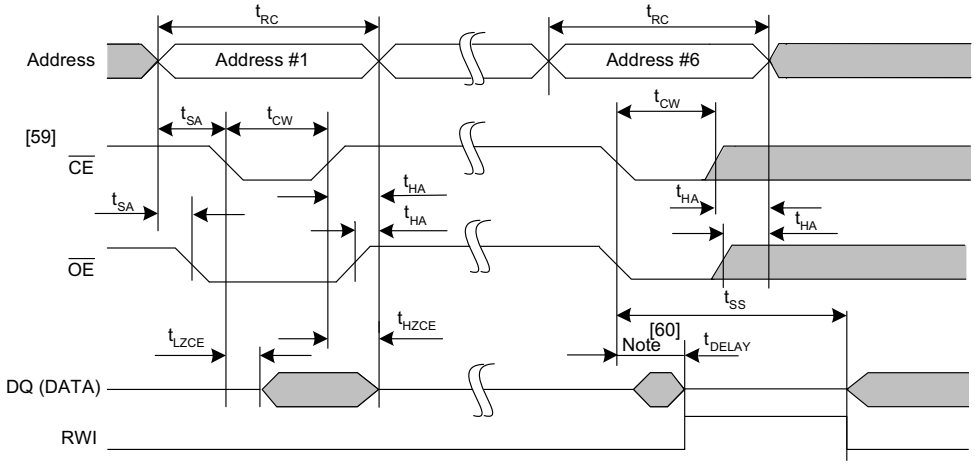


Figure 20. AutoStore Enable and Disable Cycle



Notes

55. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
56. The six consecutive addresses must be read in the order listed in Table 2. $\overline{WE}$ must be HIGH during all six consecutive cycles.
57. This is the amount of time it takes to take action on a soft sequence command. V_{CC} power must remain high to effectively register command.
58. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
59. TSOP II package is offered in single $\overline{CE}$ and BGA package is offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).
60. DQ output data at the sixth read may be invalid since the output is disabled at t_{DELAY} time.

Hardware STORE Characteristics

Over the Operating Range

Parameter	Description	CY14B116K/CY14B116M		Unit
		Min	Max	
t_{DHSB}	$\overline{HSB}$ to output active time when write latch not set	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Figure 21. Hardware STORE Cycle[61]

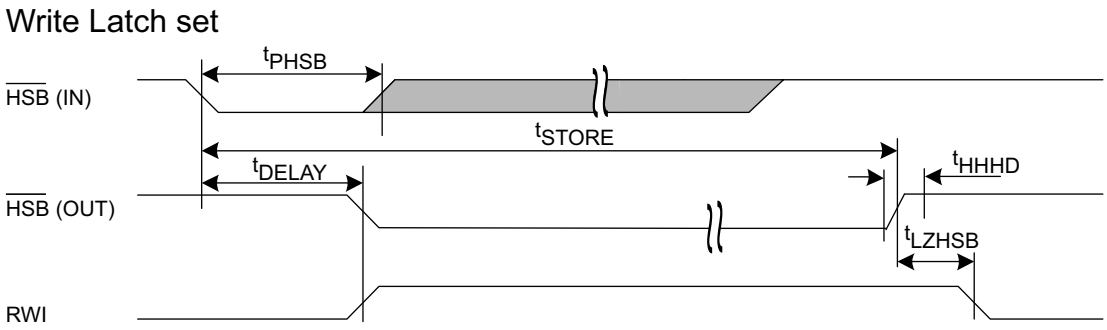
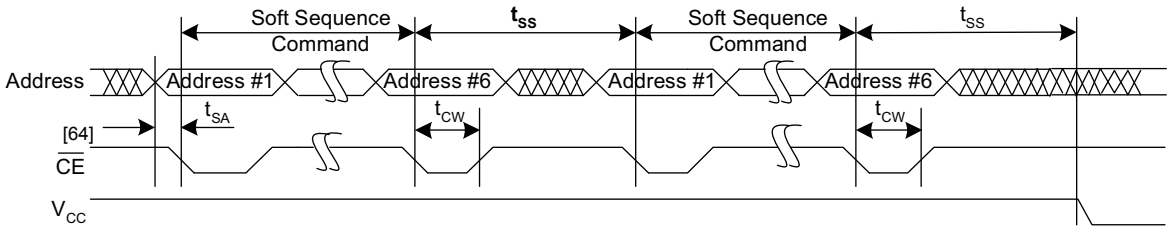


Figure 22. Soft Sequence Processing[62, 63]



Notes

61. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
62. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain high to effectively register a command.
63. Commands such as STORE and RECALL lock out I/O until the operation is complete, which further increases this time. See the specific command.
64. The TSOP II package is offered in single $\overline{CE}$ and BGA package is offered in dual $\overline{CE}$ options. In this datasheet, for a dual $\overline{CE}$ device, $\overline{CE}$ refers to the internal logical combination of $\overline{CE}_1$ and CE_2 such that when $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW. For all other cases $\overline{CE}$ is HIGH. Intermediate voltage levels are not permitted on any of the chip enable pins ($\overline{CE}$ for the single chip enable device; $\overline{CE}_1$ and CE_2 for the dual chip enable device).

Truth Table For SRAM Operations

$\overline{HSB}$ should remain HIGH for SRAM Operations.

For ×8 Configuration

Single chip enable option (44-pin TSOP II package)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs and Outputs	Mode	Power
H	X	X	High-Z	Deselect/Power-down	Standby
L	H	L	Data out (DQ_0–DQ_7);	Read	Active
L	H	H	High-Z	Output disabled	Active
L	L	X	Data in (DQ_0–DQ_7);	Write	Active

For ×16 Configuration

Single chip enable option (54-pin TSOP II package)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}$	$\overline{BHE}$	Inputs and Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	X	X	H	H	High-Z	Output disabled	Active
L	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	L	L	H	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Read	Active
L	H	L	H	L	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Read	Active
L	H	H	X	X	High-Z	Output disabled	Active
L	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	L	X	L	H	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Write	Active
L	L	X	H	L	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Write	Active

For ×16 Configuration

Dual chip enable option (165-ball FBGA package)

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BLE}$	$\overline{BHE}$	Inputs and Outputs	Mode	Power
H	X	X	X	X	X	High-Z	Deselect/Power-down	Standby
X	L	X	X	X	X	High-Z	Deselect/Power-down	Standby
L	H	X	X	H	H	High-Z	Output disabled	Active
L	H	H	L	L	L	Data out (DQ_0–DQ_{15})	Read	Active
L	H	H	L	L	H	Data out (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Read	Active
L	H	H	L	H	L	Data out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Read	Active
L	H	H	H	X	X	High-Z	Output disabled	Active
L	H	L	X	L	L	Data in (DQ_0–DQ_{15})	Write	Active
L	H	L	X	L	H	Data in (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Write	Active
L	H	L	X	H	L	Data in (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Write	Active

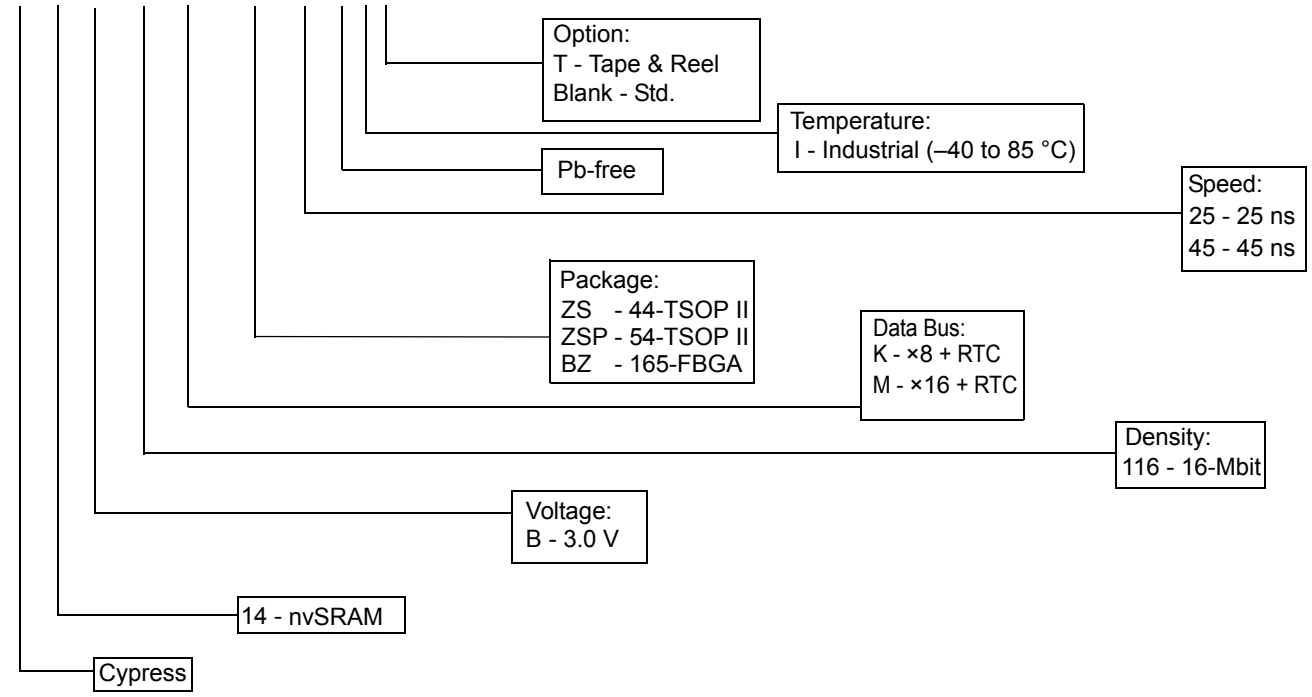
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B116K-ZS25XI	51-85087	44-pin TSOP II	Industrial
	CY14B116K-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B116M-ZSP25XI	51-85160	54-pin TSOP II	
45	CY14B116K-ZS45XI	51-85087	44-pin TSOP II	
	CY14B116K-ZS45XIT	51-85087	44-pin TSOP II	
	CY14B116M-BZ45XI	51-85195	165-ball FBGA	

All parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

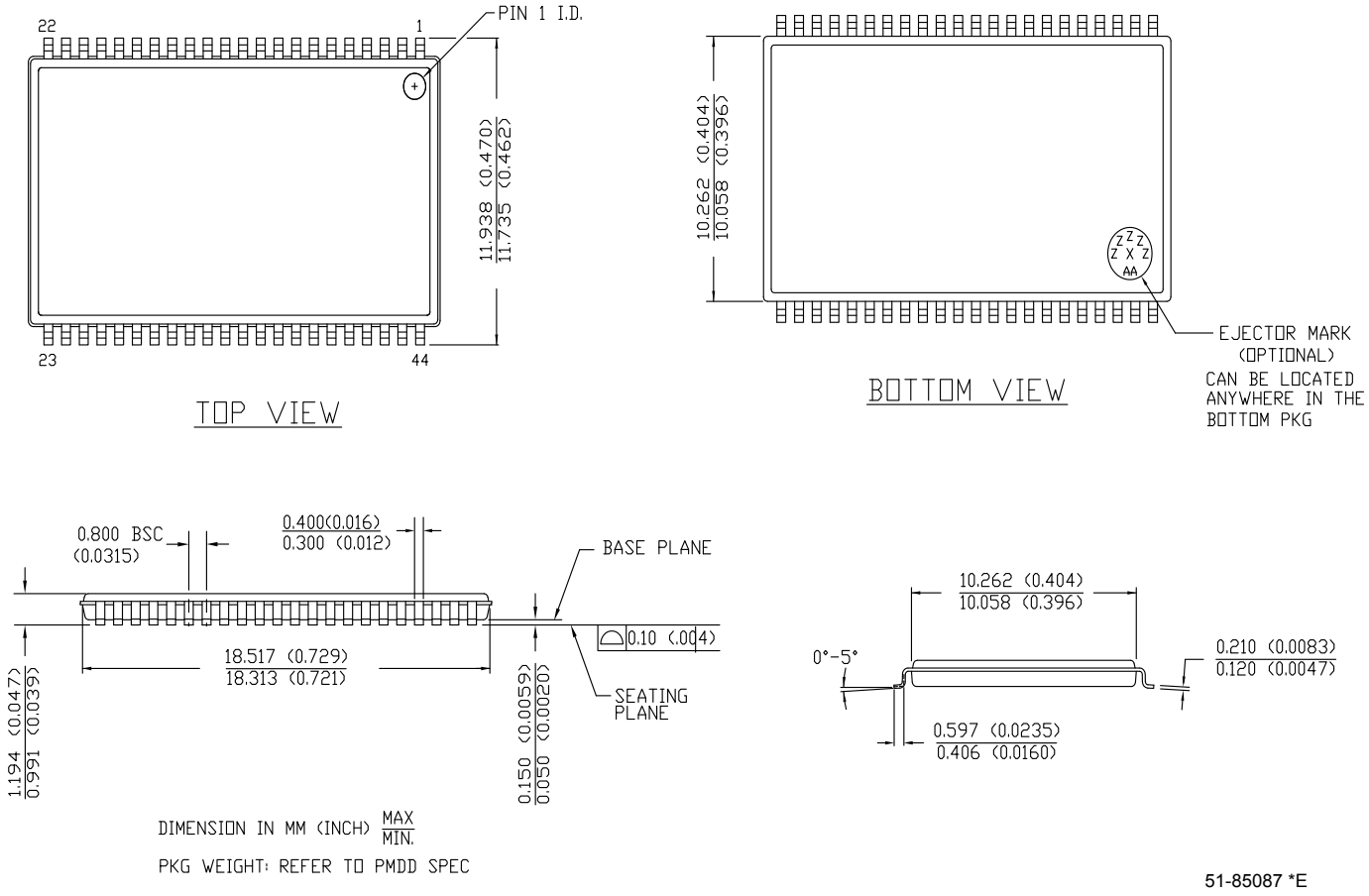
Ordering Code Definition

CY14 B 116 K - ZS 25 X I T



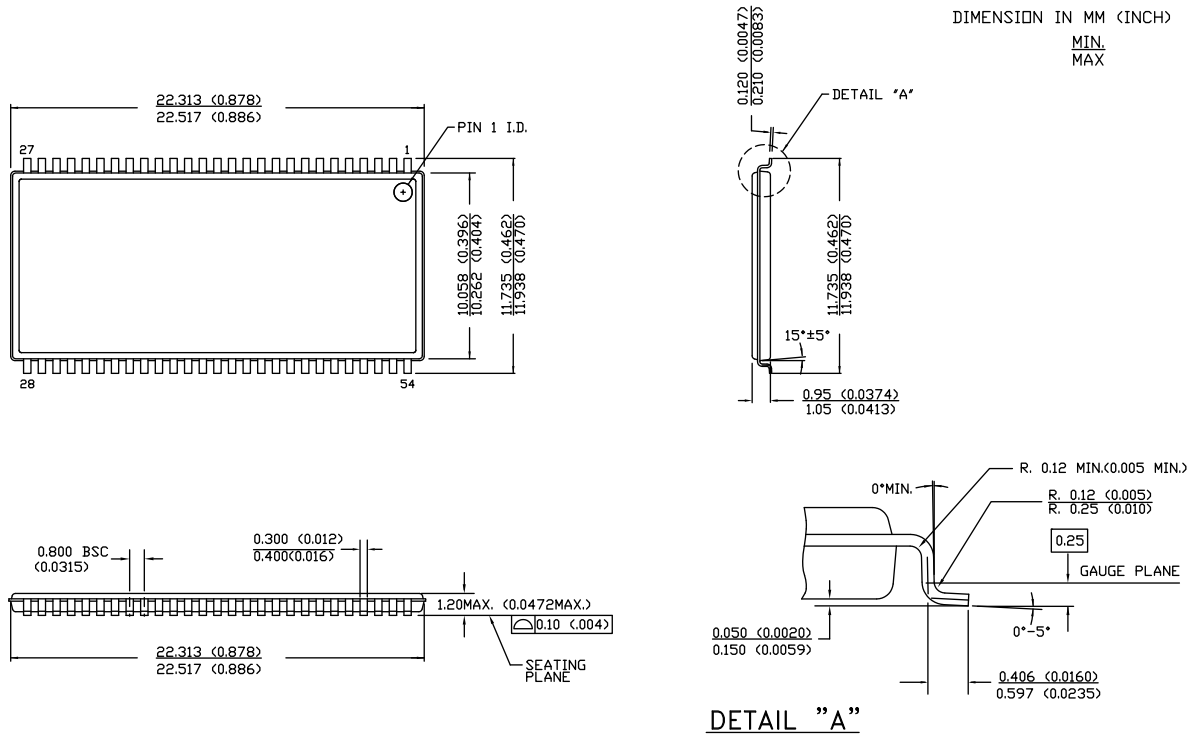
Package Diagrams

Figure 23. 44-Pin TSOP II Package Outline (51-85087)



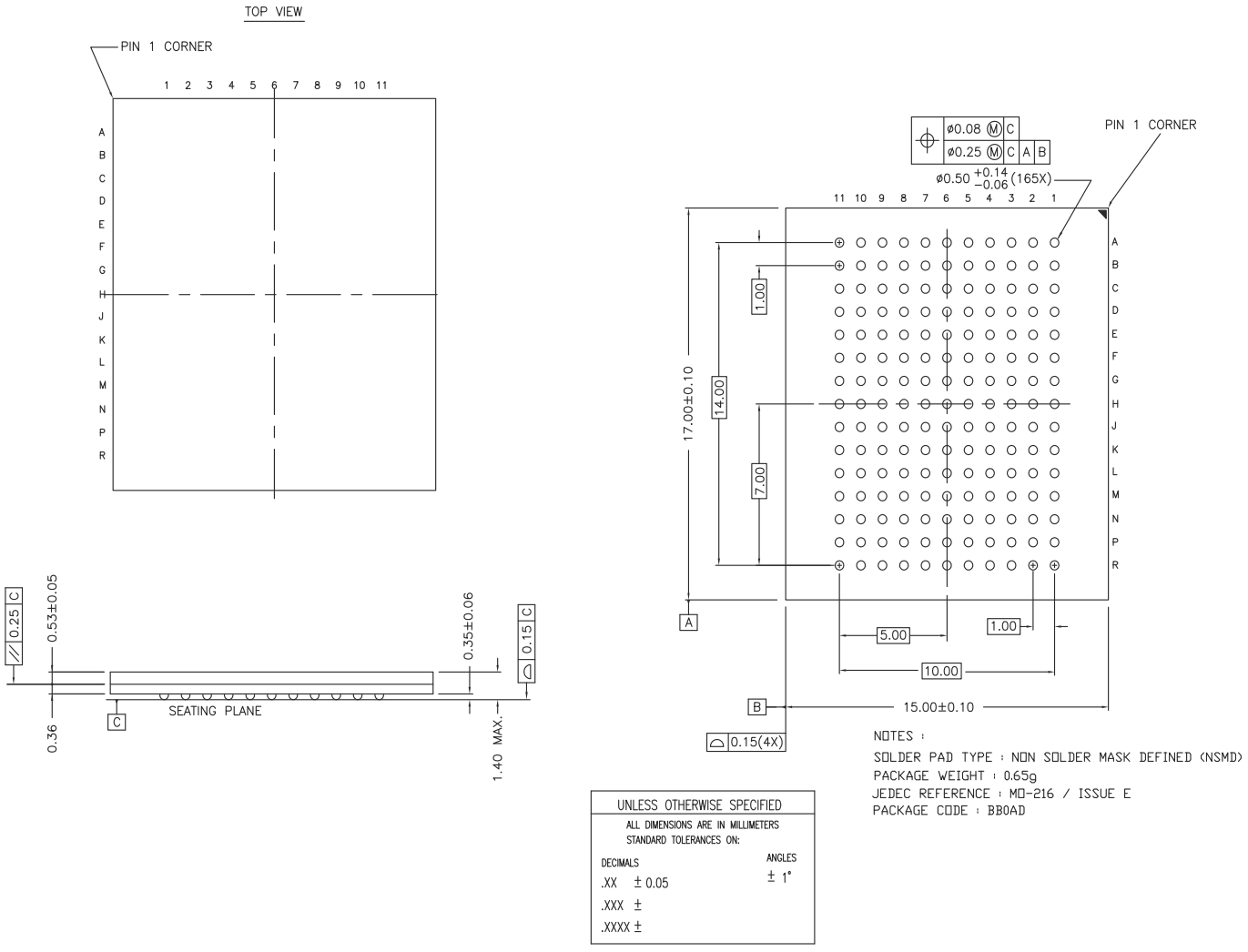
Package Diagrams (continued)

Figure 24. 54-Pin TSOP II Package Outline (51-85160)



Package Diagrams (continued)

Figure 25. 165-ball FBGA (15 mm × 17 mm × 1.40 mm) Package Outline (51-85195)



51-85195 *C

Acronyms

Acronym	Description
BCD	Binary coded decimal
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JESD	JEDEC Standards
nvSRAM	nonvolatile Static Random Access Memory
RoHS	Restriction of Hazardous Substances
RTC	Real time clock
RWI	Read and Write Inhibited
TSOP II	Thin Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
Kbit	kilobit
kHz	kilohertz
kΩ	kilohm
µA	microampere
mA	milliampere
µF	microfarad
Mbit	megabit
MHz	megahertz
µs	microsecond
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

All errata for this product are fixed, effective date code 1431 (YY=14, WW=31). For more information, refer to datasheet 001-67786 Rev. *G or contact Cypress Technical Support at http://www.cypress.com/support.

Document History Page

Document Title: CY14B116K/CY14B116M, 16-Mbit (2048 K × 8/1024 K × 16) nvSRAM with Real Time Clock Document Number: 001-67786				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3188189	GVCH	03/04/2011	New datasheet
*A	3457528	GVCH	12/13/2011	Datasheet status changed from “Advance” to “Preliminary” Pin Diagrams: Updated Figure 3 and Figure 3 Table 1: Updated $\overline{ZZ}$ pin description Added footnote 7 and 13 I_{CC1} parameter spec value changed from 70 mA to 95 mA and 50 mA to 75 mA for 25 ns and 45 ns access speed respectively. I_{CC3} parameter spec value changed from 35 mA to 50 mA I_{CC4} parameter spec value changed from 10 mA to 6 mA I_{SB} parameter spec value changed from 500 uA to 750 uA Added V_{CAP} value for CY14C116X Changed V_{CAP} typ value from 27 uF to 22 uF Added Thermal Resistance values Added footnote 20 and 32 RTC Characteristics: Updated I_{BAK} and V_{RTCcap} parameter spec values Changed $t_{HRECALL}$ parameter spec value from 40 ms to 60 ms for CY14C116X and from 20 ms to 30 ms for CY14B116X/CY14E116X. Changed t_{WAKE} parameter spec value from 40 ms to 60 ms for CY14C116X and from 20 ms to 30 ms for CY14B116X/CY14E116X. t_{RECALL} spec value changed from 300 us to 600 us t_{SS} spec value changed from 200 us to 500 us Updated Ordering Information Package Diagrams: Updated 165-FBGA package diagram
*B	3514357	ZSK	02/07/2012	No technical updates.
*C	3944873	GVCH	03/26/2013	Removed 2.5 V and 5 V operating range voltage support Removed ×32 configuration support Added 54 - pin TSOP II package Added Figure 5 (Sleep Mode (ZZ) Flow Diagram) Updated Real Time Clock Operation description Updated Maximum Ratings (Changed “Ambient temperature with power applied” to “Maximum junction temperature”). Changed C_{IN} and C_{OUT} value from 7 pF to 8 pF Changed V_{IH} max spec value from V_{CC} + 0.3 V to V_{CC} + 0.5 V Added V_{VCAP} parameter spec Added footnote 21 Changed $V_{BAKFAIL}$ spec max value from 2.0 V to 2.2 V Changed T_{RTCp} max value from 350 µs to 1 ms. Updated t_{ZZL} parameter spec value from 15 ns to 50 ns Added Figure 18 Added footnote 54

Document History Page (continued)

Document Title: CY14B116K/CY14B116M, 16-Mbit (2048 K × 8/1024 K × 16) nvSRAM with Real Time Clock Document Number: 001-67786				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	4260504	GVCH	01/24/2014	Modified Logic Block Diagram for more clarity. Updated AutoStore Operation (Power-Down): Removed sentence “The HSB signal is monitored by the system to detect if an AutoStore cycle is in progress.” Modified Figure 5 for more clarity. Added note in Watchdog Timer and Table 7 (Watchdog Timer section) to clarify additional delay at the start of countdown. Added PCB Design Considerations for RTC Added I_{SB} max spec value for 45 ns access speed Changed V_{CAP} min spec value from 20 µF to 19.8 µF Added thermal resistance values for 54-TSOP II package Added footnote 30 Updated Figure 18 for more clarity Changed t_{ZZH} max spec value from 20 ns to 70 ns.
*E	4366689	GVCH	05/01/2014	Updated Sleep Mode: Updated description. Updated Thermal Resistance values Added Note 17 and 30. Added . Updated in new template.
*F	4417851	GVCH	06/24/2014	DC Electrical Characteristics: Added R bit set to ‘0’ to I_{SB} test condition Added footnote 18 Updated maximum value of V_{VCAP} parameter from 4.5 V to 5.0 V Capacitance: Updated C_{IN} and C_{OUT}value from 8 pF to 10 pF for 165-FBGA package Added C_{IO} parameter.
*G	4432183	GVCH	07/07/2014	DC Electrical Characteristics: Updated maximum value of V_{CAP} parameter from 120.0 µF to 82.0 µF
*H	4456803	ZSK	07/31/2014	Removed Errata section. Added a note at the end of the document mentioning when the errata items were fixed.
*I	4562106	GVCH	11/05/2014	Added related documentation hyperlink in page 1. Updated package diagram 51-85160 to current revision
*J	4616093	GVCH	01/07/2015	Changed datasheet status from Preliminary to Final.

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