19-4256; Rev 0; 8/10

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

General Description

The MAX3697A/MAX3698A are low-jitter precision clock generators optimized for network applications. The devices integrate a crystal oscillator and a phase-locked loop (PLL) to generate high-frequency clock outputs for Ethernet applications.

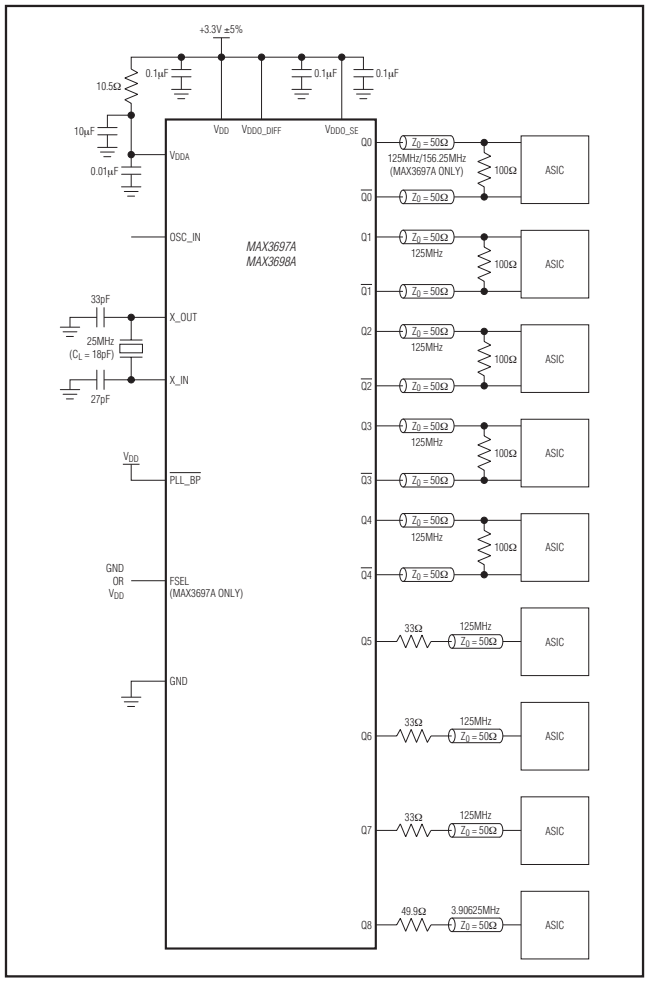
This proprietary PLL design features ultra-low jitter (0.4psRMS) and excellent power-supply noise rejection (PSNR), minimizing design risk for network equipment.

The MAX3697A/MAX3698A contain five LVDS outputs and four LVCMOS outputs. The MAX3697A has a selectable output feature on channel Q0 that allows selection between 125MHz or 156.25MHz.

Applications

Ethernet Networking Equipment

Typical Operating Circuit



Features

- **Crystal Oscillator Interface: 25MHz**
- **OSC_IN Interface:**
  - **PLL Enabled: 25MHz**
  - **PLL Disabled: 20MHz to 320MHz**
- **Outputs:**
  - **MAX3698A (Five LVDS Outputs at 125MHz)**
  - **MAX3697A (Four LVDS Outputs at 125MHz, One LVDS Output at 125MHz/156.25MHz)**
  - **Three LVCMOS Outputs at 125MHz**
  - **One LVCMOS Output at 3.90625MHz**
- **Low Phase Jitter: 0.4ps$_{RMS}$ (12kHz to 20MHz)**
- **PSNR: -57dBc at 100kHz Offset**
- **Operating Temperature Range: -40°C to +85°C**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3697AETJ+	-40°C to +85°C	32 TQFN-EP*
MAX3698AETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range at V_{DD}, V_{DDA}, V_{DDO_SE}, V_{DDO_DIFF} ..... -0.3V to +4.0V
Voltage Range at Q0, $\overline{Q0}$, Q1, $\overline{Q1}$, Q2, $\overline{Q2}$, Q3, $\overline{Q3}$, Q4, $\overline{Q4}$, Q5, Q6, Q7, Q8, $\overline{PLL\_BP}$, FSEL, OSC_IN ..... -0.3V to (V_{DD} + 0.3V)
Voltage at X_IN Pin ..... -0.3V to +1.2V
Voltage at X_OUT Pin ..... -0.3V to (V_{DD} - 0.6V)
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) 2759mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. When using X_IN, X_OUT, input no signal is applied at OSC_IN. When PLL is enabled, $\overline{PLL\_BP}$ = high-Z or high. When PLL is bypassed, $\overline{PLL\_BP}$ = low.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current (Note 2)	I_{DD}	PLL enabled		175	224	mA
		PLL bypassed		160		
LVDS OUTPUTS (Q0, $\overline{Q0}$, Q1, $\overline{Q1}$, Q2, $\overline{Q2}$, Q3, $\overline{Q3}$, Q4, $\overline{Q4}$ Pins)						
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage Amplitude	$\lvert V_{OD} \rvert$	Figure 1	250		400	mV
Change in Magnitude of Differential Output for Complementary States	$\Delta\lvert V_{OD} \rvert$				25	mV
Output Offset Voltage	V_{OS}		1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\lvert V_{OS} \rvert$				25	mV
Differential Output Impedance			80	105	140	Ω
Output Current		Shorted together		5		mA
		Short to ground (Note 3)		8		
Clock Output Rise/Fall Time	t_r, t_f	20% to 80%, R_L = 100Ω	90	180	330	ps
Output Duty-Cycle Distortion		PLL enabled	48	50	52	%
		PLL bypassed (Note 4)	46	50	54	
LVCMOS/LVTTL OUTPUTS (Q5, Q6, Q7, Q8 Pins)						
Q8 Output High Voltage	V_{OH}	I_{OH} = -2mA	2.4	2.7	3.3	V
Q8 Output Low Voltage	V_{OL}	I_{OL} = 2mA			0.4	V
Q5, Q6, Q7 Output High Voltage	V_{OH}	I_{OH} = -12mA	2.6		V_{DD}	V
Q5, Q6, Q7 Output Low Voltage	V_{OL}	I_{OL} = 12mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. When using X_IN, X_OUT, input no signal is applied at OSC_IN. When PLL is enabled, $\overline{PLL\_BP}$ = high-Z or high. When PLL is bypassed, $\overline{PLL\_BP}$ = low.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Q5, Q6, Q7 Output Rise/Fall Time	t_r, t_f	20% to 80% at 125MHz (Note 5)	0.15	0.5	0.8	ns
Q8 Output Rise/Fall Time	t_r, t_f	20% to 80% at 3.90625MHz (Note 5)		4.0	6.1	ns
Output Duty-Cycle Distortion		PLL enabled	45	50	55	%
		PLL bypassed (Note 4)	43	50	57	
Output Impedance	R_{OUT}			15		Ω
INPUT SPECIFICATIONS (FSEL, $\overline{PLL\_BP}$ Pins)						
Input-Voltage High	V_{IH}		2.0		V_{DD}	V
Input-Voltage Low	V_{IL}		0		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			82	µA
Input Low Current	I_{IL}	V_{IN} = 0	-80			µA
LVCMOS/LVTTL INPUT SPECIFICATIONS (OSC_IN) (Note 6)						
Input Clock Frequency		PLL enabled		25		MHz
		PLL bypassed	20		320	
Input Amplitude Range		(Note 7)	1.2		3.6	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			80	µA
Input Low Current	I_{IL}	V_{IN} = 0	80			µA
Reference Clock Duty Cycle			40	50	60	%
Input Capacitance	C_{IN}			1.5		pF
CLOCK OUTPUT AC SPECIFICATIONS						
VCO Center Frequency				625		MHz
Output Frequency with PLL Enabled for MAX3697A		FSEL = GND (Q0)		125		MHz
		FSEL = V_{DD} (Q0)		156.25		
		Q1 to Q7		125		
		Q8 output		3.90625		
Output Frequency with PLL Enabled for MAX3698A		Q0 to Q7		125		MHz
		Q8		3.90625		
Output Frequency with PLL Disabled		LVDS outputs	20		320	MHz
		LVCMOS outputs Q5, Q6, Q7	20		160	
Integrated Phase Jitter at 125MHz/156.25MHz	RJ_{RMS}	12kHz to 20MHz, $\overline{PLL\_BP}$ = high (Note 8)		0.4		ps_{RMS}
		12kHz to 20MHz, $\overline{PLL\_BP}$ = high-Z (Note 9)		0.4		
Power-Supply Noise Rejection (Note 10)		LVDS output		-57		dBc
		LVCMOS output		-47		
Deterministic Jitter Due to Supply Noise (Note 11)		LVDS output		7		ps_{P-P}
		LVCMOS output		23		
Nonharmonic and Subharmonic Spurs (Note 12)		MAX3697A		-73		dBc
		MAX3698A		-87		

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. When using X_IN, X_OUT, input no signal is applied at OSC_IN. When PLL is enabled, $\overline{PLL\_BP}$ = high-Z or high. When PLL is bypassed, $\overline{PLL\_BP}$ = low.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS Clock Output SSB Phase Noise at 125MHz (Note 13)		f = 100Hz		-114		dBc/Hz
		f = 1kHz		-124		
		f = 10kHz		-127		
		f = 100kHz		-131		
		f = 1MHz		-144		
		f > 10MHz		-149		
LVCMOS Clock Output SSB Phase Noise at 125MHz (Note 13)		f = 100Hz		-113		dBc/Hz
		f = 1kHz		-124		
		f = 10kHz		-126		
		f = 100kHz		-130		
		f = 1MHz		-144		
		f > 10MHz		-151		

Note 1: A series resistor of up to 10.5Ω is allowed between V_{DD} and V_{DDA} for filtering supply noise when system power-supply tolerance is V_{DD} = 3.3V ±5%. See Figure 5.
Note 2: All outputs unloaded.
Note 3: The current when an LVDS output is shorted to ground is the steady-state current after the detection circuitry has settled. It is expected that the LVDS output short to ground condition is short-term only.
Note 4: Measured with OSC_IN input with 50% duty cycle.
Note 5: Q5, Q6, and Q7 measured with a series resistor of 33Ω to a load capacitance of 3.0pF. Q8 is measured with a series resistor of 50Ω to a load capacitance of 15pF. See Figure 2.
Note 6: The OSC_IN input can be DC- or AC-coupled.
Note 7: Must be within the absolute maximum rating of V_{DD} + 0.3V.
Note 8: Measured with 25MHz crystal (with OSC_IN left open).
Note 9: Measured with 25MHz signal applied to OSC_IN.
Note 10: Measured at 125MHz output with 40mV_{P-P} sinusoidal signal on the supply at 100kHz. Measured with network in Figure 5.
Note 11: Parameter calculated based on PSNR.
Note 12: Measurement includes XTAL oscillator feedthrough, crosstalk, intermodulation spurs, etc.
Note 13: Measured with 25MHz XTAL oscillator.

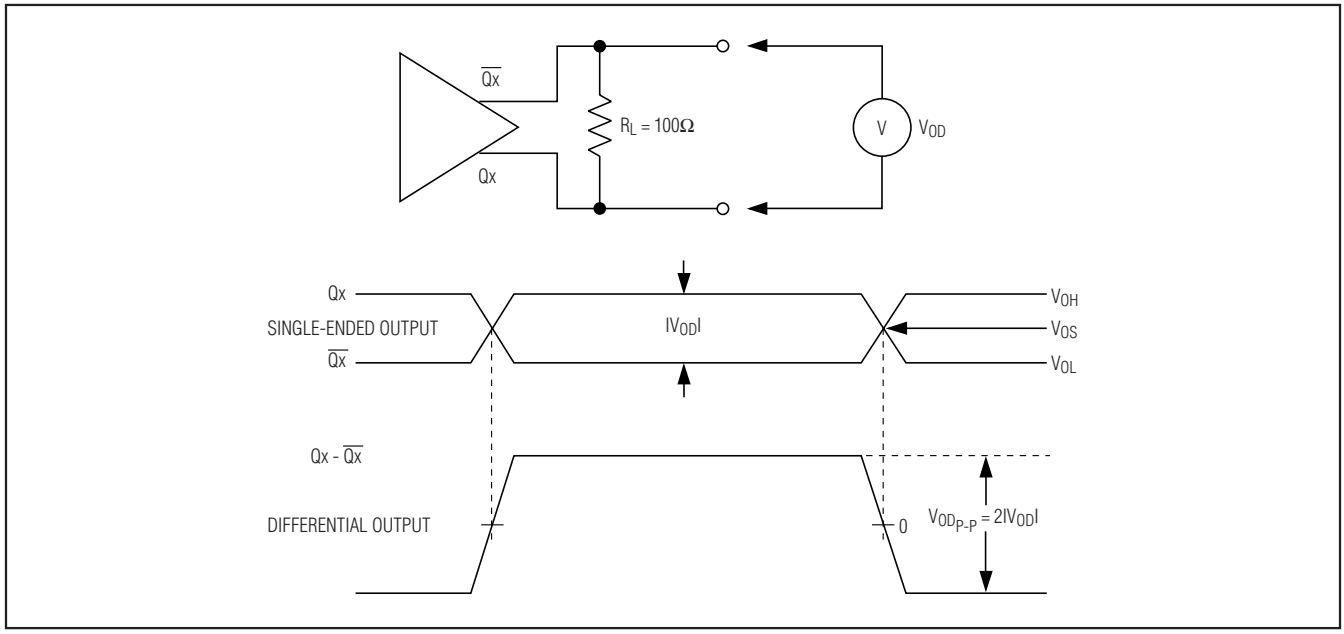


Figure 1. Driver Output Levels

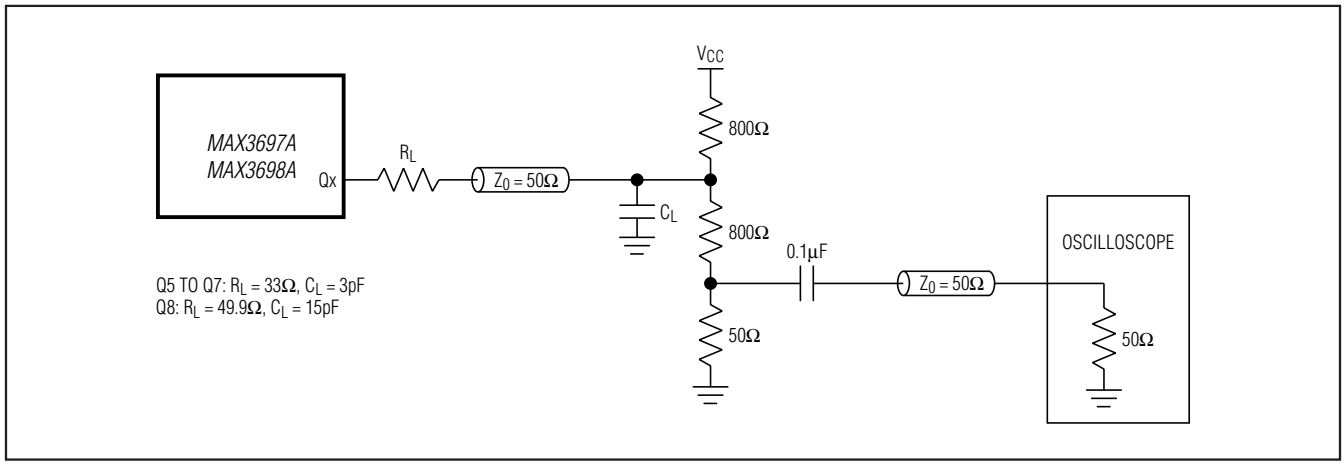


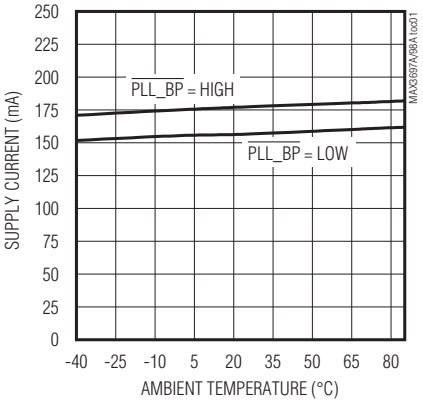
Figure 2. LVCMOS Output Measurement Setup

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

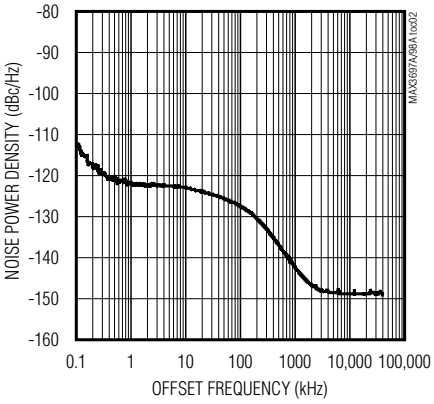
Typical Operating Characteristics

(Typical values are at V_{DD} = +3.3V, T_A = +25°C, crystal frequency = 25MHz.)

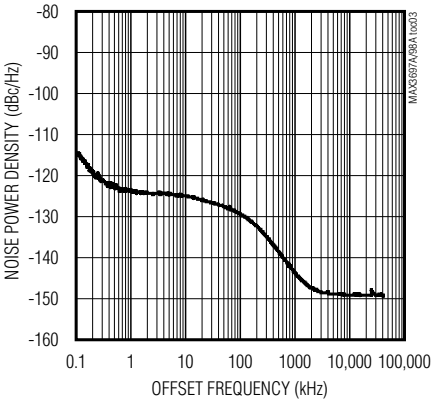
SUPPLY CURRENT vs. TEMPERATURE



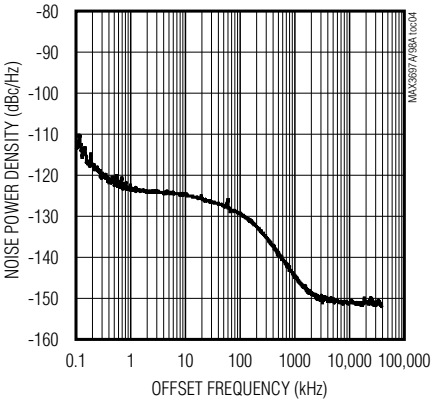
PHASE NOISE AT 156MHz CLOCK FREQUENCY (Q0)



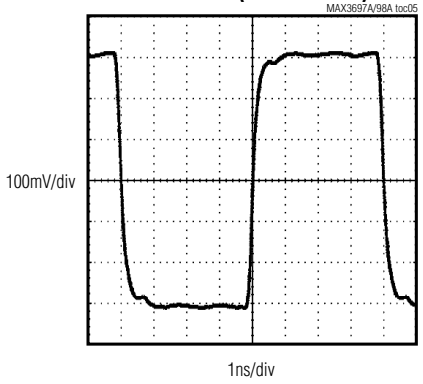
PHASE NOISE AT 125MHz CLOCK FREQUENCY (Q4)



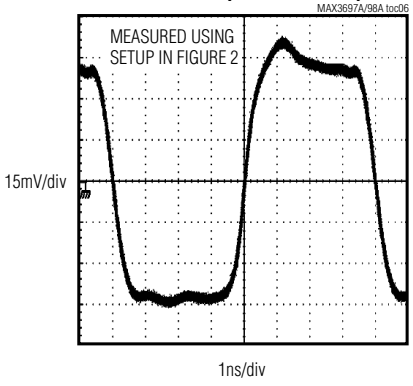
PHASE NOISE AT 125MHz CLOCK FREQUENCY (Q7)



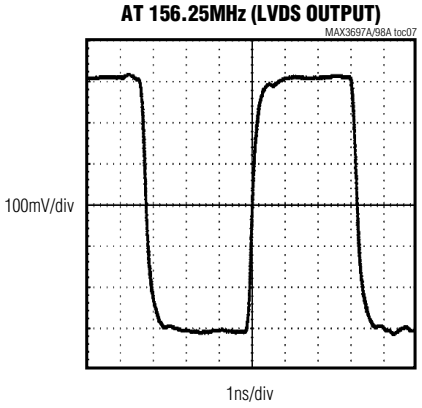
DIFFERENTIAL OUTPUT WAVEFORM AT 125MHz (LVDS OUTPUT)



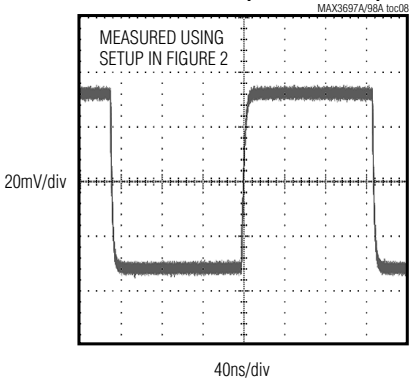
OUTPUT WAVEFORM AT 125MHz (CMOS OUTPUT)



DIFFERENTIAL OUTPUT WAVEFORM AT 156.25MHz (LVDS OUTPUT)



OUTPUT WAVEFORM AT 3.90625MHz (CMOS OUTPUT)

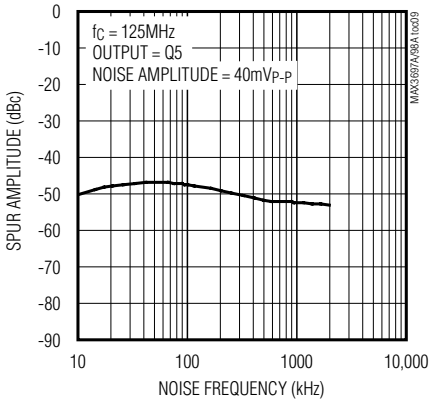


+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

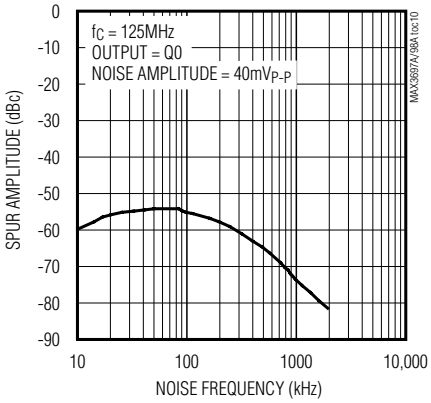
Typical Operating Characteristics (continued)

(Typical values are at V_{DD} = +3.3V, T_A = +25°C, crystal frequency = 25MHz.)

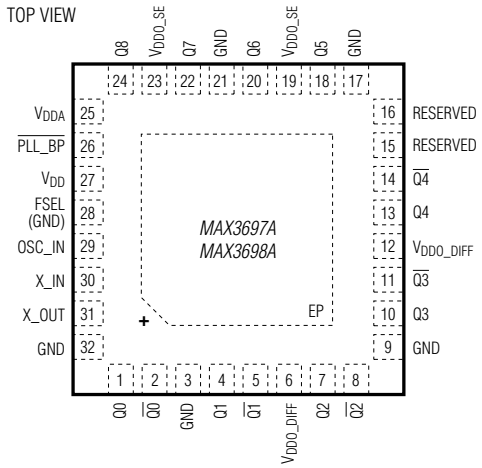
SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



SPURS INDUCED BY POWER-SUPPLY NOISE vs. NOISE FREQUENCY



Pin Configuration



THIN QFN (5mm × 5mm)

( )MAX3698A ONLY.

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

Pin Description

PIN	NAME		FUNCTION
	MAX3697A	MAX3698A	
1	Q0	Q0	LVDS, Noninverting Clock Output
2	$\overline{Q0}$	$\overline{Q0}$	LVDS, Inverting Clock Output
3, 9, 17, 21, 32	GND	GND	Supply Ground
4	Q1	Q1	LVDS, Noninverting Clock Output
5	$\overline{Q1}$	$\overline{Q1}$	LVDS, Inverting Clock Output
6, 12	V_{DDO_DIFF}	V_{DDO_DIFF}	Power Supply for Q0, Q1, Q2, Q3, and Q4 Clock Outputs. Connect to +3.3V.
7	Q2	Q2	LVDS, Noninverting Clock Output
8	$\overline{Q2}$	$\overline{Q2}$	LVDS, Inverting Clock Output
10	Q3	Q3	LVDS, Noninverting Clock Output
11	$\overline{Q3}$	$\overline{Q3}$	LVDS, Inverting Clock Output
13	Q4	Q4	LVDS, Noninverting Clock Output
14	$\overline{Q4}$	$\overline{Q4}$	LVDS, Inverting Clock Output
15	RESERVED	RESERVED	Reserved. Connect to GND.
16	RESERVED	RESERVED	Reserved. Connect to V_{DD}.
18, 20, 22, 24	Q5, Q6, Q7, Q8	Q5, Q6, Q7, Q8	LVCMOS Clock Output
19, 23	VDDO_SE	VDDO_SE	Power Supply for Q5, Q6, Q7, and Q8 Clock Outputs. Connect to +3.3V.
25	V_{DDA}	V_{DDA}	Analog Power Supply for the VCO. Connect to +3.3V. For additional power-supply noise filtering, this pin can connect to V_{DD} through a 10.5Ω resistor as shown in Figure 5.
26	$\overline{PLL\_BP}$	$\overline{PLL\_BP}$	Three-State LVCMOS/LVTTL Input (Active Low). When connected to logic-high, the PLL locks to the crystal interface (25MHz typical at X_IN and X_OUT). When left open (high-Z) the PLL locks to the OSC_IN input (25MHz typical). When connected to logic-low, the PLL is bypassed and the OSC_IN input is selected. When bypass mode is selected, the VCO/PLL is disabled to save power and eliminate intermodulation spurs.
27	V_{DD}	V_{DD}	Core Power Supply. Connect to +3.3V.
28	FSEL	GND	LVCMOS/LVTTL Input. Controls the Q0 output divider on the MAX3697A. For the MAX3697A, connect to logic-low for 125MHz output or connect to logic high for 156.25MHz output. For the MAX3698A, connect to GND.
29	OSC_IN	OSC_IN	LVCMOS Input. Self-biased to allow AC- or DC-coupling. When $\overline{PLL\_BP}$ is open, the OSC_IN input frequency should be 25MHz. When the PLL is in bypass mode ($\overline{PLL\_BP}$ = low), the OSC_IN input frequency can be between 20MHz and 320MHz. When $\overline{PLL\_BP}$ is high, the OSC_IN should be disconnected.
30	X_IN	X_IN	Crystal Oscillator Input
31	X_OUT	X_OUT	Crystal Oscillator Output
—	EP	EP	Exposed Pad. Connect to GND for proper electrical and thermal performance.

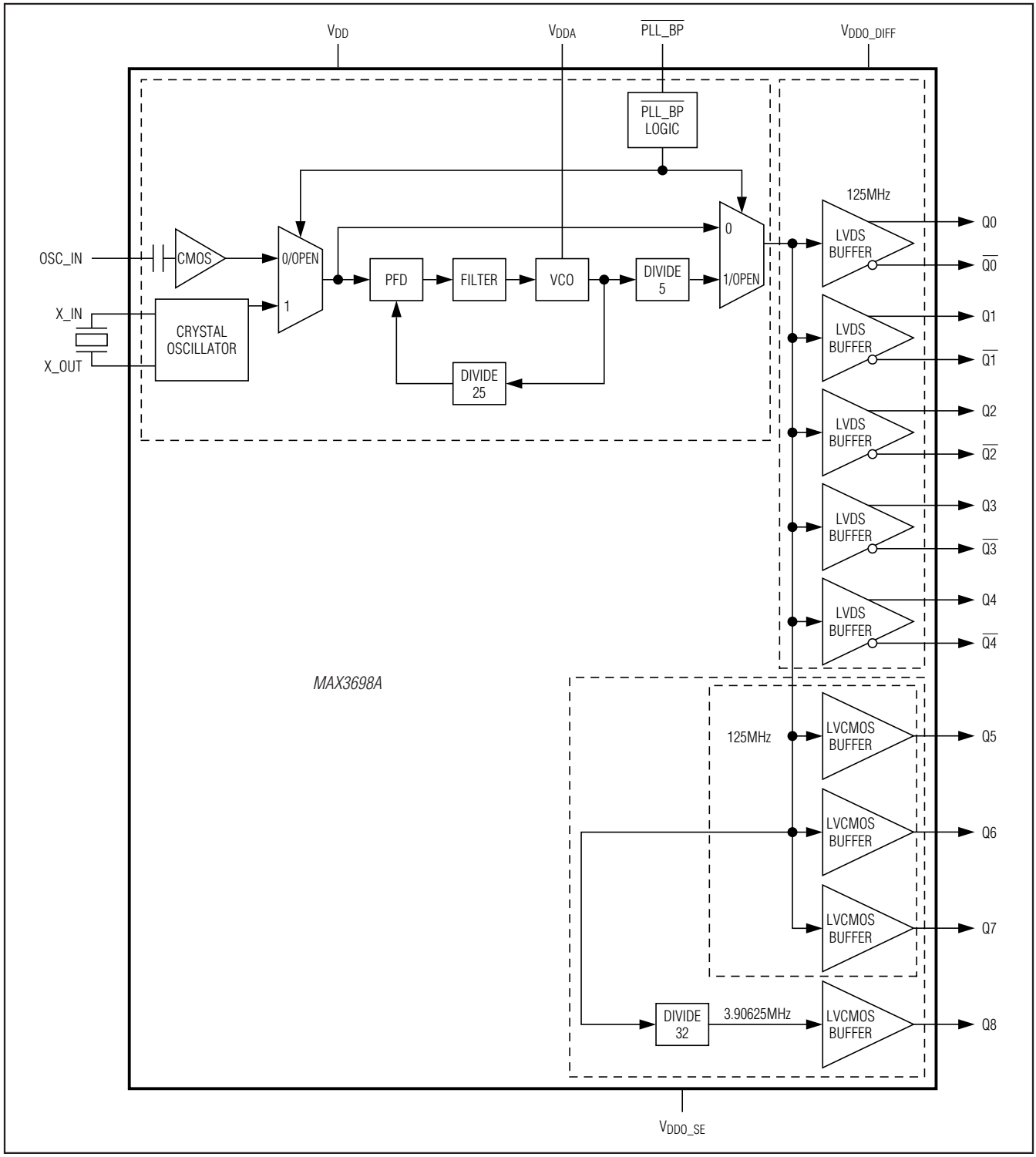


Figure 3. MAX3698A Functional Diagram

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

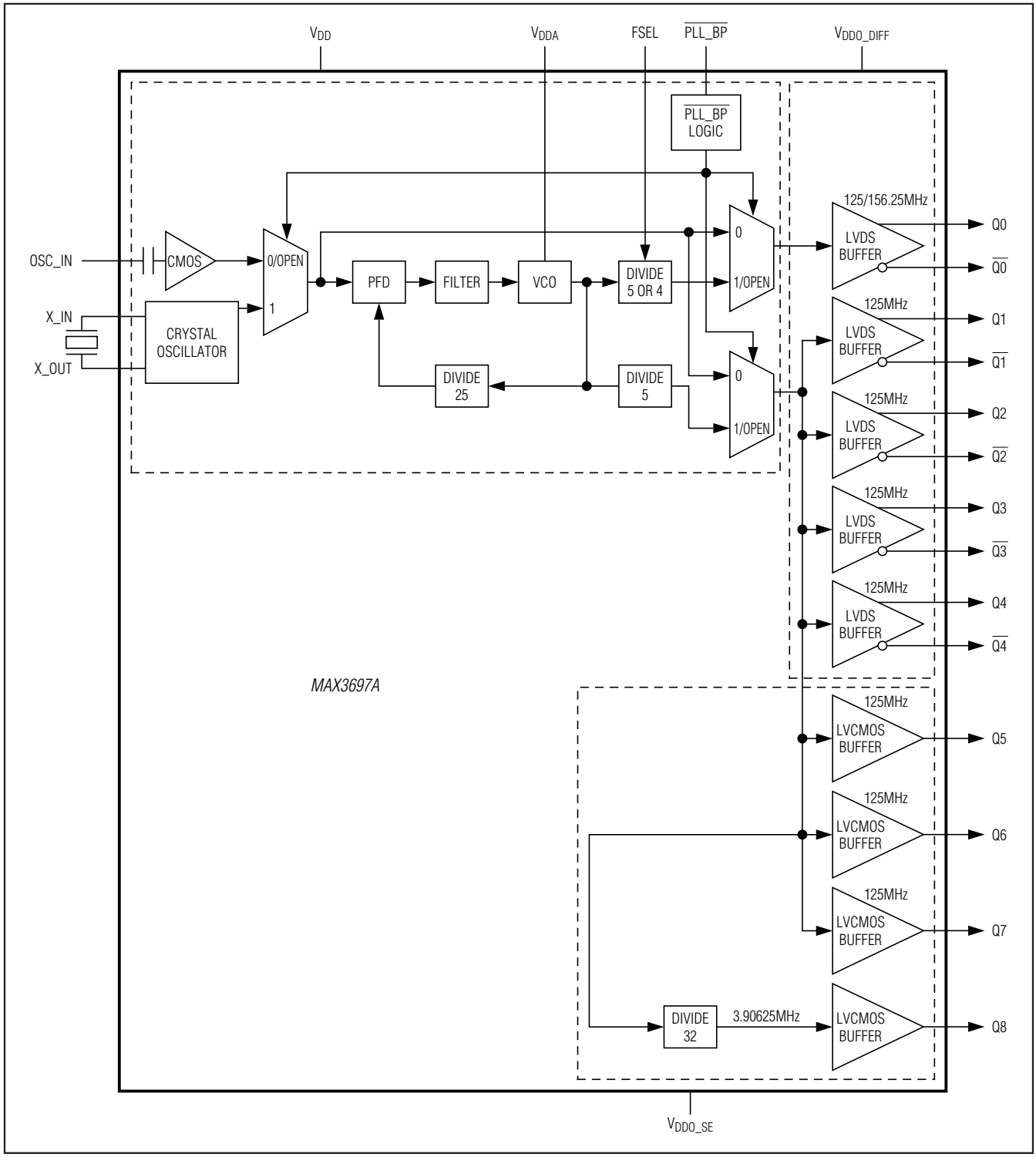


Figure 4. MAX3697A Functional Diagram

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

Detailed Description

The MAX3697A/MAX3698A are frequency generators designed to operate at Ethernet frequencies. They consist of an on-chip crystal oscillator, PLL, LVCMOS output buffers, and LVDS output buffers. Using a low-frequency clock (crystal or CMOS input) as a reference, the internal PLL generates a high-frequency output clock with excellent jitter performance. The MAX3697A comes with a selector pin (FSEL) that allows the Q0 output to be switched between 125MHz and 156.25MHz.

Crystal Oscillator

An integrated oscillator provides the low-frequency reference clock for the PLL. This oscillator requires an external crystal connected between X_IN and X_OUT. The crystal frequency is 25MHz.

OSC_IN Buffer

The LVCMOS OSC_IN buffer is internally biased to allow AC- or DC-coupling. This input is internally AC-coupled, and is designed to operate at 25MHz when the PLL is enabled ($\overline{PLL\_BP}$ is left open). When the PLL is bypassed ($\overline{PLL\_BP}$ is set low), the OSC_IN buffer can be operated from 20MHz to 320MHz.

PLL

The PLL takes the signal from the crystal oscillator or reference clock input and synthesizes a low-jitter, high-frequency clock. The PLL contains a phase-frequency detector (PFD), a lowpass filter, and a voltage-controlled oscillator (VCO) that operates at 625MHz. The VCO output is connected to the PFD input through a feedback divider that divides the VCO frequency by 25 to lock onto the 25MHz reference clock or oscillator. With the VCO locked onto the input reference, a stable 125MHz output clock is provided through a final output divider. The MAX3697A includes an extra control pin (FSEL) that selects either 125MHz or 156.25MHz output frequency at Q0. To minimize noise-induced jitter, the VCO supply (V_{DDA}) is isolated from the core logic and output buffer supplies.

LVDS Drivers

The high-frequency outputs—Q0, Q1, Q2, Q3, and Q4—are differential LVDS buffers designed to drive 100Ω.

LVCMOS Driver

LVCMOS outputs Q5, Q6, Q7, and Q8 are provided on the MAX3697A/MAX3698A. They are designed to drive single-ended high-impedance loads. The maximum data rate for Q5, Q6, and Q7 is 160MHz. Q8 output frequency is equal to the frequency of Q5, Q6, or Q7 divided by 32.

Applications Information

Power-Supply Filtering

The MAX3697A/MAX3698A are mixed analog/digital ICs. The PLL contains analog circuitry susceptible to random noise. To take full advantage of on-board filtering and noise attenuation, in addition to excellent on-chip power-supply rejection, these parts provide a separate power-supply pin, V_{DDA}, for the VCO circuitry. The purpose of this design technique is to ensure clean input power supply to the VCO circuitry and to improve the overall immunity to power-supply noise. Figure 5 illustrates the recommended power-supply filter network for V_{DDA}. This network requires that the power supply is +3.3V ±5%. Decoupling capacitors should be used on all other supply pins for best performance.

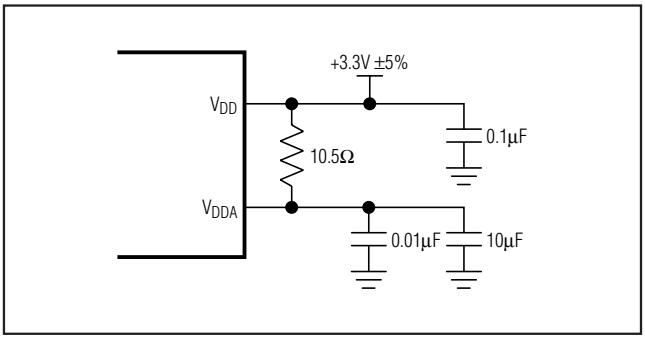


Figure 5. Analog Supply Filtering

Crystal Input Layout and Frequency Stability

The MAX3697A/MAX3698A feature an integrated on-chip crystal oscillator to minimize system implementation cost. The integrated crystal oscillator is a Pierce-type that uses the crystal in its parallel resonance mode. It is recommended to use a 25MHz crystal with a load specification of C_L = 18pF. See Table 1 for the recommended crystal specifications.

The crystal, trace, and two external capacitors should be placed on the board as close as possible to the X_IN and X_OUT pins to reduce crosstalk and active signals into the oscillator.

The layout shown in Figure 6 gives approximately 2pF of trace plus footprint capacitors per side of the crystal (Y1). The dielectric material is FR-4 and dielectric thickness of the reference board is 15 mils. Using a 25MHz crystal and the capacitor values of C45 = 27pF and C46 = 33pF, the measured output frequency accuracy is -1ppm at +25°C ambient temperature.

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

Table 1. Crystal Selection Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Oscillation Frequency	f_{OSC}		25		MHz
Shunt Capacitance	C_O			7.0	pF
Load Capacitance	C_L		18		pF
Equivalent Series Resistance (ESR)	R_S			50	Ω
Maximum Crystal Drive Level				300	µW

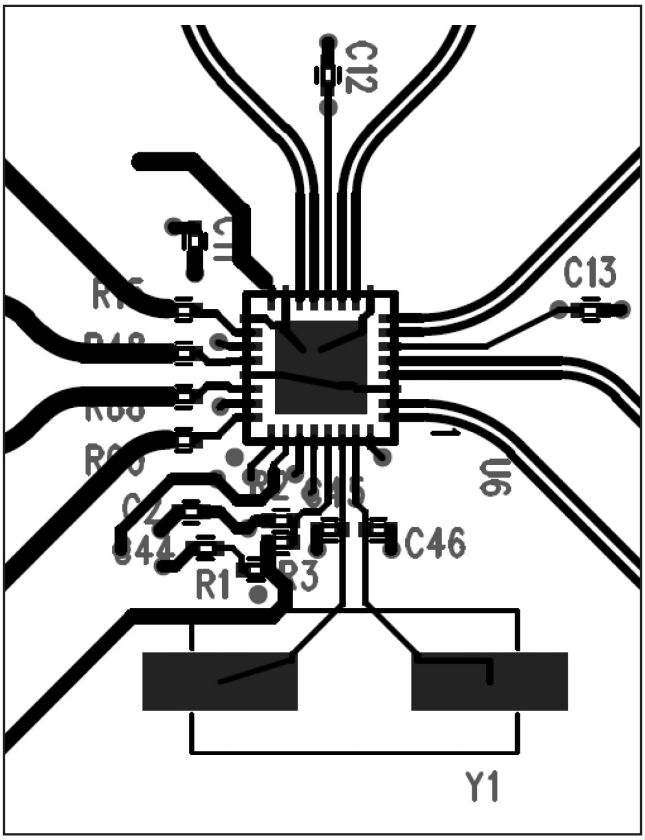


Figure 6. Crystal Layout

Crystal Selection

The crystal oscillator is designed to drive a fundamental mode, AT-cut crystal resonator. See Table 1 for recommended crystal specifications. See Figure 7 for external capacitance connection.

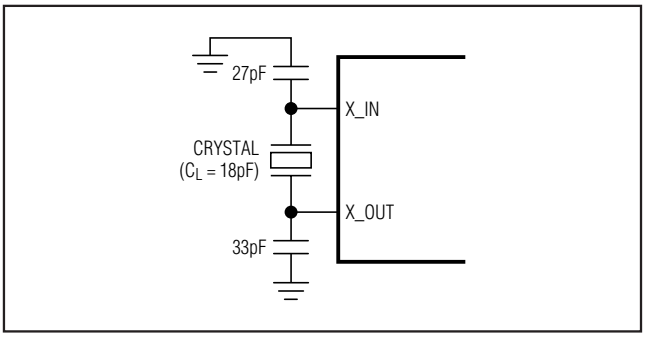


Figure 7. Crystal, Capacitors Connection

Interface Models

Figures 8 and 9 show examples of interface models.

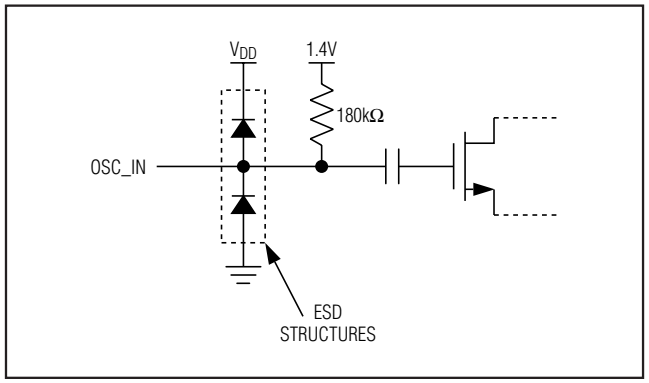


Figure 8. Simplified OSC_IN Pin Circuit Schematic

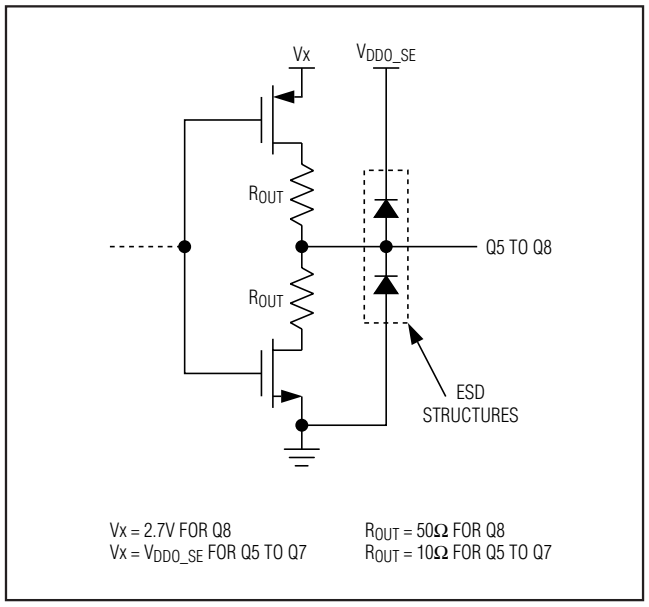


Figure 9. Simplified LVCMOS Output Circuit Schematic

Layout Considerations

The inputs and outputs are the most critical paths for the MAX3697A/MAX3698A and great care should be taken to minimize discontinuities on these transmission lines between the connector and the IC. Here are some suggestions for maximizing the performance of the MAX3697A/MAX3698A:

- An uninterrupted ground plane should be positioned beneath the clock outputs. The ground plane under the crystal should be removed to minimize capacitance.
- Ground pin vias should be placed close to the IC and the input/output interfaces to allow a return current path to the MAX3697A/MAX3698A and the receive devices.
- Supply decoupling capacitors should be placed close to the supply pins, preferably on the same layer as the MAX3697A/MAX3698A.
- Take care to isolate crystal input traces from the MAX3697A/MAX3698A outputs.
- The crystal, trace, and two external capacitors should be placed on the board as close as possible to the X_IN and X_OUT pins to reduce crosstalk and active signals into the oscillator.
- Maintain 100Ω differential (or 50Ω single-ended) transmission line impedance into and out of the part.
- Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk.

Refer to the MAX3697A and MAX3698A evaluation kits for more information.

Exposed-Pad Package

The exposed pad on the 32-pin TQFN package provides a very low inductance path for return current traveling to the PCB ground plane. The pad is also electrical ground on the MAX3697A/MAX3698A and must be soldered to the circuit board ground for proper electrical performance.

Chip Information

TRANSISTOR COUNT: 13,768

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **http://www.microsemi.com**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+5	21-0140	90-0013

+3.3V, Low-Jitter, Precision Clock Generator with Multiple Outputs

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/10	Initial release	—

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