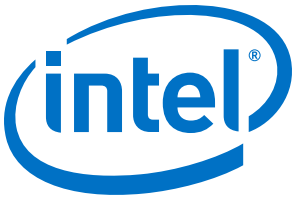

# Intel® Stratix® 10 Power Management User Guide

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# Contents

# 1. Intel® Stratix® 10 Power Management Overview

The Intel® Stratix® 10 device family offers SmartVID standard power devices in all speed grades. Lower power fixed-voltage devices are also available in all speed grades except for the fastest speed grade.

Intel Stratix 10 devices also offer power gating feature to the digital signal processing (DSP) blocks and M20K memory blocks that are not in use for static power savings. You can implement this feature through the Intel Quartus® Prime software. This user guide describes power saving features of the Intel Stratix 10 device family, and also describes the power-up and power-down sequencing requirements for the Intel Stratix 10 devices.

### Related Information

- Intel Stratix 10 Device Family Pin Connection Guidelines
- Intel Stratix 10 Device Datasheet

# 2. Intel Stratix 10 Power Management Architecture and Features

The following sections describe the power consumption, power reduction techniques, power sense line feature, power-on reset (POR) requirements, power-up and power-down sequencing requirements.

## 2.1. Power Consumption

The total power consumption of an Intel Stratix 10 device consists of the following components:

- Static power—the power that the configured device consumes when powered up but no user clocks are operating, excluding DC bias power of analog blocks, such as I/O and transceiver analog circuitry.
- Dynamic power—the additional power consumption of the device due to signal activity or toggling.
- Standby power—the component of active power that is independent of signal activity or toggling. Standby power includes, but is not limited to, I/O and transceiver DC bias power.

### 2.1.1. Dynamic Power Equation

The following equation shows how to calculate dynamic power where P is power, C is the load capacitance, and V is the supply voltage level. The frequency refers to the clock frequency and data toggles once every clock cycle.

**Figure 1. Dynamic Power Equation**

$$P = \frac{1}{2} CV^2 \times frequency$$

The equation shows that power is design-dependent. Power is dependent on the operating frequency of your design, applied voltage, and load capacitance, which depends on design connectivity. Intel Stratix 10 devices minimize static and dynamic power using advanced process optimizations. These optimizations allow Intel Stratix 10 designs to meet specific performance requirements with the lowest possible power.

## 2.2. Power Reduction Techniques and Features

Intel Stratix 10 devices leverage on advanced 14-nm process technology, an enhanced core architecture, and various optimizations to reduce total power consumption. The power reduction techniques and features are listed below:

- SmartVID Standard Power Devices
- Power-Screened Devices
- Temperature Compensation
- DSP and M20K Power Gating
- Clock Gating
- Power Sense Line

### 2.2.1. SmartVID Standard Power Devices

The SmartVID feature compensates for process variation by narrowing the process distribution using voltage adaptation. This feature is supported in devices with the –V standard power option only. For the –V standard power option devices, you must connect the PWRMGT_SCL and PWRMGT_SDA pins in both the Power Management BUS (PMBus™) master and PMBus slave modes. An additional PWRMGT_ALERT pin is required when you configure the Intel Stratix 10 device in the PMBus slave mode. All connections required must be set up on the circuit board and the Intel Quartus Prime software.

For more information about how to connect these pins on the circuit board, refer to the *Intel Stratix 10 Device Family Pin Connection Guidelines*.

For instructions to set up the connection in the Intel Quartus Prime software, refer to the *Specifying Parameters and Options* section of this document.

*Note:* Intel Stratix 10 standard power devices (–1V, –2V, –3V power grade) are SmartVID devices. The core voltage supplies ($V_{CC}$ and $V_{CCP}$) for each SmartVID device must be driven by a PMBus-compliant voltage regulator dedicated to the Intel Stratix 10 –V device that is connected to that Intel Stratix 10 device via PMBus. For Intel Stratix 10 standard power devices, use of a PMBus-compliant voltage regulator for each device is mandatory. Intel Stratix 10 devices will not configure or function correctly if the core voltage is driven by a non-PMBus compliant regulator with a fixed output voltage.

Intel programs the optimum voltage level required by each individual Intel Stratix 10 device into a fuse block during device manufacturing. The Secure Device Manager (SDM) Power Manager reads these values and can communicate them to an external power regulator or a system power controller through the PMBus interface.

The SmartVID feature allows a power regulator to provide the Intel Stratix 10 device with $V_{CC}$ and $V_{CCP}$ voltage levels that maintain the performance of the specific device speed grade. When the SmartVID feature is used:

1. Intel Stratix 10 devices are initially powered up to a nominal voltage level of 0.9V for both $V_{CC}$ and $V_{CCP}$.
2. After the SmartVID value in the Intel Stratix 10 device is determined and propagated to the external voltage regulator, both the $V_{CC}$ and $V_{CCP}$ voltages are regulated based on the SmartVID value.

**Related Information**

- Intel Stratix 10 Device Family Pin Connection Guidelines
- Specifying Parameters and Options on page 22

### 2.2.1.1. SmartVID Feature Implementation in Intel Stratix 10 Devices

Devices supporting the SmartVID feature have a SmartVID value programmed into a fuse block during device manufacturing. The SmartVID value represents a voltage level in the range of 0.8V to 0.94V. Each device has its own specific SmartVID value.

The SmartVID value is sent to the external regulator or system power controller through the PMBus interface. Upon receiving the SmartVID value, an adjustable regulator tunes the $V_{CC}$ and $V_{CCP}$ voltage levels to the voltage specified by the SmartVID value.

Intel Stratix 10 devices perform the SmartVID setup in the early stage of the configuration process. The SmartVID process will continue to monitor the $V_{CC}$ and $V_{CCP}$ voltage rails in user mode. The Power Manager monitors the temperature and adjusts the voltage when required. For more information, refer to the Temperature Compensation section.

**Table 1. SmartVID Regulator Requirements**

| Specification | Value |
|---|---|
| Voltage range | 0.8 V – 0.94 V |
| Voltage step | 10 mV |
| Ramp time | • Non-CvP—10 mV/10 ms to 10 mV/20 µs<br>• Configuration via Protocol (CvP)—10 mV/60 µs to 10 mV/20 µs (1) |

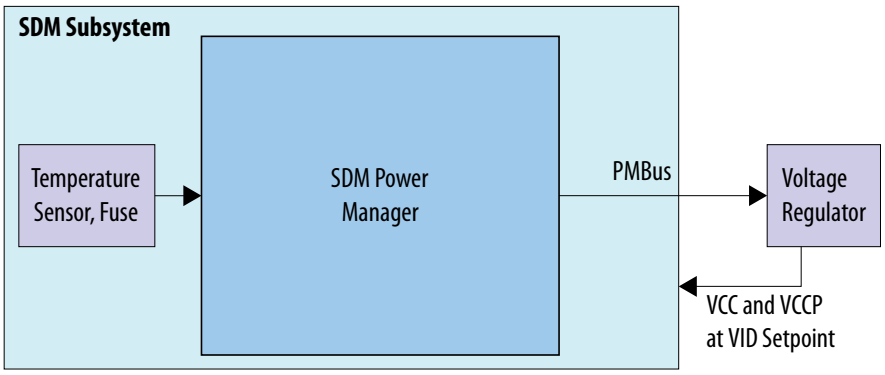
**Related Information**

- Temperature Compensation on page 11
- Recommended Operating Conditions
  Provides more information on the voltage range specifications.

(1) When the system is required to support the CvP functionality and meet the PCI Express* (PCIe*) link-up timing budget during the initial power up, the minimum ramp time is 10 mV/60 µs.

### 2.2.1.2. SDM Power Manager

**Figure 2. SDM Power Manager Block Diagram**




In Intel Stratix 10 devices, the SmartVID feature is managed by the SDM subsystem. The SDM subsystem is powered up after $V_{CC}$ and $V_{CCP}$ voltage levels are powered up to 0.9V. The SDM Power Manager reads the SmartVID programmed value and communicates this value to the external voltage regulator through the PMBus interface.

The SDM Power Manager has the following stages:

- Initial/Shutdown stage
  - Powers up $V_{CC}$ and $V_{CCP}$ to the voltage level based on the SmartVID programmed value and the device temperature.
  - Configures the FPGA and switches the FPGA to user mode.
- Monitor stage
  - Monitors temperature and updates the $V_{CC}$ and $V_{CCP}$.

The shutdown stage is triggered during device reconfiguration.

#### 2.2.1.2.1. PMBus Master Mode

In the PMBus master mode, during the initial stage, the SDM Power Manager powers up the $V_{CC}$ and $V_{CCP}$ to the voltage level based on the SmartVID programmed value and the device temperature before it starts to configure the FPGA. After entering the user mode (in the monitor stage), the SDM Power Manager monitors temperature changes and decides if the $V_{CC}$ and $V_{CCP}$ output voltage values need to be updated. If voltages require updating, the SDM Power Manager identifies the voltage value based on the fuse values and the current temperature and sends the desired voltage value to the voltage regulators through the PMBus (PWRMGT_SCL and PWRMGT_SDA).

The PMBus master mode supports the multi-master mode.

*Note:* The PMBus mode only supports the 1.8-V I/O standard.

**Figure 3. PMBus Master Mode**

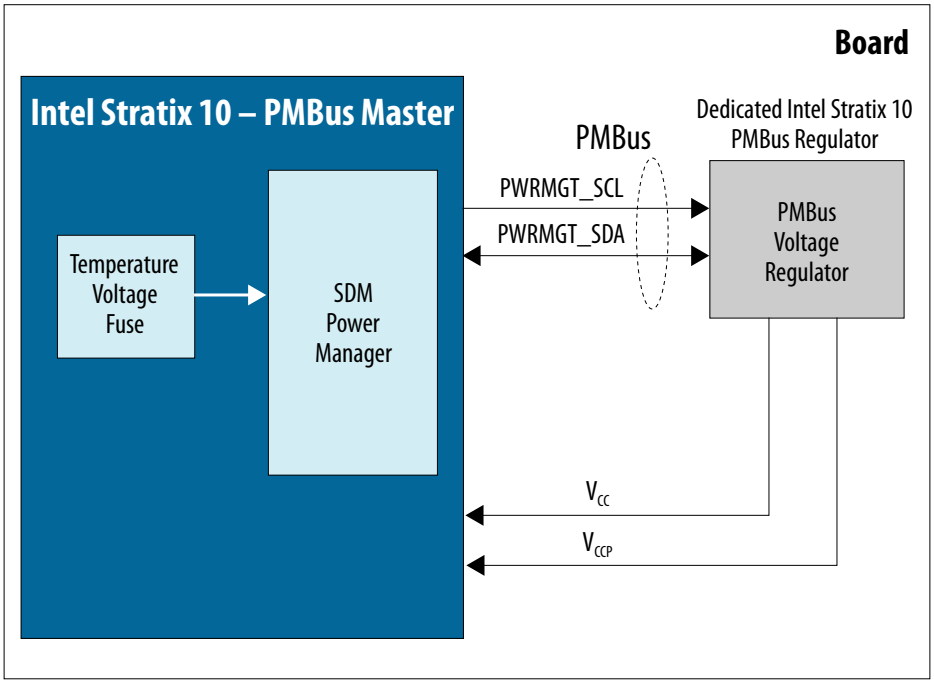



**Table 2. Supported Commands for the PMBus Master Mode**

| Command Name | Command Code | PMBus Transaction Type | Number of Bytes |
|---|---|---|---|
| PAGE(2) | 00h | Write byte | 1 |
| VOUT_MODE(3) | 20h | Read byte | 1 |
| VOUT_COMMAND | 21h | Write word | 2 |
| READ_VOUT | 8Bh | Read word | 2 |
| MFR_ADC_CONTROL(4) | D8h | Write byte | 1 |

**Related Information**

Power Management and VID Parameters on page 23

(2) This is an optional command. This command is only applicable if you enable the PAGE command parameter. For more information, refer to the Power Management and VID Parameters section.

(3) This is an optional command. This command is only applicable if you select the Auto discovery in the voltage output format parameter. For more information, refer to the Power Management and VID Parameters section.

(4) This command is sent when you set the device type to LTM4677 only.

### 2.2.1.2.2. PMBus Slave Mode

Intel Stratix 10 devices can also be configured in the PMBus slave mode with an external power management controller acting as the PMBus master. When you configure the Intel Stratix 10 device in the PMBus slave mode, you must connect an additional PWRMGT_ALERT pin while connecting the existing PWRMGT_SCL and PWRMGT_SDA pins.

*Note:* The PMBus mode only supports the 1.8-V I/O standard.

**Figure 4. PMBus Slave Mode**

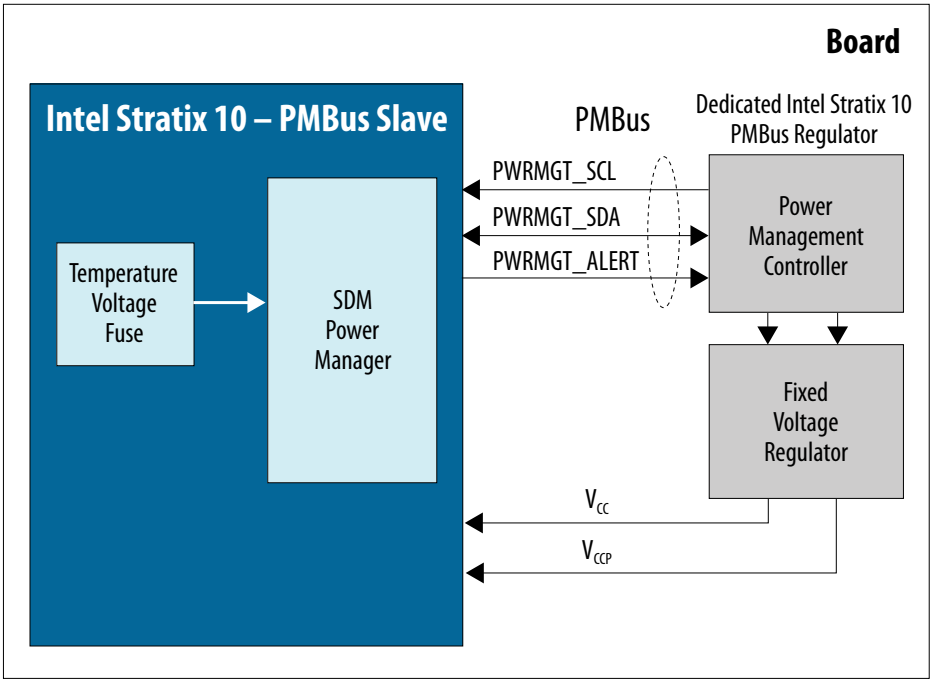
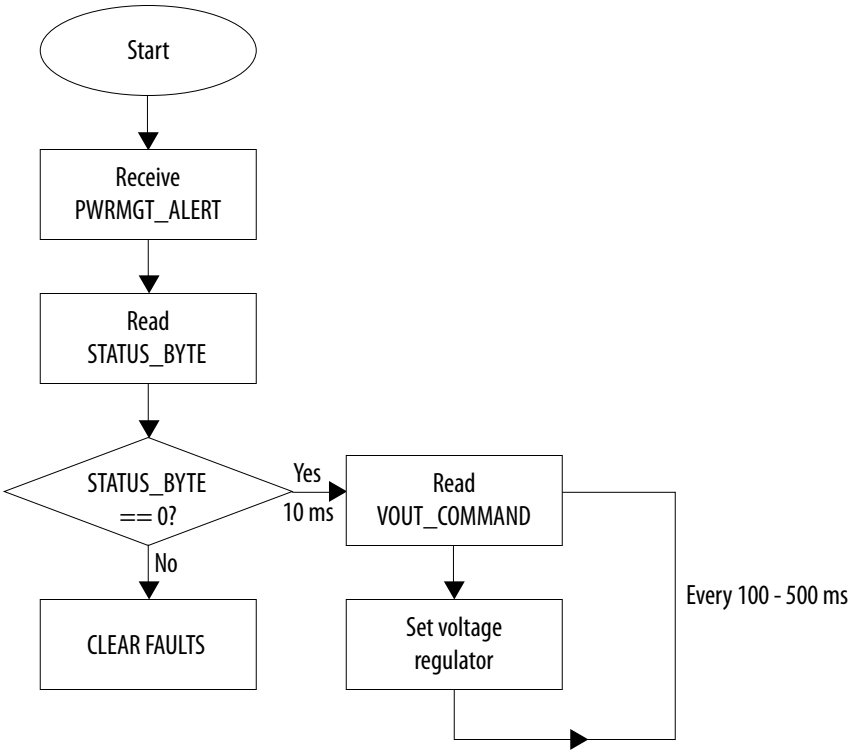



**Table 3. Supported Commands for the PMBus Slave Mode**

| Command Name | Command Code | Default | PMBus Transaction Type | Number of Bytes |
|---|---|---|---|---|
| CLEAR_FAULTS | 03h | — | Send byte | 0 |
| VOUT_MODE | 20h | 40h | Read byte | 1 |
| VOUT_COMMAND | 21h | — | Read word | 2 |
| STATUS_BYTE | 78h | 00h | Read byte | 1 |

The following figure shows the stage flow for the external power management controller in the PMBus slave mode.

**Figure 5. Stage Flow for the External Power Management Controller in the PMBus Slave Mode**




The Intel Stratix 10 device in the PMBus slave mode will be sending the VOUT_COMMAND value in the direct format only. To read the actual voltage value, use the following equation to convert the VOUT_COMMAND value from the Intel Stratix 10 device.

**Figure 6. Direct Format Equation**

$$X = \frac{1}{m}\left(Y \times 10^{-R} - b\right)$$

The equation shows how to convert the direct format value where:

- X, is the calculated, real value units in mV;
- m, is the slope coefficient, a 2-byte two's complement integer;
- Y, is the 2-byte two's complement integer received from the Intel Stratix 10 device;
- b, is the offset, a 2-byte two's complement integer;
- R, is the exponent, a 1-byte two's complement integer

The following example shows how an external power management controller retrieves values from the Intel Stratix 10 device. Coefficients used in the VOUT_COMMAND are as follows:

- m = 1
- b = 0
- R = 0

If the external power management controller retrieved a value of 0384h, it is equivalent to the following:

$X = (1/1) \times (0384h \times 10^{-0} - 0) = 900\ mV = 0.90\ V$

## 2.2.2. Power-Screened Devices

Intel Stratix 10 power-screened devices are available in –2L and –3X options. Power-screened devices offer lower static power than the SmartVID –V power option devices. The –2L and –3X power-screened devices run at a fixed-voltage supply and do not require using the PMBus regulator.

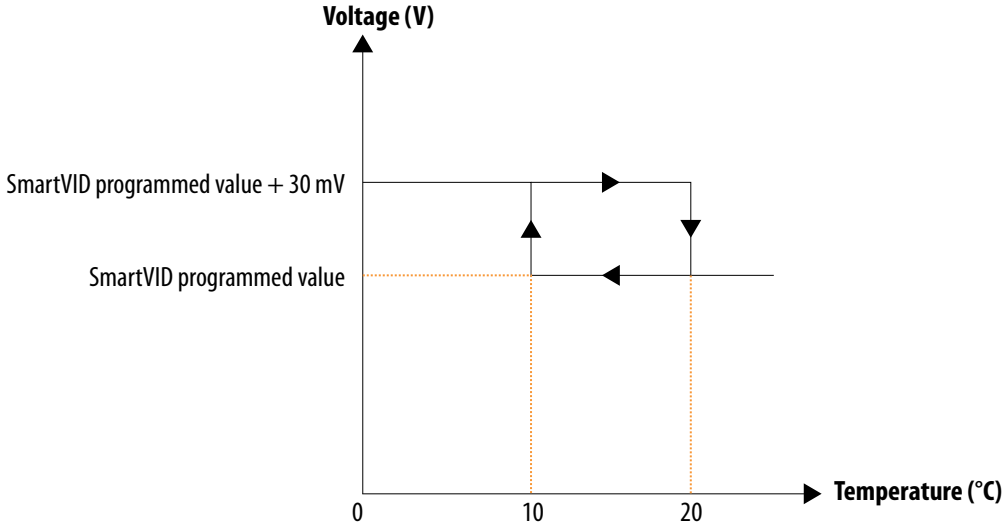
## 2.2.3. Temperature Compensation

Intel Stratix 10 devices are able to compensate for performance degradation at colder temperatures by raising the voltage. While raising the voltage does increase the dynamic power consumption, this is countered by lower leakage at cold temperatures, thus enabling total power consumption at cold temperatures to still be lower than at hot temperatures.

The SmartVID feature supports this dynamic voltage adjustment. The SDM Power Manager checks for temperature changes and updates the new VID value if the temperature crosses the threshold point.

**Figure 7. Temperature Compensation for SmartVID for Intel Stratix 10 Devices—Preliminary**

The SDM monitors the temperature, normally at every 100 ms, and adjusts the voltage by communicating with an external power management system. Adjustment is made by the SDM after the sensor detects the temperature setting is below 10 °C or above 20 °C.



### 2.2.4. DSP and M20K Power Gating

Power gating of the DSP blocks and M20K memory blocks is enabled via the configuration RAM (CRAM) bits. Intel Stratix 10 devices support power gating for both DSP blocks and M20K memory blocks. By default, the Intel Quartus Prime software automatically configures unused DSP blocks and M20K memory blocks to be power gated.

### 2.2.5. Clock Gating

Clock gating can be used to reduce dynamic power consumption. When an application is idle, its clock can be gated temporarily and ungated based on wake-up events. This is done using user logic to enable or disable the global clock (GCLK) and sector clock (SCLK).

You can perform dynamic power reduction by gating the clock signals of any circuitry not used by the design in the Intel Stratix 10 devices. The sector clock gating is done at the multiplexer level.

Clock gating a large portion of your FPGA design could cause significant current change over a short time period when the gated circuitry is enabled or disabled. The maximum current step resulting from this clock gating should be sized such that it does not create noise exceeding the maximum allowed AC noise specification, as determined by the PDN decoupling design on your PCB. You can control the current step size by dividing a large gated area into smaller sub-regions and staging those regions to enter or exit power gating sequentially.

### 2.2.6. Power Sense Line

Intel Stratix 10 devices support the power sense line feature. VCCLSENSE and GNDSENSE pins are differential remote sense pins used to monitor the $V_{CC}$ power supply.

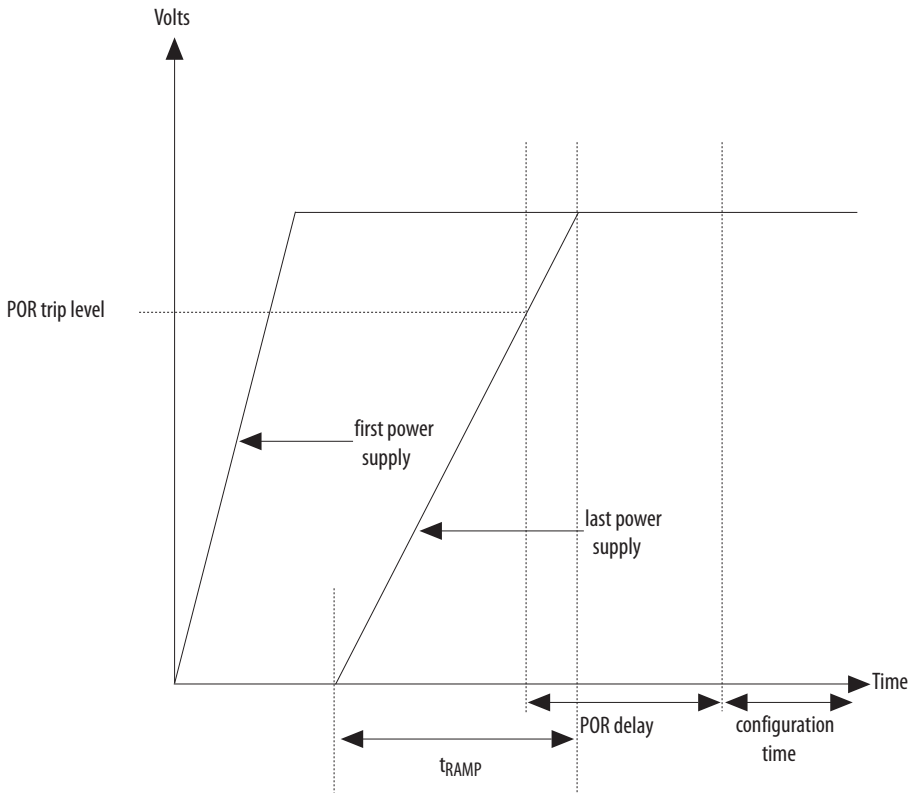
You must connect the VCCLSENSE and GNDSENSE pins to the remote sense inputs for all regulators that support the remote voltage sensing feature.

## 2.3. Power-On Reset Circuitry

The POR circuitry keeps the Intel Stratix 10 device in the reset state until the power supply outputs are within the recommended operating range.

A POR event occurs when you power up the Intel Stratix 10 device until all power supplies monitored by the POR circuitry reach the recommended operating range within the maximum power supply ramp time, $t_{RAMP}$. If $t_{RAMP}$ is not met, the Intel Stratix 10 device I/O pins and programming registers remain tri-stated, which may cause device configuration to fail.

**Figure 8. Relationship Between $t_{RAMP}$ and POR Delay**




The Intel Stratix 10 POR circuitry uses individual detection circuitry to monitor each of the configuration-related power supplies independently. The POR circuitry is gated by the outputs of all the individual detectors.

POR delay is the time from when the POR trips out to the final reset signal.

The Intel Stratix 10 device is held in the POR state until all power supplies have passed their trigger point. After power supplies have passed the trigger point, the SDM will wait for a configurable delay time and then start device configuration.

## 2.3.1. Power Supplies Monitored and Not Monitored by the POR Circuitry

**Table 4. Power Supplies Monitored and Not Monitored by the Intel Stratix 10 POR Circuitry**

| Power Supplies Monitored | Power Supplies Not Monitored |
|---|---|
| • $V_{CC}$<br>• $V_{CCERAM}$<br>• $V_{CCPT}$<br>• $V_{CCADC}$<br>• $V_{CCIO\_SDM}$<br>• $V_{CCBAT}$<br>• $V_{CCL\_HPS}$ (5) | • $V_{CCP}$<br>• $V_{CCR\_GXB}$<br>• $V_{CCT\_GXB}$<br>• $V_{CCH\_GXB}$<br>• $V_{CCIO}$<br>• $V_{CCIO\_HPS}$ (5) |

(5) These are only supported by system-on-a-chip (SoC) FPGA.

| Power Supplies Monitored | Power Supplies Not Monitored |
|---|---|
| | • $V_{CCA\_PLL}$<br>• $V_{CCFUSEWR\_SDM}$<br>• $V_{CCPLLDIG\_SDM}$<br>• $V_{CCPLLDIG\_HPS}$(5)<br>• $V_{CCPLL\_HPS}$(5)<br>• $V_{CCPLL\_SDM}$<br>• $V_{CCM\_WORD}$<br>• $V_{CCIO\_UIB}$<br>• $V_{CCRT\_GXE}$<br>• $V_{CCRTPLL\_GXE}$ |

*Note:* For the device to exit POR, you must power the $V_{CCBAT}$ power supply even if you do not use the volatile key.

## 2.4. Power Sequencing Considerations for Intel Stratix 10 Devices

The Intel Stratix 10 devices require a specific power-up and power-down sequence. This section describes several power management options and discusses proper I/O management during device power-up and power-down. Design your power supply solution to properly control the complete power sequence.

The requirements in this section must be followed to prevent unpredictable current draw to the FPGA device, which can potentially impact the I/O functionality. Intel Stratix 10 devices do not support 'Hot-Socketing' except under the conditions stated in the table below. The table below also shows what the unpowered pins can tolerate during power-up and power-down sequences.

**Table 5. Pin Tolerance – Power-Up/Power-Down**

'√' is Acceptable; '-' is Not Applicable.

| Pin Type | Power-Up | | | | Power-Down | | | |
|---|---|---|---|---|---|---|---|---|
| | Tristate | Drive to GND | Drive to VCCIO | Driven with < 1.1 Vp-p | Tristate | Drive to GND | Drive to VCCIO | Driven with < 1.1 Vp-p |
| 3VIO banks | √ | - | - | - | √ | √ | - | - |
| LVDS I/O banks | √ | √ | √(6) | - | √ | √ | √(6) | - |
| Differential Transceiver pins | √ | √ | - | √(7) | √ | √ | - | √(7) |

**Related Information**

- LVDS I/O Pin Guidance for Unpowered FPGA
- Transceiver Pin Guidance for Unpowered FPGA

(6) The maximum current allowed through any LVDS I/O bank pin when the device is unpowered or during power up/down conditions = 10 mA (refer to "LVDS I/O Pin Guidance for Unpowered FPGA Pins").

(7) This applies to Intel Stratix 10 L-Tile/H-Tile only (refer to "Transceiver Pin Guidance for Unpowered FPGA Transceiver Pins").

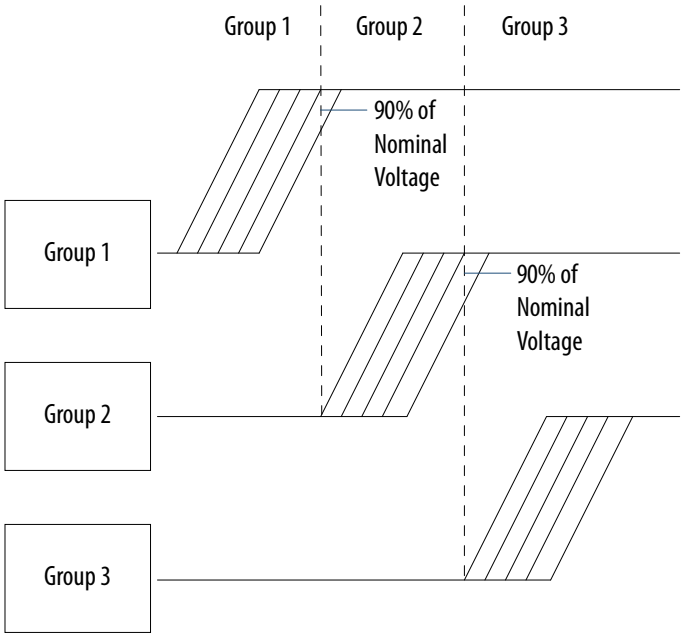
## 2.4.1. Power-Up Sequence Requirements for Intel Stratix 10 Devices

*Note:* To satisfy the power-up requirements, program the FPGA device immediately after the power-up sequence completes.

The power rails in Intel Stratix 10 devices are each divided into three groups. Refer to the *Intel Stratix 10 Device Family Pin Connection Guidelines* and *AN692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria® 10, and Intel Stratix 10 Devices* for additional details.

The diagram below illustrates the voltage groups of the Intel Stratix 10 devices and their required power-up sequence.

**Figure 9. Power-Up Sequence for Intel Stratix 10 Devices**




*Note:* VCCBAT is not in any of the groups below. VCCBAT does not have any sequence requirements. VCCBAT holds the contents of the security keys.

**Table 6. Voltage Rails**

| Power Group | Intel Stratix 10 |
|---|---|
| Group 1 | $V_{CC}$<br>$V_{CCP}$<br>$V_{CCERAM}$<br>$V_{CCR\_GXB}$<br>$V_{CCT\_GXB}$<br>$V_{CCL\_HPS}$<br>$V_{CCPLLDIG\_SDM}$<br>$V_{CCRT\_GXE}$ (TX device)<br>$V_{CCRTPLL\_GXE}$ (TX device) |
| Group 2 | $V_{CCPT}$<br>$V_{CCH\_GXB}$ |

***continued...***

| Power Group | Intel Stratix 10 |
|---|---|
| | $V_{CCA\_PLL}$<br>$V_{CCPLL\_HPS}$<br>$V_{CCPLL\_SDM}$<br>$V_{CCADC}$<br>$V_{CCH\_GXE}$ (TX device) |
| Group 3 | $V_{CCIO}$<br>$V_{CCIO3V}$<br>$V_{CCIO\_SDM}$<br>$V_{CCIO\_HPS}$<br>$V_{CCFUSEWR\_SDM}$<br>$V_{CCIO\_UIB}$<br>$V_{CCM}$<br>$V_{CCCLK\_GXE}$ (TX device) |

All power rails in Group 1 must ramp up (in any order) to a minimum of 90% of their respective nominal voltage before the power rails from Group 2 can start ramping up.

The power rails within Group 2 can ramp up in any order after the last power rail in Group 1 ramps to the minimum threshold of 90% of its nominal voltage. All power rails in Group 2 must ramp to a minimum threshold of 90% of their nominal value before the Group 3 power rails can start ramping up.

The power rails within Group 3 can ramp up in any order after the last power rail in Group 2 ramps up to a minimum threshold of 90% of their full value.

For Intel Stratix 10 devices, you can combine and ramp up Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as Group 2 power rail $V_{CCPT}$.

*Note:* Ensure that the newly combined power rails do not cause any driving of unpowered GPIO or transceiver pins.

All power rails must ramp up monotonically. The power-up sequence should meet either the standard or the fast POR delay time. The POR delay time depends on the POR delay setting you use. For the POR specifications of the Intel Stratix 10 devices, refer to the POR Specifications section in the *Intel Stratix 10 Device Datasheet* .

For configuration via protocol (CvP), the total TRAMP must be less than 10 ms from the first power supply ramp-up to the last power supply ramp-up. Select a fast POR delay setting to allow sufficient time for the PCI Express (PCIe) link initialization and configuration. The power-up sequence must meet either the standard or fast POR delay time depending on the POR delay setting you use.

### Related Information

- Intel Stratix 10 Device Family Pin Connection Guidelines
- AN692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
- POR Specifications

## 2.4.2. Power-Down Sequence Recommendations and Requirements for Intel Stratix 10 Devices

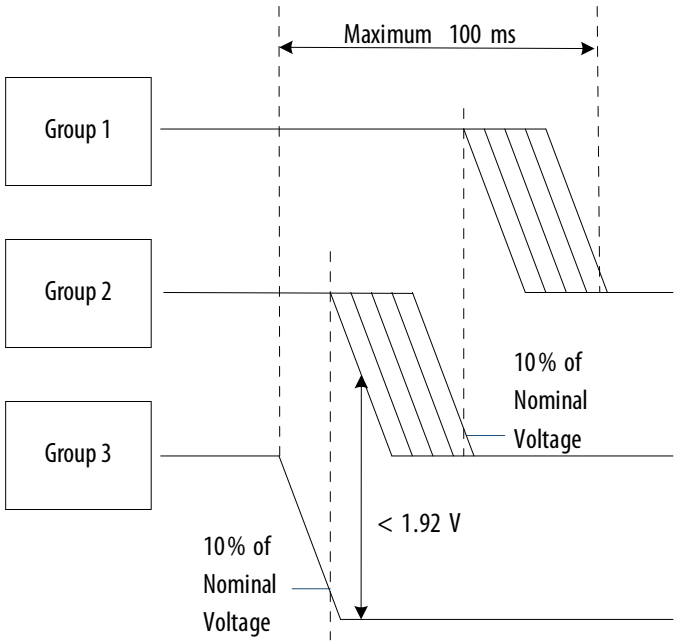
Intel's FPGAs need to follow certain requirements during a power-down sequence. The power-down sequence can be a controlled power-down event via an on/off switch or an uncontrolled event as with a power supply collapse. In either case, you must follow a specific power-down sequence. Below are four power-down sequence specifications. They are either Recommended (one), Required (two), or Relaxed (one). To comply with Intel's FPGA Power-Down requirements, the Recommended option is best.

*Note:* If you cannot follow the Recommended specification, you must follow the Required specification.

### Recommended Power-Down Ramp Specification

This is the best option to minimize power supply currents.

**Figure 10. Recommended Power-Down Ramp Specification**




- Power down all power rails fully within 100 ms.
- Power down power supplies within the same Group in any order.
- Before Group 2 supplies power down, power down all Group 3 supplies within 10% of GND.
- Before Group 1 supplies power down, power down all Group 2 supplies within 10% of GND.
- The maximum voltage differential between any Group 3 supply and any Group 2 supply is 1.92 V.

For Intel Stratix 10 devices, you can combine and ramp down Group 3 power rails with Group 2 power rails if the two groups share the same voltage level and the same voltage regulator as the Group 2 power rails.

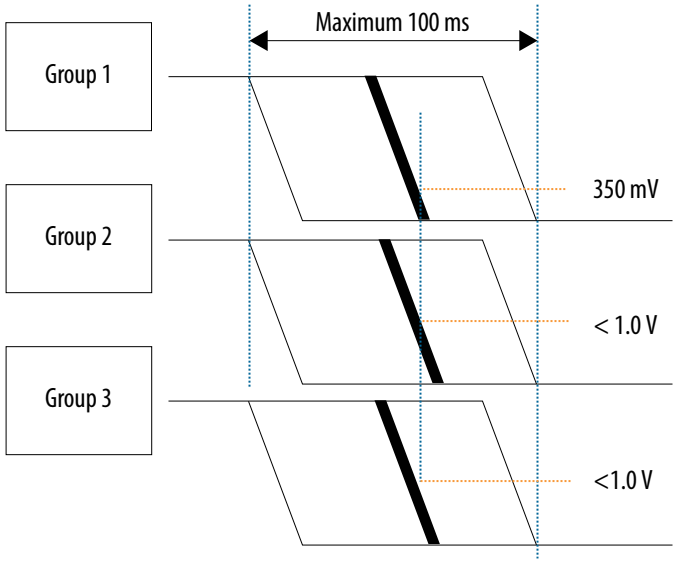
- Ensure that the newly combined power rails do not cause any driving of unpowered GPIO or transceiver pins.
- Ensure that the newly combined power rails do not violate any power-down sequencing specification due to device (third party) leakage; maintain the Required Voltage Differential Specification.

During the power-up/down sequence, the device output pins are tri-stated. To ensure long term reliability of the device, Intel recommends that you do not drive the input pins during this time.

### Required Power-Down Ramp Specification

In cases where power supply is collapsing or if the recommended specification cannot be met, the following PDS sequence is required.

**Figure 11. Required Power-Down Ramp Specification**



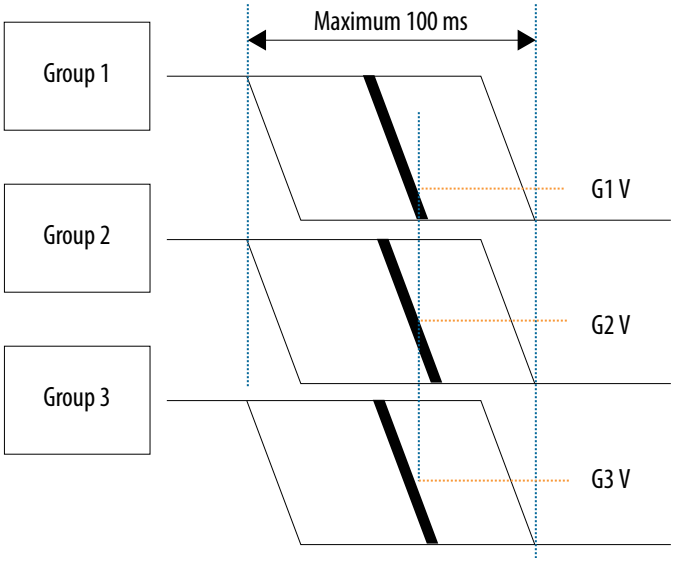

- Power down all power rails fully within 100 ms.
- As soon as possible, disable all power supplies.
  - Tri-state Group 1 supplies, and do not drive them actively to GND.
  - If possible, drive or terminate Group 2 and Group 3 supplies to GND.
- Ensure no alternative sourcing of any power supply exists during the power-down sequence; reduce all supplies monotonically and with a consistent RC typical decay.
- By the time any Group 1 supply goes under 0.35 V, all Group 2 and Group 3 supplies must be under 1.0 V.

### Required Voltage Differential Specification

To not excessively overstress device transistors during power-down, there is an additional voltage requirement between any two power supplies between different power groups during power-down:

$\Delta V < \Delta V_{nom} + 500$ mV

**Figure 12. Required Voltage Differential Specification**




- Power down all power rails fully within 100 ms.
- For example, if Group 1 Voltage = 0.9 V, Group 2 Voltage = 1.8 V, and Group 3 Voltage = 3.0 V, then:

| | | |
|---|---|---|
| $G3V_{nom}$ = 3.0 V<br>$G2V_{nom}$ = 1.8 V | $G2V_{nom}$ = 1.8 V<br>$G1V_{nom}$ = 0.9 V | $G3V_{nom}$ = 3.0 V<br>$G1V_{nom}$ = 0.9 V |
| $(G3V - G2V)_{nom}$ = 1.2 V | $(G2V - G1V)_{nom}$ = 0.9 V | $(G3V - G1V)_{nom}$ = 2.1 V |
| (G3V – G2V) <= 1.2 V + .5 V | (G2V – G1V) <= 0.9 V + .5 V | (G3V – G1V) <= 2.1 V + .5 V |
| (G3V – G2V) <= 1.7 V | (G2V – G1V) <= 1.4 V | (G3V – G1V) <= 2.6 V |

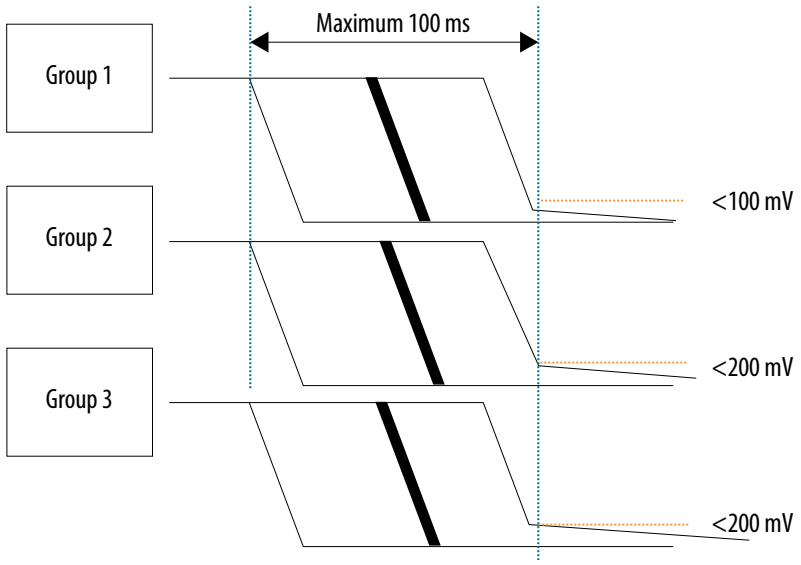
- To meet this voltage differential requirement, ramp down all power supplies as soon as possible according to the Required Power-Down Ramp Specification.

*Note:* Not following the required power sequence can result in unpredictable device operation and internal high current paths.

### Relaxed Power-Down Duration Specification

For supplies being powered down with no active termination, voltage reduction to GND slows down as supply approaches 0 V. In this case, the 100 ms power requirement is relaxed - measure it when supply reaches near GND.

**Figure 13. Relaxed Power-Down Duration Specification**




- Ensure all Group 1 supplies reach < 100 mV within 100 ms.
- Ensure all Group 2 and Group 3 supplies reach < 200 mV within 100 ms.

**Related Information**

AN692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices

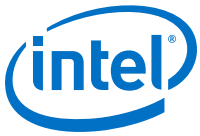
## 2.5. Power Supply Design

The power supply requirements for Intel Stratix 10 devices will vary depending on the static and dynamic power for each specific use case. The Enpirion portfolio of power management solutions, combined with comprehensive design tools, enable optimized Intel Stratix 10 device power supply design. The Enpirion portfolio includes power management solutions that are compatible with the multiple interface methods utilized by Intel Stratix 10 devices and designed to support Intel Stratix 10 power reduction features such as the SmartVID feature.

Intel Stratix 10 devices have multiple input voltage rails that require regulated power supplies for their operation. Multiple input rail requirements may be grouped according to system considerations such as voltage requirements, noise sensitivity, and sequencing. The *Intel Stratix 10 Device Family Pin Connection Guidelines* provides more detailed recommendations about which input rails may be grouped. The Early Power Estimator (EPE) tool for Intel Stratix 10 devices also provides input rail power requirements and specific device recommendations based on each specific Intel Stratix 10 use case. Individual input rail voltage and current requirements are summarized on the "Report" tab. Input rail groupings and specific power supply recommendations can be found on the "Report" and "Enpirion" tabs, respectively.

**Related Information**

- Intel Intel Enpirion® Power Solutions
  Provides more information about Intel's Power Management IC and PowerSoC solutions designed for powering FPGAs.



- Intel Stratix 10 Device Family Pin Connection Guidelines

# 3. Intel Stratix 10 Power Management and VID Interface Implementation Guide

The Intel Stratix 10 SDM Power Management Firmware manages the SmartVID configuration and enables the FPGA to power up before you can access the FPGA core. The Intel Stratix 10 device is connected to the external voltage regulator through the PMBus interface.

## 3.1. Intel Stratix 10 Power Management and VID Interface Getting Started

The Intel Stratix 10 Power Management and VID interface is installed as part of the Intel Quartus Prime software.

### 3.1.1. Specifying Parameters and Options

Follow these steps to specify the Power Management and VID parameters and options.

1. Create an Intel Quartus Prime project using the **New Project Wizard** available from the File menu.
2. On the **Assignments** menu, click **Device**.
3. On the **Device** dialog box, click **Device and Pin Options**.
4. On the **Device and Pin Options** dialog box, click **Configuration**.
5. On the **Configuration** page, specify the **VID Operation mode**. There are two modes available—PMBus Master and PMBus Slave.
6. The PMBus modes require these pins—PWMGT_SDA, PWMGT_SCL, and PWRMGT_ALERT. To configure these pins, on the **Configuration** page, click **Configuration Pin Options**. The PWRMGT_ALERT pin is only available and used in the slave mode. For the configuration pin parameters, refer to Table 7 on page 23.
7. On the **Configuration Pin** dialog box, assign the appropriate SDM_IO pin to the power management pins. Click **OK**.
8. On the **Device and Pin Options** dialog box, click **Power Management and VID** to specify the device settings if your device is in the PMBus Master mode. Click **OK**. For the power management and VID parameters, refer to Table 8 on page 23.

This completes the SmartVID setup for the Intel Stratix 10 device.

#### 3.1.1.1. Configuration Pin Parameters

You can configure the following power management pins using the GUI parameters.

**Table 7. Configuration Pin Parameters**

| Parameters | Value | Description |
|---|---|---|
| Use PWRMGT_SCL output | SDM_IO0<br>SDM_IO14 | This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode.<br>Disable this parameter for the non-SmartVID device.<br>Intel recommends using the SDM_IO14 pin for this parameter. |
| Use PWRMGT_SDA output | SDM_IO11<br>SDM_IO12<br>SDM_IO16 | This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode.<br>Disable this parameter for the non-SmartVID device.<br>Intel recommends using the SDM_IO11 pin for this parameter. |
| Use PWRMGT_ALERT output | SDM_IO0<br>SDM_IO12 | This is a required PMBus interface for the power management that is used only in the PMBus Slave mode.<br>Disable this parameter for the non-SmartVID device.<br>Intel recommends using the SDM_IO12 pin for this parameter. |

**Related Information**

- SDM Pin Mapping
  Provides more information on the configuration functions for each SDM pin.
- Secure Device Manager (SDM) Pins
  Provides more information on the pin description and connection guidelines for each SDM pin.

### 3.1.1.2. Power Management and VID Parameters

You can use the GUI parameters to configure the Power Management and VID interface if the VID operation is in the PMBus Master mode.

**Table 8. Power Management and VID Parameters**

| Parameters | Value | Description |
|---|---|---|
| Bus speed mode(8) | 100 KHz<br>400 KHz | Bus speed mode of PMBus interface when operating in the PMBus Master mode. |
| Slave device type(8) | LTM4677<br>Other | Supported device types. |
| Device address in PMBus Slave mode(9) | 7-bit hexadecimal value | Device address in the PMBus Slave mode. |
| Slave device_0 address(8) | 7-bit hexadecimal value | External power regulator address. |

*continued...*

(8) This parameter is used for the PMBus Master mode.

(9) This parameter is used for the PMBus Slave mode.

| Parameters | Value | Description |
|---|---|---|
| | | This parameter must be non-zero when you are using the PMBus Master mode. |
| Slave device_1 address[8] | 7-bit hexadecimal value | External power regulator address. |
| Slave device_2 address[8] | 7-bit hexadecimal value | External power regulator address. |
| Slave device_3 address[8] | 7-bit hexadecimal value | External power regulator address. |
| Slave device_4 address[8] | 7-bit hexadecimal value | External power regulator address. |
| Slave device_5 address[8] | 7-bit hexadecimal value | External power regulator address. |
| Slave device_6 address[8] | 7-bit hexadecimal value | External power regulator address. |
| Slave device_7 address[8] | 7-bit hexadecimal value | External power regulator address. |
| Voltage output format[8] | Auto discovery | The voltage output format when the operation mode is PMBus Master.<br>If the voltage output format is the Auto discovery or Direct format, you must set the following parameters:<br>• Direct format coefficient m<br>• Direct format coefficient b<br>• Direct format coefficient R<br>If the voltage regulator is the Linear format, you must set the Linear format N parameter. [10] |
| | Direct format | |
| | Linear format | |
| Direct format coefficient m[8] | Signed integer: -32768 to 32767 | Direct format coefficient m of the slave device type when the operation mode is PMBus Master. |
| Direct format coefficient b[8] | Signed integer: -32768 to 32767 | Direct format coefficient b of the slave device type when the operation mode is PMBus Master. |
| Direct format coefficient R[8] | Signed integer: -128 to 127 | Direct format coefficient R of the slave device type when the operation mode is PMBus Master. |
| Linear format N[8] | –16 to 15 | Output voltage command when the voltage output format is set to the Linear format. |
| Translated voltage value unit[8] | millivolts | Indicates the translated output voltage is in millivolts (mV) or volts (V). |
| | volts | |
| Enable PAGE command[8] | Enable | By enabling the PAGE command, the FPGA PMBus Master mode will use the PAGE command to set all the output channels on registered regulator modules to respond to VOUT_COMMAND. |
| | Disable | |

[10] N is the exponent of a 5-bit two's compliment integer.

# 4. Intel Stratix 10 Power Management User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

| IP Core Version | User Guide |
|---|---|
| 17.1 | Intel Stratix 10 Power Management User Guide |
| 18.0 | Intel Stratix 10 Power Management User Guide |

# 5. Document Revision History for the Intel Stratix 10 Power Management User Guide

| Document Version | Intel Quartus Prime Version | Changes |
|---|---|---|
| 2018.09.26 | 18.1 | • Updated the SmartVID details in the *Intel Stratix 10 Power Management Overview* section.<br>• Added the power-screened devices feature in the *Power Reduction Techniques and Features* section.<br>• Added the *Power-Screened Devices* section.<br>• Updated the SmartVID regulator requirements in the *SmartVID Standard Power Devices* section.<br>• Updated the *Power Sequencing Considerations for Intel Stratix 10 Devices* section.<br>• Updated the *Power-Up Sequence Requirements for Intel Stratix 10 Devices* section to provide more information on the Group 2 and Group3 power rails sharing.<br>• Updated the *PMBus Master Mode* and *PMBus Slave Mode* figures.<br>• Removed support for the Pulse-Width Modulation (PWM) mode. |
| 2018.05.07 | 18.0 | • Added the MFR_ADC_CONTROL command to the *Supported Commands for the PMBus Master Mode* table.<br>• Updated the *SmartVID* section to include information for the PWRMGT_SCL and PWRMGT_SDA pins.<br>• Updated the *Stage Flow for the External Power Management Controller in the PMBus Slave Mode* figure.<br>• Removed the *Monitor Stage for the External Power Management Controller in the PMBus Slave Mode* figure.<br>• Updated the description of the direct format equation in the *PMBus Slave Mode* section.<br>• Updated the *Power Supplies Monitored and Not Monitored by the Intel Stratix 10 POR Circuitry* table:<br>— Added the $V_{CCRT\_GXE}$ and $V_{CCRTPLL\_GXE}$ rails<br>— Removed the $V_{CC\_SDM}$ rail<br>• Editorial updates. |
| 2018.02.28 | 17.1 | • Added the Supported Commands for the PMBus Slave Mode table.<br>• Added a note about the PWRMGT_ALERT pin for the PMBus Slave mode in the PMBus Mode section.<br>• Added a note about the I/O standards supported in the PMBus mode in the PMBus Mode section.<br>• Added recommendation to connect to the PWRMGT_ALERT when configuring in the PMBus slave mode in the PMBus Slave Mode section.<br>• Added information on the multi-master mode in the PMBus Master Mode section.<br>• Added the direct format equation for the PMBus Slave Mode section.<br>• Added the Temperature Compensation for SmartVID for Intel Stratix 10 Devices figure.<br>• Updated the SmartVID section to change the nominal voltage to 0.9V.<br>• Updated the SmartVID Regulator Requirements table to update the values for the non-CvP and CvP ramp time. |

*continued...*

| Document Version | Intel Quartus Prime Version | Changes |
|---|---|---|
| | | • Updated the guidelines for the Power Sense Line section.<br>• Updated the Power Sequencing Considerations for Intel Stratix 10 Devices section.<br>• Updated the value of slave device addresses in the Power Management and VID Parameters table.<br>• Updated the steps in the Specifying Parameters and Options section.<br>• Updated the SDM Power Manager section to include the initial/ shutdown and monitor stages.<br>• Removed the Temperature Compensation for SmartVID for Intel Stratix 10 Devices table. |

| Date | Version | Changes |
|---|---|---|
| May 2017 | 2017.05.08 | • Updated the PowerPlay Early Power Estimator (EPE) to Early Power Estimator.<br>• Updated the Power Consumption section to include the standby power.<br>• Updated the Power Reduction Techniques section.<br>• Updated the SmartVID section to change the nominal voltage to 0.89V.<br>• Updated the SmartVID Feature Implementation in Stratix 10 Devices section.<br>• Updated the SDM Power Management section.<br>• Updated the PMBus Mode section.<br>• Updated the PWM Mode section.<br>• Updated the Temperature Compensation section.<br>• Updated the DSP and M20K Power Gating section.<br>• Updated the Clock Gating section.<br>• Updated the Power Sense Line section.<br>• Updated the Power-On Reset Circuitry section.<br>• Updated the Power-Up and Power-Down Sequences section.<br>• Updated the Using the SmartVID Feature on $V_{CC}$ and $V_{CCP}$ Rails section.<br>• Updated the Power Supply Design section.<br>• Updated the Specifying Parameters and Options section.<br>• Added the Temperature Compensation for SmartVID for Stratix 10 Devices table.<br>• Updated the CvP's ramp time in the SmartVID Regulator Requirements table.<br>• Updated the Power Supplies Monitored and Not Monitored by the Stratix 10 POR Circuitry table to include the HPS power supplies.<br>• Updated the Power Groups Ramping Sequence table.<br>• Updated the Configuration Pin Parameters table.<br>• Updated the Power Management and VID Parameters table.<br>• Updated the Configuration Pin Parameters table.<br>• Updated the Power Management and VID Parameters table.<br>• Updated the SDM Power Management Block Diagram figure.<br>• Updated the PMBus Master Mode figure.<br>• Updated the PMBus Slave Mode figure.<br>• Updated the Power-Up and Power-Down Sequences Requirement for Stratix 10 Devices figure. |
| October 2016 | 2016.10.31 | Initial release. |