SCOPE: IMPROVED 8-CHANNEL/DUAL 4-CHANNEL CMOS ANALOG MULTIPLEXER

Device Type	Generic Number	Circuit Function
01	DG408A(x)/883B	8-Channel Analog Multiplexer
02	DG409A(x)/883B	Dual 4-Channel Analog Multiplexer

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
K	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
L	CDFP4-F16	16 LEAD FLATPACK	F16
Z	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V^-
- V^+ to V^- ..... -0.3V, 44V
- V^- to GND ..... -0.3V, 25V
- Digital Inputs, S, D 1/ .....(V^-) -2V to (V^+)+2V or 30mA whichever occurs first
- Continuous Current, Any terminal 30mA
- Peak Current, S or D (Pulsed at 1ms, 10% duty cycle max) 100mA

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 lead FLATPACK (derate 6.1mW/°C above +70°C) 485mW
16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW
20 lead LCC (derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
- Case Outline 16 lead FLATPACK ..... 65°C/W
- Case Outline 16 lead CERDIP..... 50°C/W
- Case Outline 20 lead LCC ..... 20°C/W

Thermal Resistance, Junction to Ambient, ΘJA:
- Case Outline 16 lead FLATPACK ..... 165°C/W
- Case Outline 16 lead CERDIP..... 100°C/W
- Case Outline 20 lead LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V^+) ..... +15V
Negative Supply Voltage (V^-) ..... -15V
V_{AL} (max) 0.8V
V_{AH} (min) 2.4V

1/ Signals on SX, DX, EN, A0, A1, A2 exceeding V+ or V- will be clamped by internal diodes. Limit forward current to the maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS: DUAL SUPPLIES

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{AH}=+2.4V, V_{AL}=+0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	NOTE 3	1,2,3	All	-15	15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S =-1.0mA, V_D=±10V	1 2,3	All		100 125	Ω
On-resistance Matching between Channels	$\Delta r_{DS(ON)}$	I_S =-10mA, V_D=±10V NOTE 4	1 2,3	All		8 10	Ω
On-resistance Flatness	r_{FLAT}	I_S =-10mA, V_D=±5V or 0V	1 2,3	All		9 12	Ω
Source- Off Leakage Current	$I_{S(OFF)}$	V_D=±10V V_S =±10V, V_{EN}=0V	1 2,3	All	-0.5 -50	0.5 50	nA
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S =±10mA, VD=±10V, V_{EN}=0V	1 2,3	01	-1.0 -100	1.0 100	nA
			1 2,3	02	-1.0 -50	1.0 50	
Drain-On Leakage Current	$I_{D(ON)}$	V_D =V_S=±10V, sequence each switch on	1 2,3	01	-1.0 -100	1.0 100	nA
			1 2,3	02	-1.0 -50	1.0 50	
INPUT							
Input Current/Voltage High	I_{AH}	V_{IN}= 2.4V, 15V	1,2,3	All	-1.0	1.0	µA
Input Current/Voltage Low	I_{AL}	V_{EN}=0V, 2.4V; V_A=0V	1,2,3	All	-1.0	1.0	µA
SUPPLY							
Power Supply Range			1,2,3	All	±4.5	±20	V
Positive Supply Current	I+	V_{EN}=V_A=0V or 4.5V	1 2,3	All		30 75	µA
		V_{EN}=2.4V, $V_{A(ALL)}$=0V or 2.4V	1 2,3	All		0.5 2.0	mA
Negative Supply Current	I-	V_{EN}=2.4V, $V_{A(ALL)}$=0V or 2.4V	1 2,3	All	-1 -10	1 10	µA
DYNAMIC							
Transition Time	t_{TRANS}	Figure 2	9 10,11	All		175 250	ns
Break-Before-Make interval	t_{OPEN}	Figure 4	9	All	10		ns

TABLE 1. ELECTRICAL TESTS: DUAL SUPPLIES

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{AH}=+2.4V, V_{AL}=+0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3	9 10,11	All		150 225	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	9 10,11	All		150 300	ns
Charge Injection	Q	Figure 5, NOTE 3	9	ALL		15	pC

TABLE 1. ELECTRICAL TESTS: SINGLE SUPPLY

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+12V, V^-=0V, GND=0V V_{AH}=+2.4V, V_{AL}=+0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 2/	Limits Max 2/	Units
SWITCH							
Analog Signal Range	V_{ANALOG}	NOTE 3	1,2,3	All	0	12	V
Drain-Source On-Resistance	$r_{DS(ON)}$	I_S=-1.0mA, V_D=3V or 10V	1	All		175	Ω
DYNAMIC							
Transition Time NOTE 3	t_{TRANS}	V_{S1}=8V, V_{S8}=0V, V_A=0V, Figure 2	9	All		450	ns
Enable Turn-On Time NOTE 3	$t_{ON(EN)}$	V_{AL}=0V, V_{S1}=5V, Figure 3	9	All		600	ns
Enable Turn-Off Time NOTE 3	$t_{OFF(EN)}$	V_{AL}=0V, V_{S1}=5V, Figure 3	9	All		300	ns

NOTE 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

NOTE 3: Guaranteed by design.

NOTE 4: $\Delta r_{DS(ON)} = r_{DS(ON)max} - r_{DS(ON)min}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

FIGURE 2: Transition Time Diagrams: See Commercial Data Sheet
FIGURE 3: Enable Switching Time Diagrams: See Commercial Data Sheet
FIGURE 4: Break-Before-Make Interval Diagrams: See Commercial Data Sheet
FIGURE 5: Charge Injection Diagrams: See Commercial Data Sheet

ORDERING INFORMATION:	
DG408AL/883B 16 FLATPACK	DG409AL/883B 16 FLATPACK
DG408AK/883B 16 CDIP	DG409AK/883B 16 CDIP
DG408AZ/883B 20 LCC	DG409AZ/883B 20 LCC

TRUTH TABLE

A2	A1	A0	EN	DG408A ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
				DG409
	A1	**A0**	**EN**	**ON SWITCH**
	X	X	0	None
	0	0	1	1
	0	1	1	2
	1	0	1	3
	1	1	1	4

TERMINAL CONNECTION

TERMINAL NUMBER	01 DG408A	01 DG408A	02 DG409A	02 DG409A
	F16 & J16	20LCC	F16 & J16	20LCC
1	A0	NC	A0	NC
2	EN	A0	EN	A0
3	V-	EN	V-	EN
4	S1	V-	S1a	V-
5	S2	S1	S2a	S1a
6	S3	NC	S3a	NC
7	S4	S2	S4a	S2a
8	D	S3	Da	S3a
9	S8	S4	Db	S4a
10	S7	D	S4b	Da
11	S6	NC	S3b	NC
12	S5	S8	S2b	Db
13	V+	S7	S1b	S4b
14	GND	S6	V+	S3b
15	A2	S5	GND	S2b
16	A1	NC	A1	NC
17		V+		S1b
18		GND		V+
19		A2		GND
20		A1		A1

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.