CY62136FV30 MoBL®

2-Mbit (128 K × 16) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
  - Automotive-E: –40 °C to +125 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62136V, CY62136CV30/CV33, and CY62136EV30
- Ultra low standby power
  - Typical standby current: 1 μA
  - Maximum standby current: 5 μA (Industrial)
- Ultra low active power
  - Typical active current: 1.6 mA at f = 1 MHz (45 ns speed)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP) II packages

Functional Description

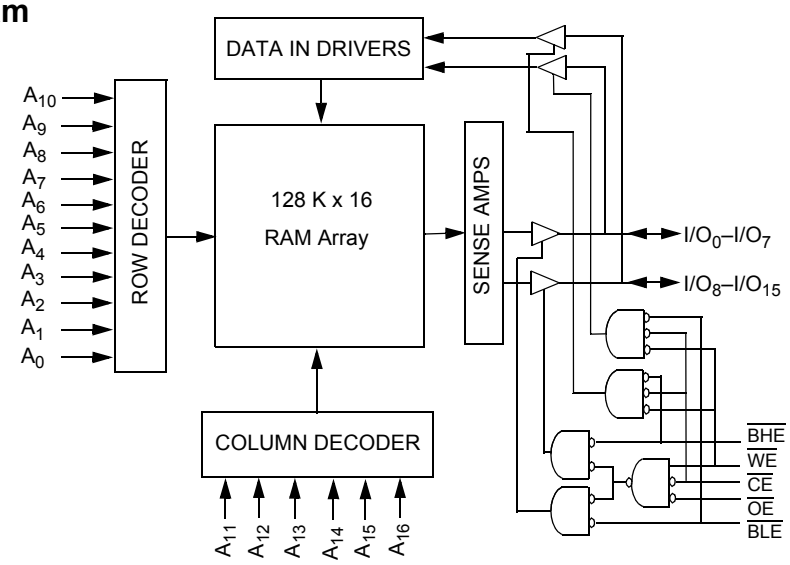
The CY62136FV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 90 percent when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related resources, click here.

Logic Block Diagram



Contents

Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62136FV30LL	Industrial/Auto-A	2.2	3.0	3.6	45	1.6	2.5	13	18	1	5
	Auto-E	2.2	3.0	3.6	55	2	3	15	25	1	20

Pin Configuration

Figure 1. 48-ball VFBGA pinout [2, 3]

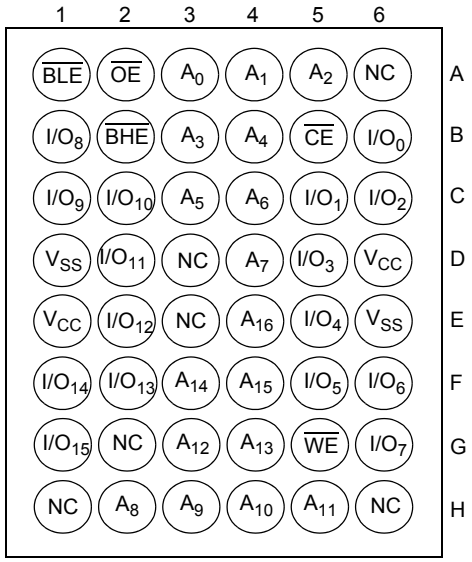
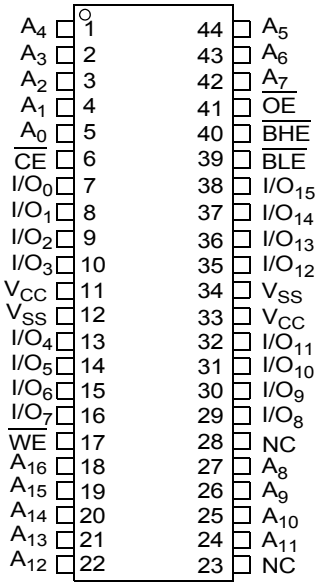


Figure 2. 44-pin TSOP II pinout [2]



Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, H6 and H3 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential [4, 5] ... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC voltage applied to outputs in High Z State [4, 5] ..... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

DC input voltage [4, 5] ..... –0.3 V to 3.9 V ($V_{CC(max)}$ + 0.3 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[6]
CY62136FV30LL	Industrial/ Auto-A	–40 °C to +85 °C	2.2 V to 3.6 V
	Auto-E	–40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-45 (Industrial/Auto-A)			-55 (Auto-E)			Unit
				Min	Typ [7]	Max	Min	Typ [7]	Max	
V_{OH}	Output high voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	2.4	–	–	V
V_{OL}	Output low voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
V_{IH}	Input high voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input low voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.8	–0.3	–	0.8	V
I_{IX}	Input leakage current	$GND \le V_I \le V_{CC}$		–1	–	+1	–4	–	+4	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output disabled		–1	–	+1	–4	–	+4	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$	–	13	18	–	15	25	mA
		f = 1 MHz	I_{OUT} = 0 mA CMOS levels	–	1.6	2.5	–	2	3	
I_{SB1}[8]	Automatic CE power down current — CMOS inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V, $V_{IN} \le$ 0.2 V, f = f_{max} (Address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$), V_{CC} = 3.60 V		–	1	5	–	1	20	µA
I_{SB2} [8]	Automatic CE power down current — CMOS inputs	$\overline{CE} \ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	5	–	1	20	µA

Notes

4. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$=V_{CC} + 0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Capacitance

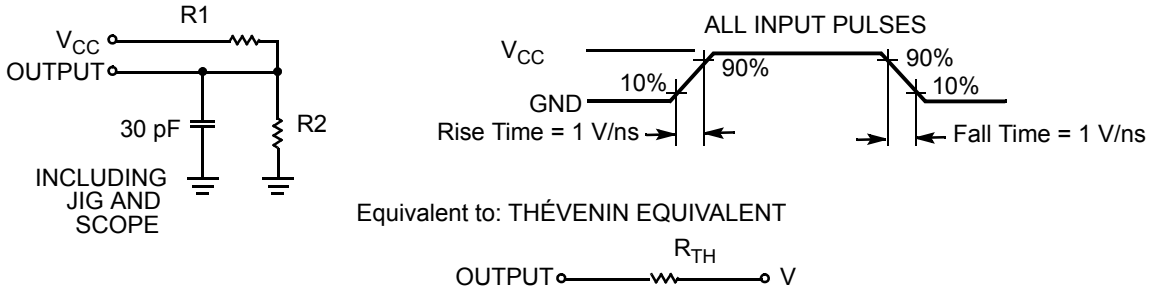
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board	75	77	°C/W
Θ_{JC}	Thermal resistance (junction to case)		10	13	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
9. Tested initially and after any design or process changes that may affect these parameters.

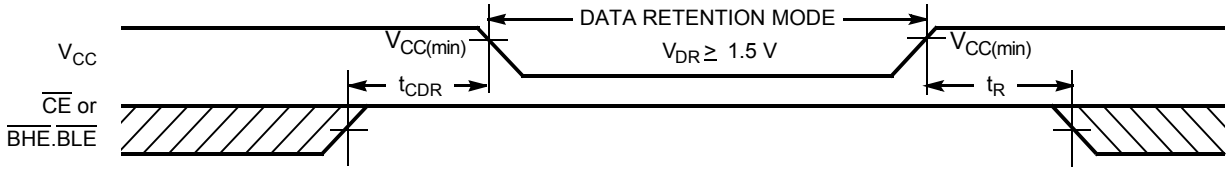
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 1.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial/ Automotive-A	–	–	4	µA
			Automotive-E	–	–	12	
t_{CDR} [12]	Chip deselect to data retention time			0	–	–	ns
t_R [13]	Operation recovery time		CY62136FV30LL-45	45	–	–	ns
			CY62136FV30LL-55	55	–	–	

Data Retention Waveform

Figure 4. Data Retention Waveform [14]



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1}/ I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [15, 16]	Description	-45 (Industrial/Automotive-A)		-55 (Automotive-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [17]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [17, 18]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [17]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [17, 18]	–	18	–	20	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	45	–	55	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	22	–	25	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to low Z [17]	5	–	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to high Z [17, 18]	–	18	–	20	ns
Write Cycle [19, 20]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data Hold From Write End	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [17, 18]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [17]	10	–	10	–	ns

Notes

15. Test conditions for all parameters other than tristate parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 3 on page 5.
16. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production. .
17. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
18. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals are ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.
20. The minimum write cycle pulse width for Write Cycle No. 3 and Write Cycle No. 4 should be equal to the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No.1: Address Transition Controlled [21, 22]

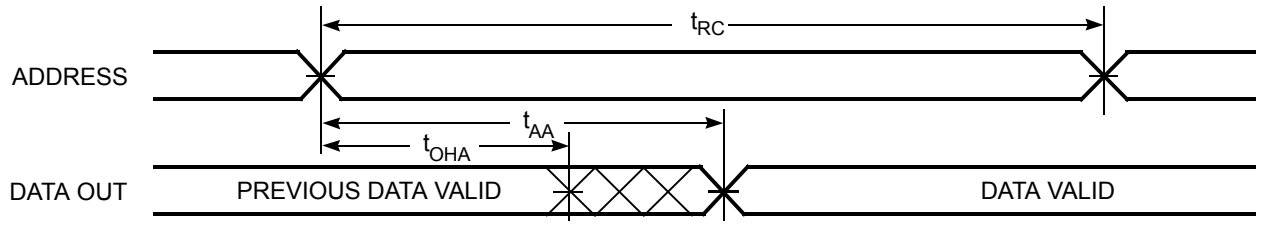
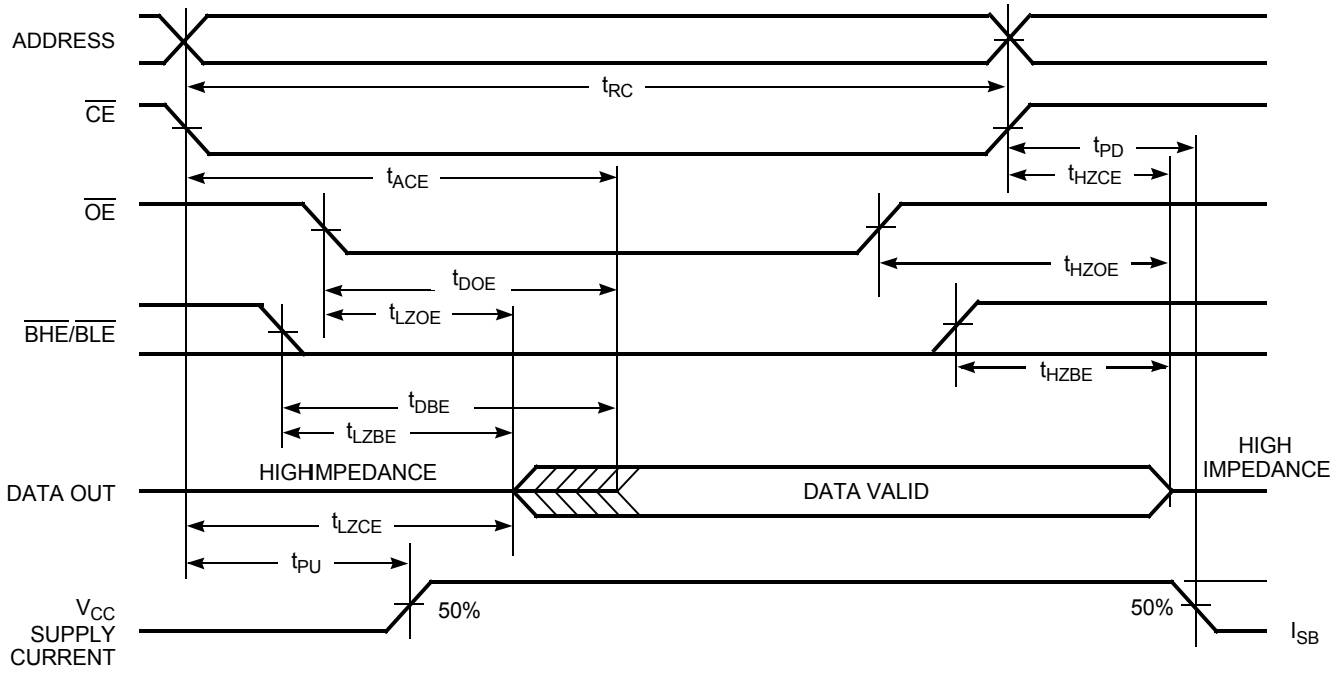


Figure 6. Read Cycle No. 2: $\overline{OE}$ Controlled [22, 23]



Notes
21. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and $\overline{BLE}$ = V_{IL}.
22. $\overline{WE}$ is HIGH for read cycle.
23. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No 1: $\overline{WE}$ Controlled [24, 25, 26]

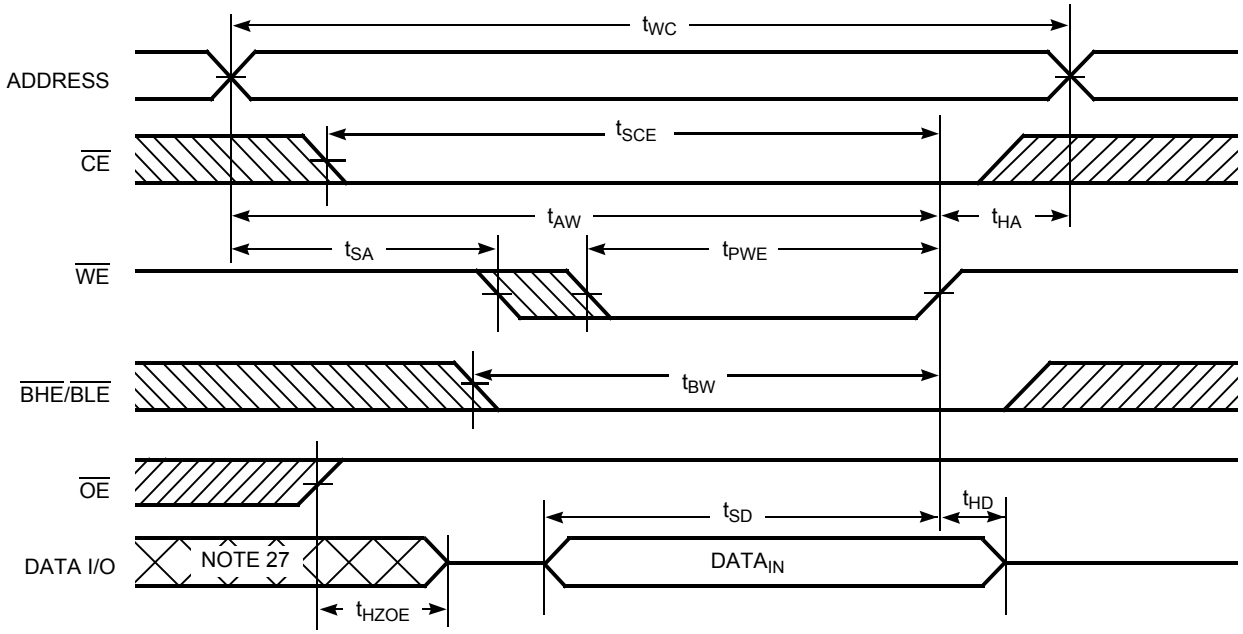
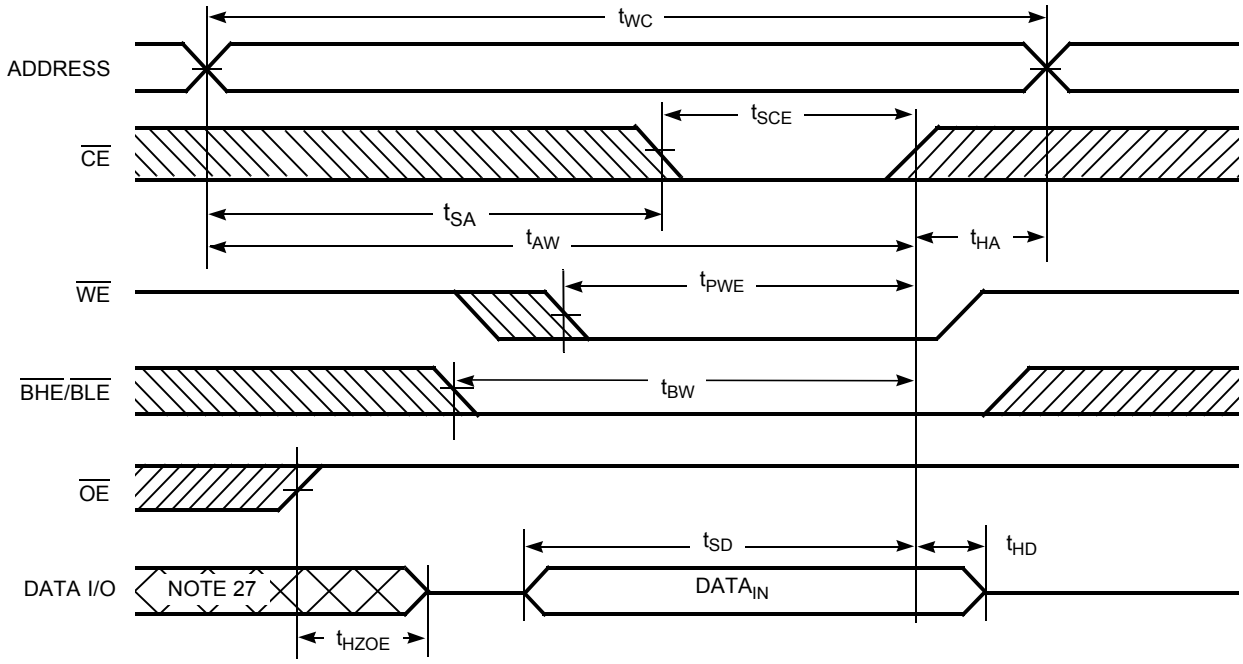


Figure 8. Write Cycle 2: $\overline{CE}$ Controlled [24, 25, 26]



Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle 3: $\overline{WE}$ controlled, $\overline{OE}$ LOW [28, 29]

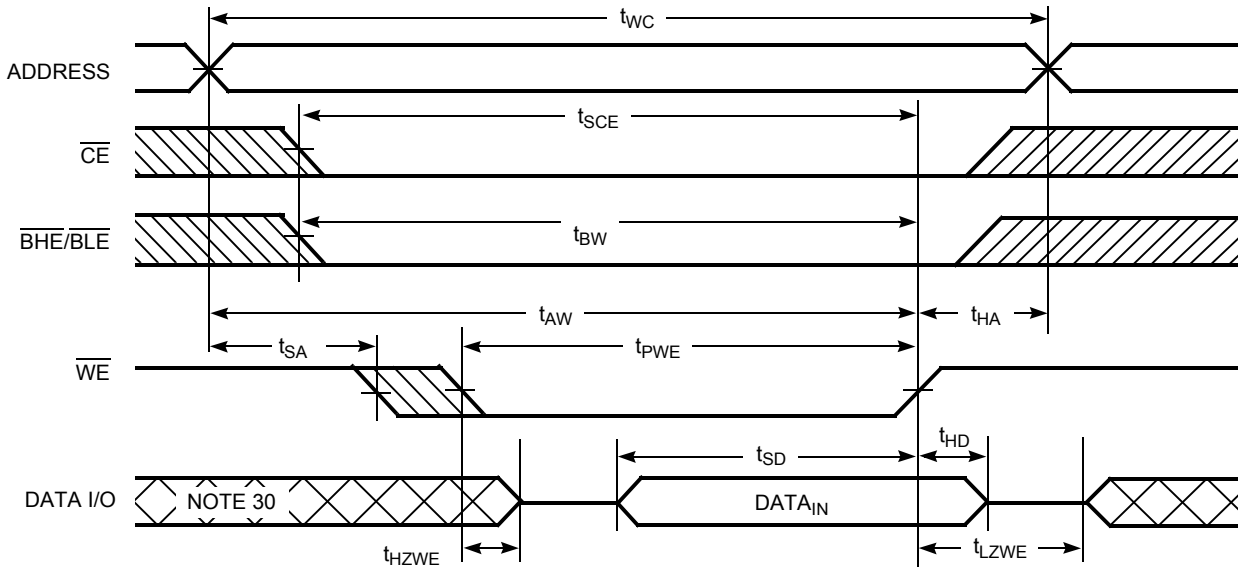
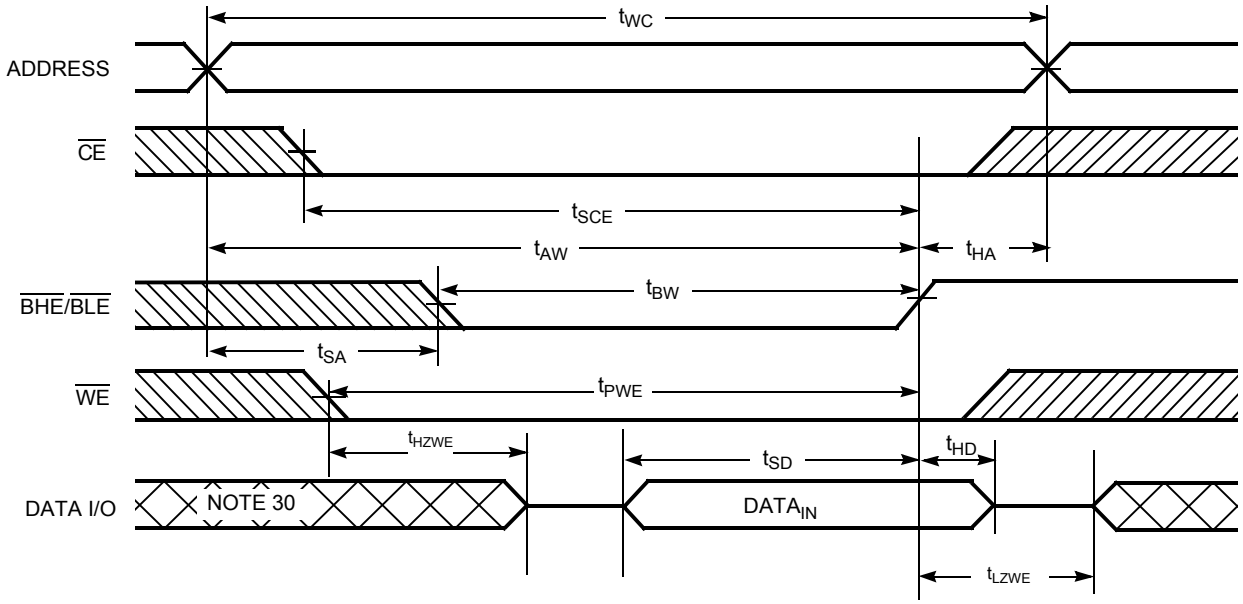


Figure 10. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW [28, 29]



Notes
28. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
29. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.
30. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs or Outputs	Mode	Power
H	X	X	X[31]	X[31]	High Z	Deselect or power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	X	X	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

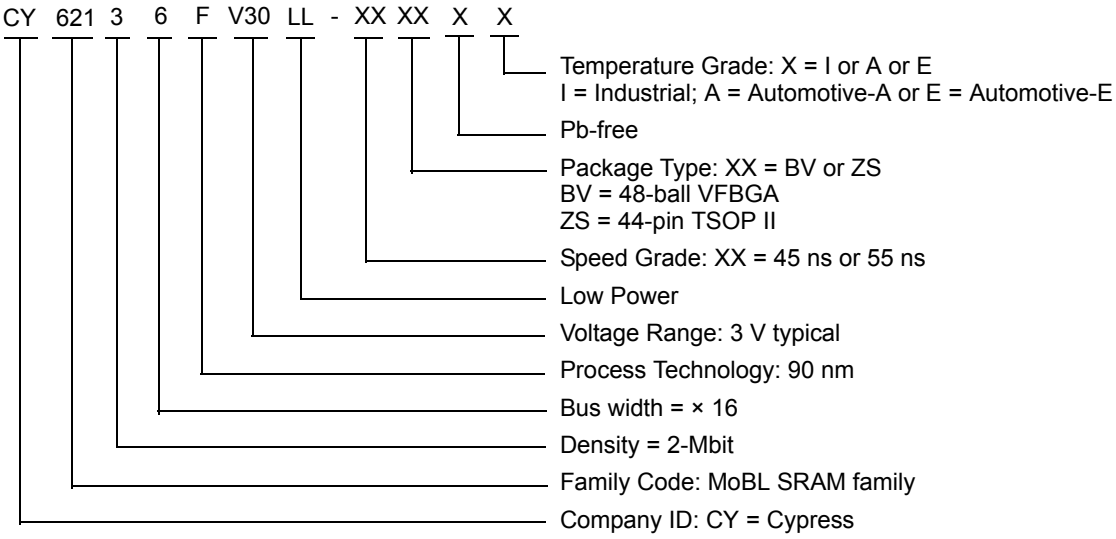
Note
31. The 'X' (Don't care) state for the Chip enable ($\overline{CE}$) and Byte enables ($\overline{BHE}$ and $\overline{BLE}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136FV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62136FV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	
	CY62136FV30LL-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
55	CY62136FV30LL-55ZSXE	51-85087	44-pin TSOP II (Pb-free)	Automotive-E

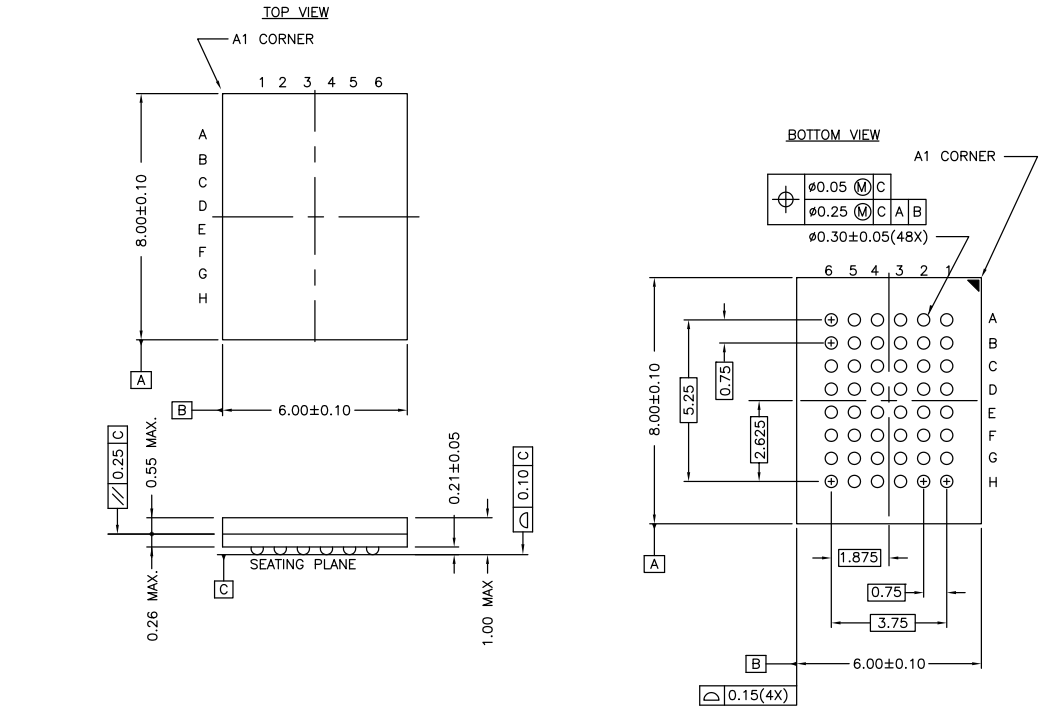
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

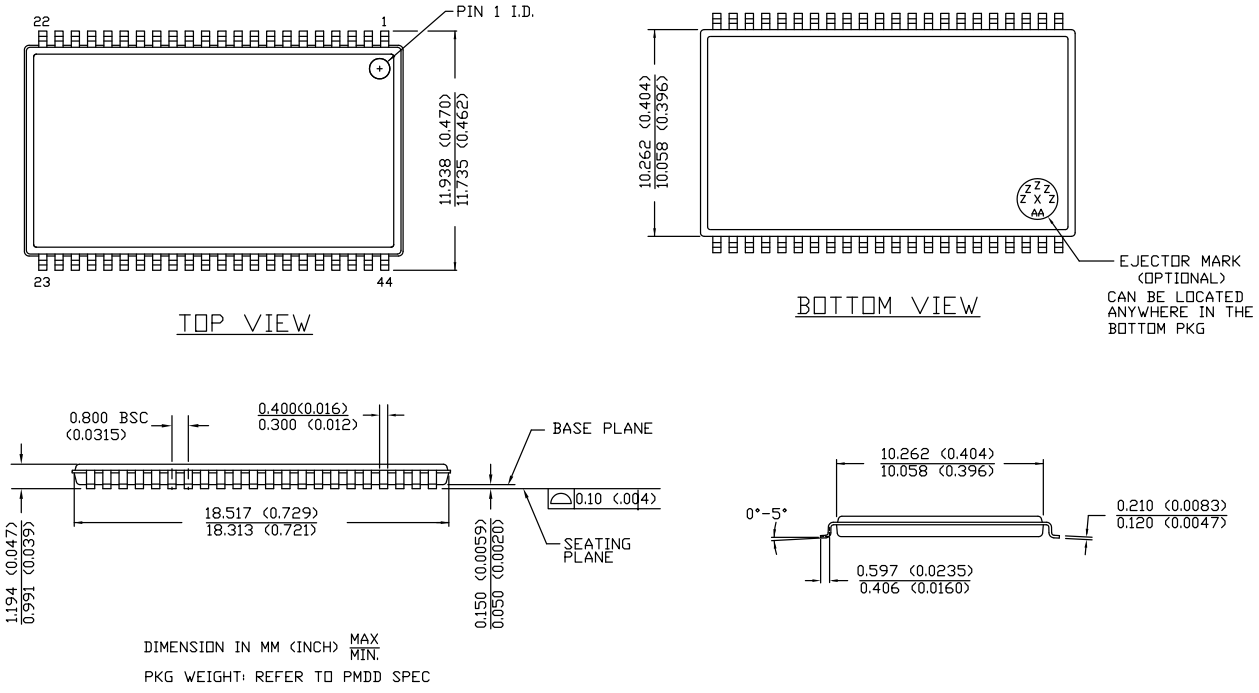


NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
%	percent
pF	picofarad
Ω	ohm
V	volt
W	watt

Document History Page

Document Title: CY62136FV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 001-08402				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	467351	See ECN	NXR	New data sheet.
*A	797956	See ECN	VKN	Changed status from Preliminary to Final. Updated Features: Changed value of Typical standby current from 0.5 µA to 1.0 µA. Changed value of Maximum standby current from 2.5 µA to 5.0 µA. Updated Electrical Characteristics: Changed maximum value of I_{CC} parameter corresponding to Test Condition "f = 1 MHz" from 2.25 µA to 2.5 µA. Changed typical value of I_{SB1} parameter from 0.5 µA to 1.0 µA. Changed maximum value of I_{SB1} parameter from 2.5 µA to 5.0 µA. Changed typical value of I_{SB2} parameter from 0.5 µA to 1.0 µA. Changed maximum value of I_{SB2} parameter from 2.5 µA to 5.0 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 0.5 µA to 1.0 µA. Changed maximum value of I_{CCDR} parameter from 2.5 µA to 4.0 µA.
*B	869500	See ECN	VKN	Added Automotive Temperature Grade related information in all instances across the document. Updated Switching Characteristics: Added Note "Access time parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. Please see application note AN3842 for further clarification." and referred the same in t_{ACE} parameter. Updated Ordering Information.
*C	901800	See ECN	VKN	Updated Electrical Characteristics: Added Note 8 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 11 and referred the same note in I_{CCDR} parameter. Updated Switching Characteristics: Removed Note from t_{ACE} parameter and added the same note in "Parameters" column with some updates (Replaced Access time parameters with AC parameters in the note).
*D	1371124	See ECN	VKN / AESA	Changed status of Automotive information from Preliminary to Final (Removed shades). Updated Electrical Characteristics: Changed minimum value of I_{IX} parameter corresponding to 55 ns speed bin from –1 µA to –4 µA. Changed maximum value of I_{IX} parameter corresponding to 55 ns speed bin from +1 µA to +4 µA. Changed minimum value of I_{OZ} parameter corresponding to 55 ns speed bin from –1 µA to –4 µA. Changed maximum value of I_{OZ} parameter corresponding to 55 ns speed bin from +1 µA to +4 µA. Updated Switching Characteristics: Changed maximum value of t_{DBE} parameter corresponding to 55 ns speed bin from 55 ns to 25 ns.
*E	2594937	10/22/08	NXR / PYRS	Added Automotive-A Temperature Grade related information in all instances across the document. Updated Switching Characteristics: Changed minimum value of t_{LZBE} parameter corresponding to 55 ns speed bin from 10 ns to 5 ns.
*F	2675375	03/17/2009	VKN / PYRS	Updated Product Portfolio: Corrected typo (Replaced µA with mA for unit of Standby I_{SB2}).

Document History Page (continued)

Document Title: CY62136FV30 MoBL®, 2-Mbit (128 K × 16) Static RAM Document Number: 001-08402				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*G	2882113	02/19/2010	VKN / AESA	Updated Truth Table: Corrected typo. Updated Package Diagrams.
*H	2943752	06/03/2010	VKN	Updated Truth Table: Added footnote related to Chip enable and Byte enables. Updated Package Diagrams.
*I	3055169	10/12/2010	RAME	Updated all foot notes from table notes. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated Package Diagrams.
*J	3263825	06/17/2011	RAME	Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Data Retention Characteristics (Minimum value of t_R parameter). Updated to new template.
*K	3376161	09/19/2011	RAME	No technical updates. Completing Sunset Review.
*L	4102266	08/22/2013	VINI	Updated Switching Characteristics: Updated Note 16. Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*M	4581648	11/27/2014	VINI	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Maximum Ratings: Referred Notes 4, 5 in “Supply voltage to ground potential”.
*N	4989003	10/27/2015	NILE	Updated Switching Characteristics: Added Note 20 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 29 and referred the same note in Figure 9 and Figure 10. Updated Truth Table. Updated to new template. Completing Sunset Review.

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