IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

BT150S-600R

SCR

1 November 2016 **Product data sheet**

1. General description

Planar passivated SCR with sensitive gate in a TO252 (DPAK) surface mountable plastic package. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- General purpose switching
- Protection Circuits

4. Quick reference data

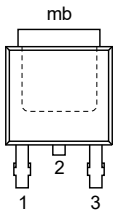
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 1		-	-	2.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 2; Fig. 3		-	-	4	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	-	35	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	-	38	A
T_j	junction temperature		[2]	-	-	125	°C
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; $T_j = 25$ °C; Fig. 7		-	15	200	µA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402$ V; $T_j = 125$ °C; $R_{GK} = 100$ Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		-	50	-	V/µs

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.
[2] Operation above 110˚C may require the use of a gate to cathode resistor of 1kΩ or less.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 DPAK (TO252N)	
2	A	anode[1]		
3	G	gate		
mb	A	mounting base; connected to anode		

[1] It is not possible to connect to pin 2 of the TO252 package.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT150S-600R	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	TO252N

7. Marking

Table 4. Marking codes

Type number	Marking code
BYV10ED-600P	BYV10ED-600P

8. Limiting values

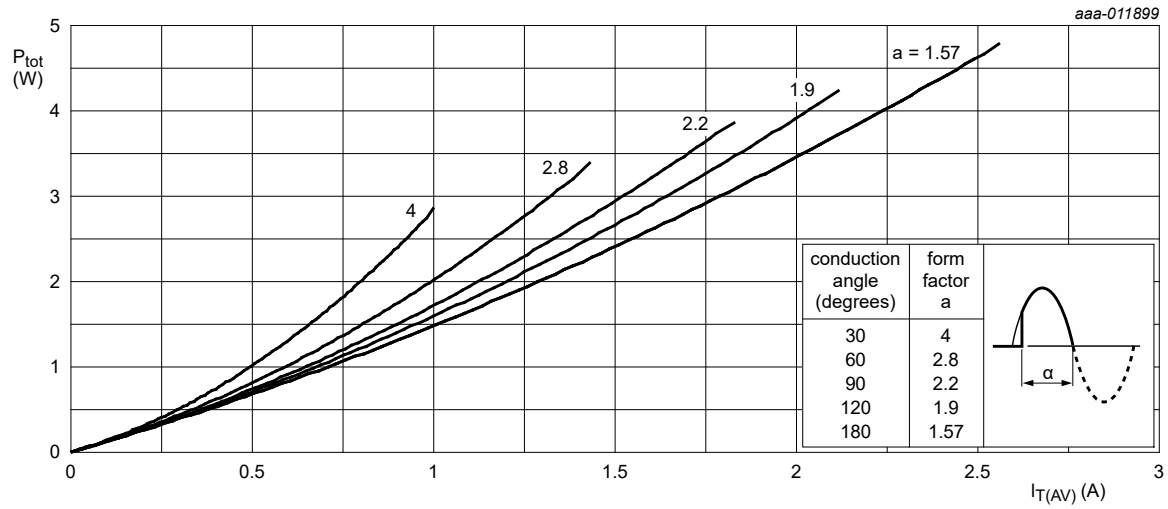
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V_{RRM}	repetitive peak reverse voltage			-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 1		-	2.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 2; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	35	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	38	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	6.1	A²s
dI_T/dt	rate of rise of on-state current	$I_T = 10$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature		[2]	-	125	°C

[1] Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.

[2] Operation above 110˚C may require the use of a gate to cathode resistor of 1kΩ or less.



α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

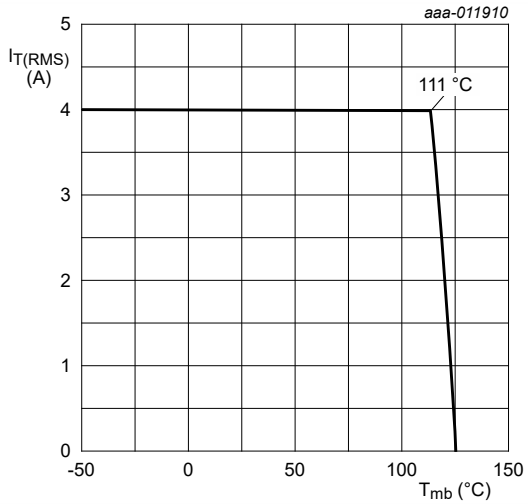
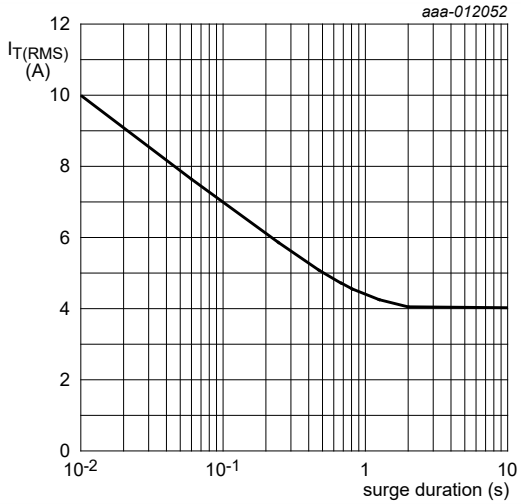
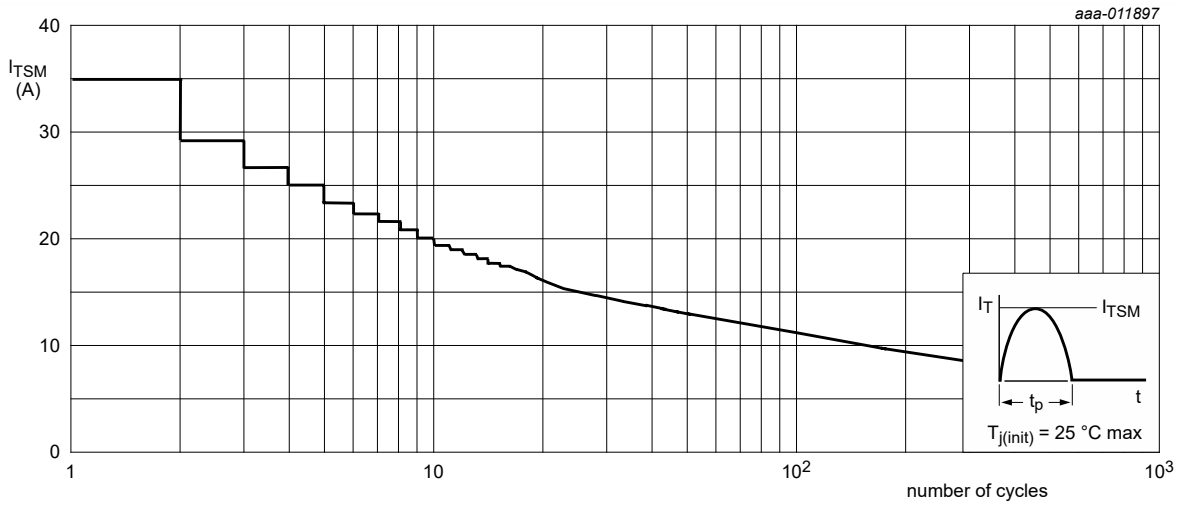


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



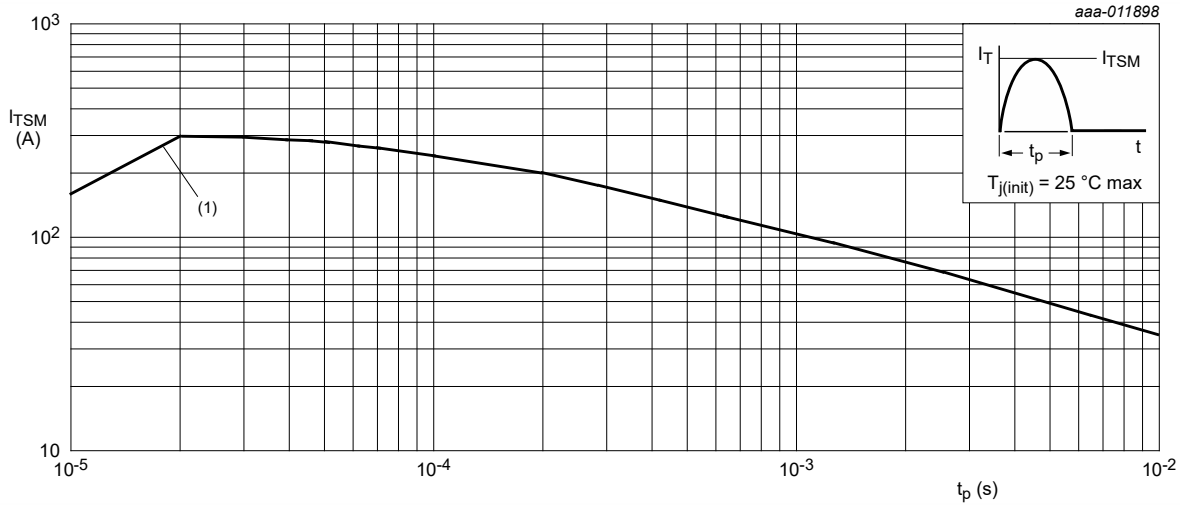
f = 50 Hz; T_{mb} = 111 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint		-	75	-	K/W

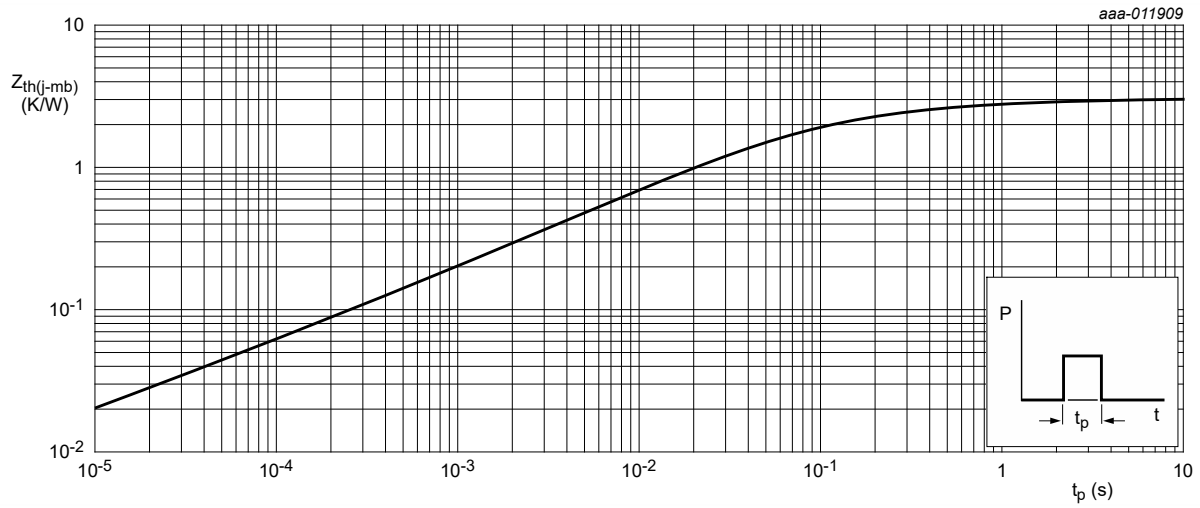


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	15	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	0.17	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	0.1	6	mA
V_T	on-state voltage	I_T = 5 A; T_j = 25 °C; Fig. 10		-	1.23	1.8	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.4	1	V
		V_D = 600 V; I_T = 0.1 A; T_j = 110 °C; Fig. 11		0.1	0.2	-	V
I_D	off-state current	V_D = 600 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 600 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		-	50	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 10 A; V_D = 600 V; I_G = 5 mA; dI_G/dt = 0.2 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 402 V; T_j = 125 °C; I_{TM} = 8 A; V_R = 10 V; $(dI_T/dt)_M$ = 10 A/µs; dV_D/dt = 2 V/µs; $R_{GK(ext)}$ = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

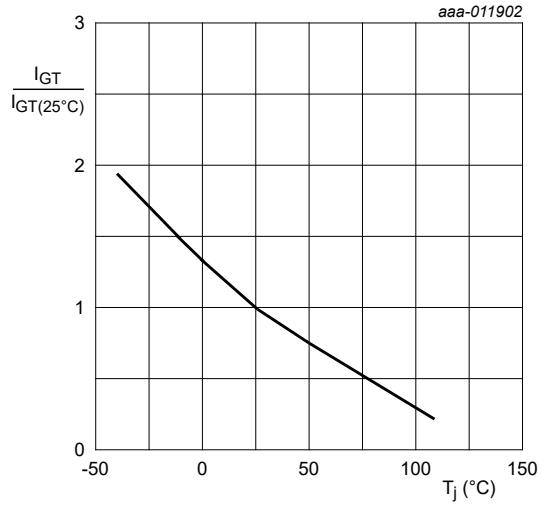
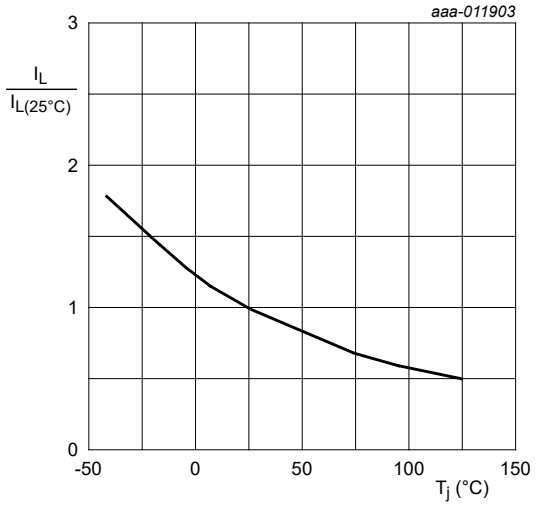
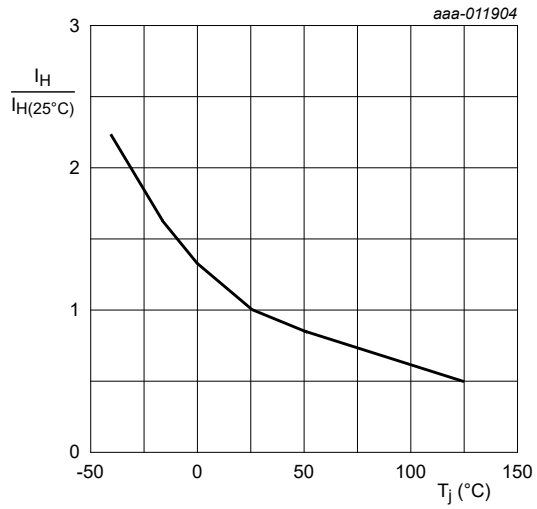


Fig. 7. Normalized gate trigger current as a function of junction temperature



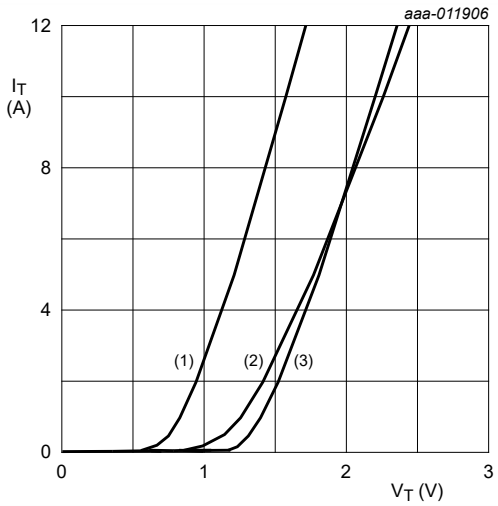
R_{GK} = 1 kΩ

Fig. 8. Normalized latching current as a function of junction temperature



R_{GK} = 1 kΩ

Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.26 V; R_s = 0.099 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

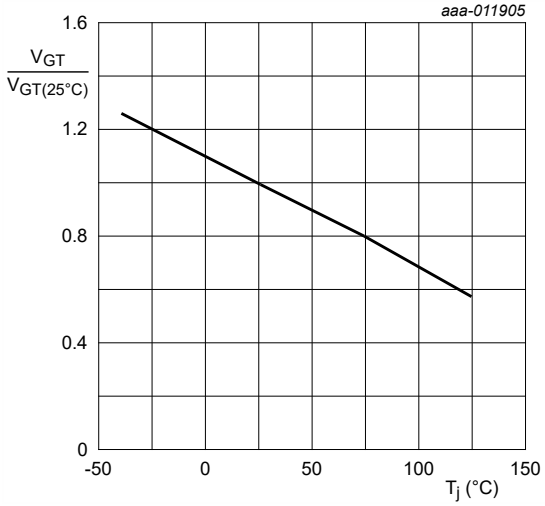
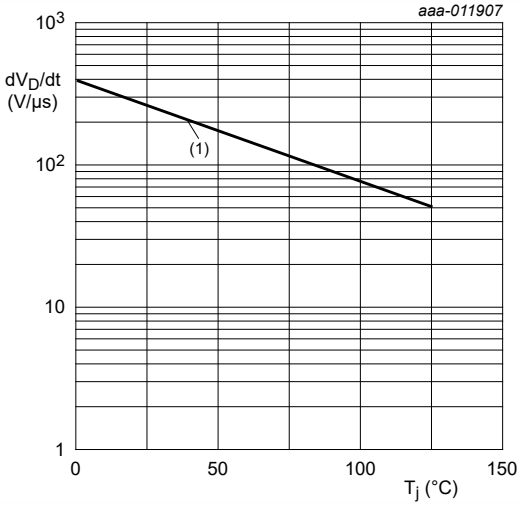


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

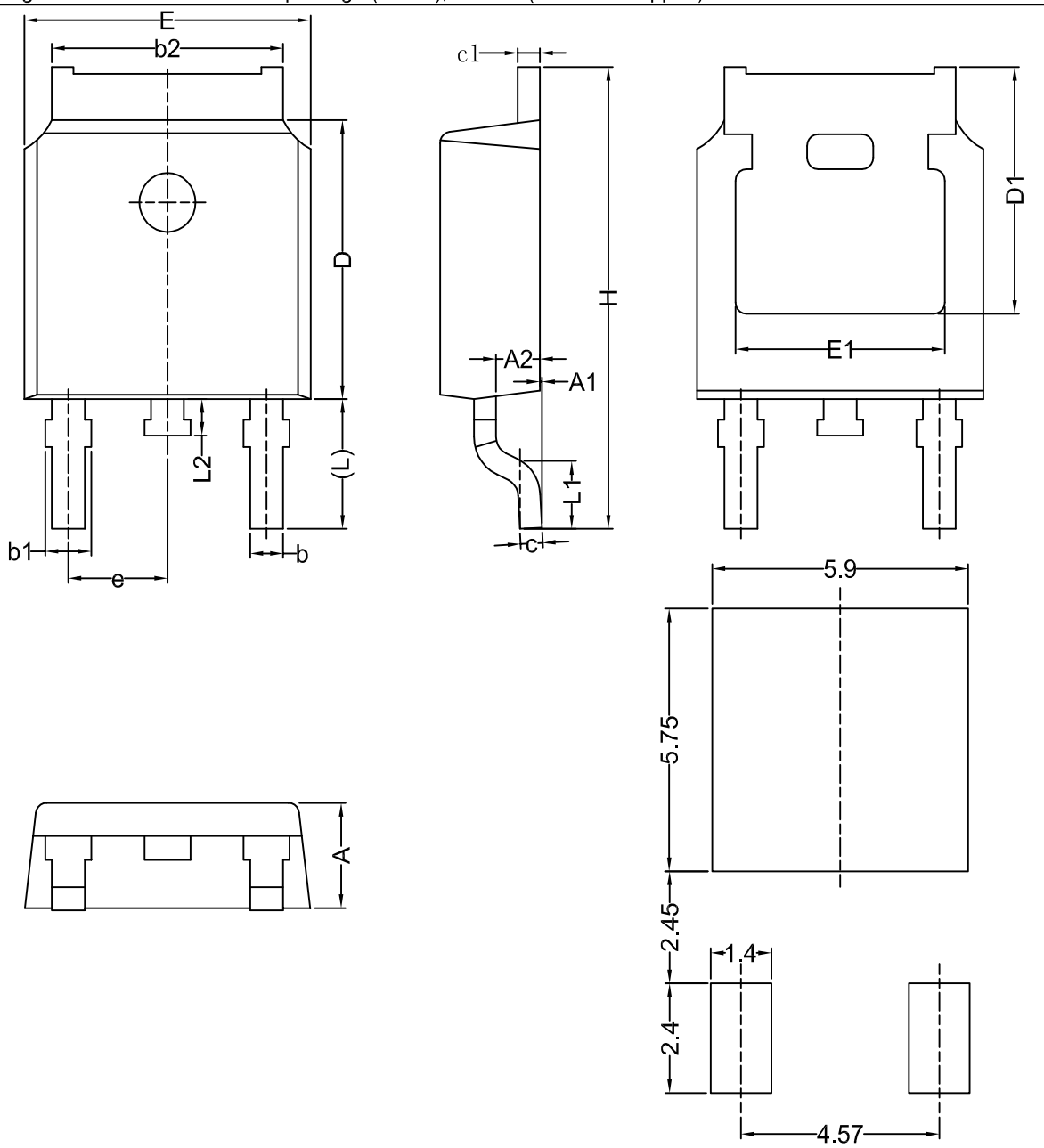


(1) R_{GK} = 100 Ω

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

11. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252



Unit	A	A1	A2	b	b1	b2	c	c1	D	D1	e	E	E1	H	L	L1	L2
min	2.20	0.00	0.90	0.71	0.72	5.00	0.20	0.46	5.98	5.25	2.285 (typ.)	6.47	4.45	9.60	2.90 (Ref.)	0.50	0.50
max	2.38	0.10	1.10	0.89	1.10	5.46	0.56	0.93	6.22	---		6.73	---	10.40		---	0.90

Fig. 13. Package outline DPAK (TO252N)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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13. Contents

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Date of release: 1 November 2016