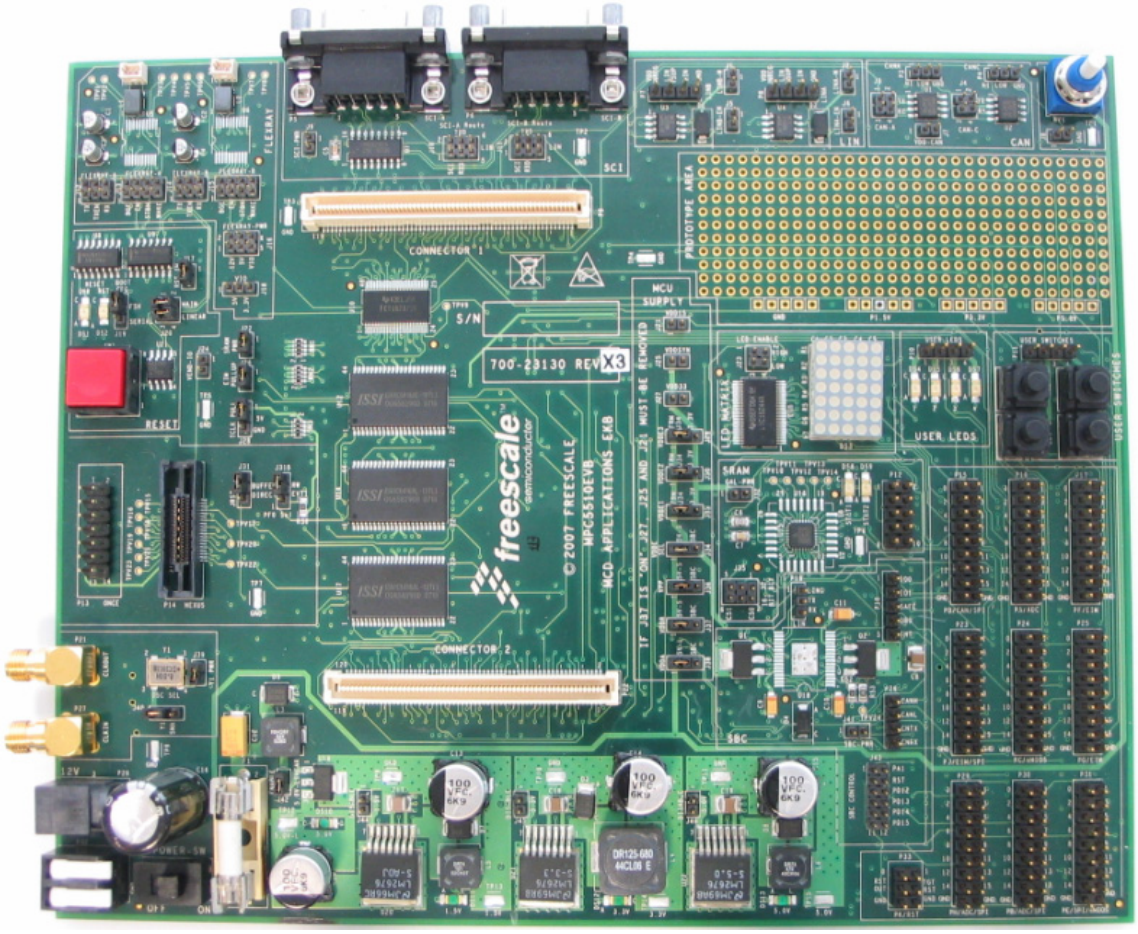

MPC5510EVB User Manual

Revision 1.0 – September 2007

Note – This user manual is written for EVB PCB revision E

Revision History:

Revision	Date	Author	Comment
0.1	March 2007	A. Robertson	Initial Release, RevA PCB's only. Excludes BOM and daughter card instructions.
1.0	September 2007	A. Robertson	Production EVB release. Includes BOM and schematics for EVB, 144QFP, 176QFP and 208BGA daughter cards

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1. Introduction

This user manual details the setup and configuration of the Freescale Semiconductor MPC5510 Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the MPC5510 family of microprocessors, and to facilitate hardware and software development.

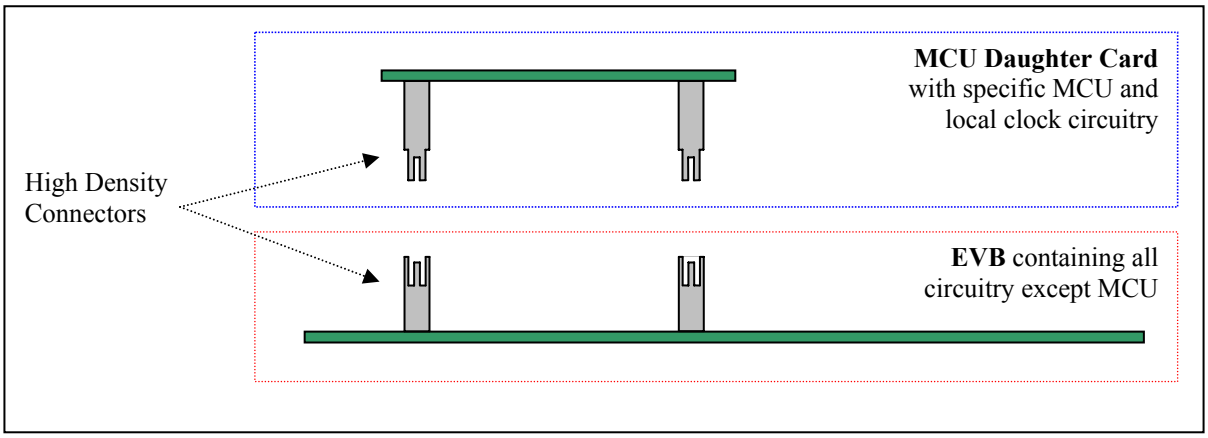
There are currently 3 package types supported within the MPC5510 family (and by the EVB), namely 208BGA, 176QFP and 144QFP. For the latest product information, please speak to your freescale representative or consult the MPC5510 website at www.freescale.com

The EVB is intended for bench / laboratory use and has been designed using normal temperature specified components (+70°C).

1.1 Modular Concept

For maximum flexibility and simplicity, the EVB has been designed as a modular development platform. The EVB main board does not contain an MCU. Instead, the MCU is fitted to an MCU daughter card (sometimes referred to as an adapter board). This approach means that the same EVB platform can be used for multiple package and MCU derivatives within the MPC5510 family. High density connectors provide the interface between the EVB and MCU daughter cards as shown in the diagram below. See section 4 for more information on the daughter card configuration.

Figure 1-1 Modular Concept – EVB and MCU Daughter Cards



2. EVB Features

The EVB provides the following key features:

- Support provided for different MPC5510 MCU family members by utilising MCU daughter cards.
- Single 12-14V external power supply input with on-board regulators to provide all of the necessary EVB and MCU voltages. Power may be supplied to the EVB via a 2.1mm barrel style power jack or a 2-way lever connector. 12V operation allows in-car use if desired.
- Freescale System Basis Chip footprint to allow use of the SBC power supply if required (available end 2007).
- Flexible on-board power supply configuration with the option to bypass the internal MCU regulators for diagnostic purposes. MCU power can also be sourced from either the EVB regulators or the SBC.
- Master power switch and regulator status LED's.
- User reset switch with status LED's.
- User configurable LVI (Low Voltage Inhibit) device to monitor the status of the 5V regulators.
- Control of the BOOTCFG status via a dedicated jumper.
- Flexible MCU clocking options allow provision of an external clock via an SMA connector or 8Mhz EVB clock oscillator circuit. Jumpers on the daughter card allow selection between these external clocks or the local daughter card ALC oscillator circuitry. The MCU clkout signal is routed to an SMA connector for easy access.
- Standard 14-pin ONCE debug connector and 38-pin MICTOR Nexus2+ connectors.
- Twin 120-way polarised daughter card expansion connectors allowing connection of the MCU daughter card or a custom board for additional application specific circuitry.
- All of the MCU signals are readily accessible at a group of port-ordered 0.1" pitch headers.
- Up to 256Kbytes of external SRAM memory which can be configured as either 32-bit or 16-bit data port width.
- SCI channels A and B can be routed to either a standard DB9 female connector (PC RS-232 compliant) or LIN interface header (0.1"), both will full physical transceivers (the SBC provides an additional 2 LIN interfaces).
- MCU FlexCAN channels A and C can be routed to 0.1" headers via a Philips high speed CAN transceiver (The SBC provides an additional CAN physical interface).
- 7x5 LED dot matrix display connected to the MCU eMIOS PWM channel [0..11] via a 16244 buffer / driver.
- User prototyping area consisting of a 0.1" grid of through hole pads with easy access to the EVB ground and power supply rails. 4 active low LED's and 4 small pushbutton switches are adjacent to the prototype area.
- Jumper selectable variable resistor connected to ATD channel 0, driving between VRH and VRL.
- Liberal scattering of GND test points (surface mount loops) placed throughout the EVB.

Note – to alleviate confusion between jumpers and headers, all EVB jumpers are implemented as 2mm pitch whereas headers are 0.1inch (2.54mm). This prevents inadvertently fitting a jumper to a header.

IMPORTANT

Before the EVB is used or power is applied, please fully read this user manual.

Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.

3. Configuration

This section details the configuration of each of the EVB functional blocks.

Throughout this document, all of the default jumper and switch settings are clearly marked with "**(D)**" and are shown in blue text. This should allow a more rapid return to the default state of the EVB if required. Note that the default configuration for 3-way jumpers is a header fitted between pins 1 and 2. On the EVB, 2-way and 3-way jumpers have been aligned such that Pin1 is either to the top or to the left of the jumper. On 2-way jumpers, the source of the signal is connected to Pin1.

The EVB has been designed with ease of use in mind and has been segmented into functional blocks as shown below. Detailed silkscreen legend has been used throughout the board to identify all switches, jumpers and user connectors.

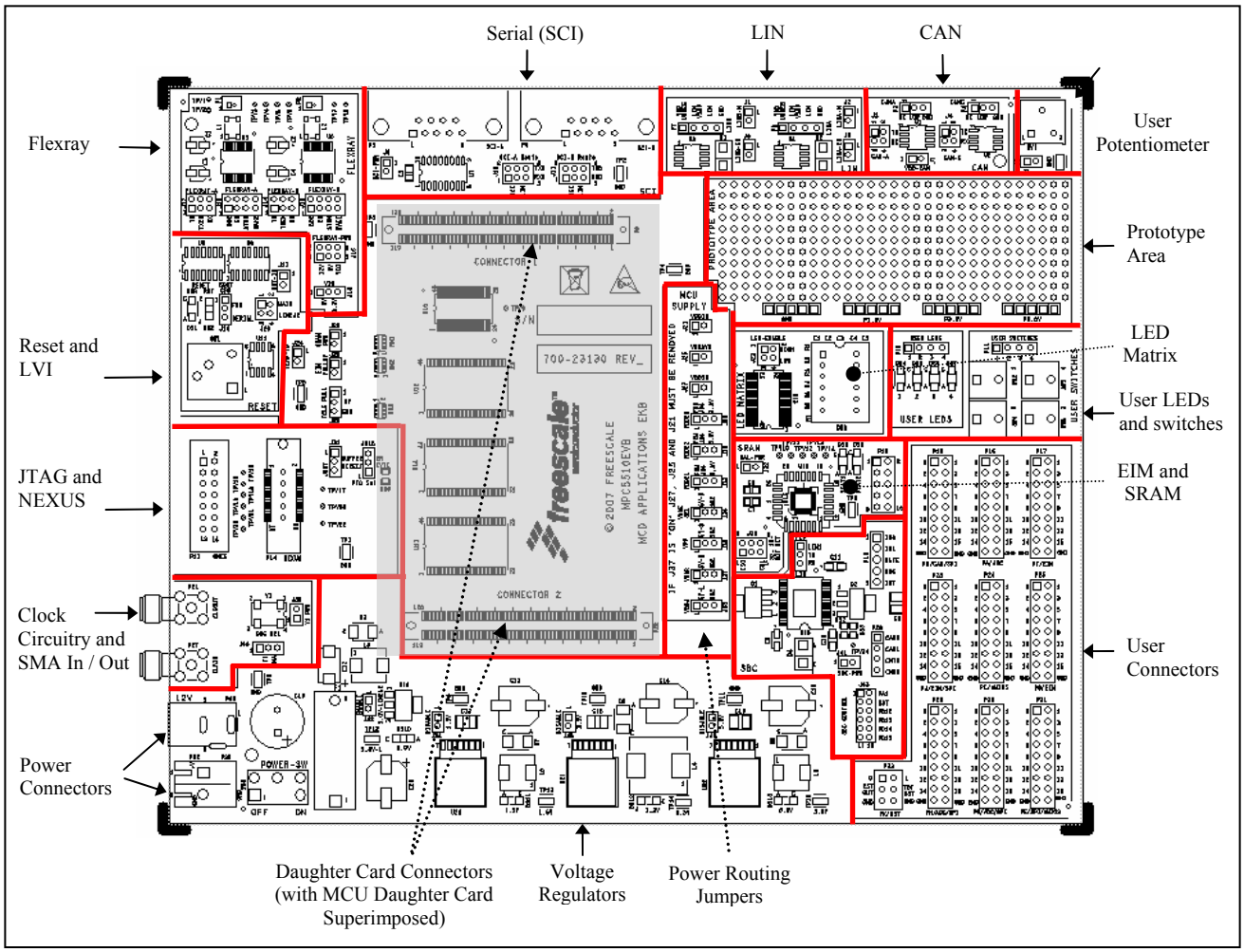
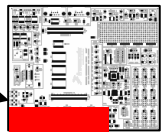


Figure 3-1 EVB Functional Blocks

3.1 Power Supply Configuration

The Power supply section is located in the bottom left area of the EVB



The EVB requires an external power supply voltage of 12V DC, minimum 1A. This allows the EVB to be easily used in a vehicle if required. The 12v input is regulated on the EVB using 1 linear and 3 switching regulators to provide the necessary EVB and MCU operating voltages of 5.0V, 3.3V and 1.5V. In addition, the EVB supports the Freescale System Basis Chip (SBC) which is an integrated regulator for the MCU power supply lines. For flexibility there are two different power supply input connectors on the EVB as detailed below.

3.1.1 Power Supply Connectors

2.1mm Barrel Connector – P28:

This connector should be used to connect the supplied wall-plug mains adapter. Note – if a replacement or alternative adapter is used, care must be taken to ensure the 2.1mm plug uses the correct polarisation as shown below:

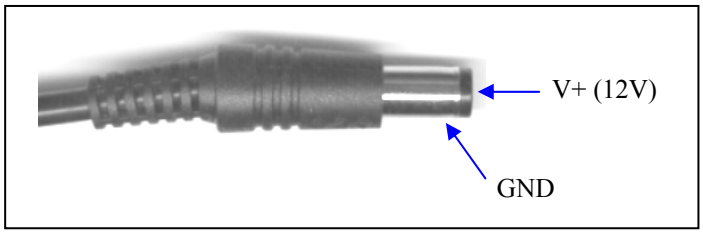


Figure 3-2 2.1mm Power Connector

2-Way Lever Connector – P32:

This can be used to connect a bare wire lead to the EVB, typically from a laboratory power supply. The polarisation of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

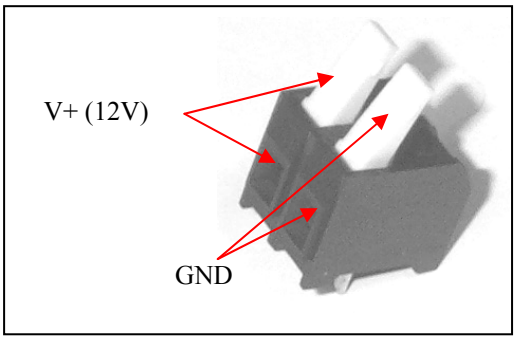


Figure 3-3 2-Lever Power Connector

3.1.2 Power Switch (SW6)

Slide switch SW6 can be used to isolate the power supply input from the EVB voltage regulators if required.

Moving the slide switch to the **right** (away from connector P32) will turn the EVB **on**.
Moving the slide switch to the **left** (towards connector P32) will turn the EVB **off**.

3.1.3 Regulator Power Jumpers (J42, J44, J45 and J46)

The Power supply control jumpers are located adjacent to the respective regulators.

As mentioned above, the EVB has four voltage regulators on board:

- 1.5V switching regulator (U20) to supply the MCU Core voltage when the MCU on-chip regulator is disabled.
- 3.3V switching regulator (U21) for EVB peripherals and MCU logic when the on-chip regulator is disabled.
- 5.0V switching regulator (U22) for the MCU regulator and I/O and EVB peripherals.
- 5.0V linear regulator (U19) for the MCU ADC power supply

All of the regulators have the option of being disabled if they are not required. The table below details the jumper configurations for enabling and disabling the regulators. By default, all of the regulators are enabled.

Table 3-1 Regulator Power Jumpers

Jumper	Position	PCB Legend	Description
J42 (5.0V-LINEAR)	FITTED **(D)** REMOVED	ENABLE	5.0V linear regulator output is Enabled 5.0V linear regulator output is Disabled
J44 (1.5V)	FITTED REMOVED **(D)**	DISABLE	1.5V switching regulator output is Disabled 1.5V switching regulator output is Enabled
J45 (3.3V)	FITTED REMOVED **(D)**	DISABLE	3.3V switching regulator output is Disabled 3.3V switching regulator output is Enabled
J46 (5.0V)	FITTED REMOVED **(D)**	DISABLE	5.0V switching regulator output is Disabled 5.0V switching regulator output is Enabled

3.1.4 Power Status LED's and Fuse

When power is applied to the EVB, four green LED's adjacent to the voltage regulators show the presence of the supply voltages as follows:

LED DS10 – Indicates that the 5.0V linear regulator is enabled and working correctly
LED DS11 – Indicates that the 1.5V switching regulator is enabled and working correctly
LED DS12 – Indicates that the 3.3V switching regulator is enabled and working correctly
LED DS13 – Indicates that the 5.0V switching regulator is enabled and working correctly

If no LED's are illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW6 is in the "OFF" position or that the fuse F1 has blown. The fuse will blow if power is applied to the EVB in reverse-bias, where a protection diode ensures that the main fuse blows rather than causing damage to the EVB circuitry. If the fuse has blown, check the polarity of your power supply connection then replace fuse F1 with a 20mm 500mA fast blow fuse.

3.1.5 SBC Power Jumper (J41)

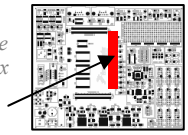
The optional SBC (System Basis Chip) regulator has a single power supply input jumper as detailed in the table below. By default, the SBC is disabled. For more details on the SBC regulator see Figure 3-4 below.

Table 3-2 SBC Power Jumpers

Jumper	Position	PCB Legend	Description
J41 (SBC-PWR)	FITTED REMOVED **(D)**		SBC linear regulator output is Enabled SBC linear regulator output is Disabled

Note – the SBC will not be available until the end of 2007 so it will not be fitted on an EVB manufactured prior to the SBC release date.

The MCU power supply jumpers are located in the centre of the EVB in a box titled "MCU Supply"



3.1.6 MCU Supply Routing and Jumpers (J21, J25, J27, J29, J30, J33, J34, J36, J37, J38)

The MCU has internal regulators to generate the 3.3V and 1.5V supplies for VDDSYN, VDD33 and VDD. Whilst this is the intended mode of operation for the MCU, the EVB allows the internal MCU regulators to be disabled by disconnecting VDDR and applying external voltages to the VDDSYN, VDD33 and VDD pins via jumpers J25, J27 and J21 respectively).

The VDDE[1..3] pins control the pad voltages over 3 groupings of pads (see the MCU reference manual for details). Jumpers J29, J30, J33 and J34 allow the VDDEx pins to be connected to the 5.0v or 3.3V switching regulators or to the SBC auxiliary output which can is software selectable between 5.0V and 3.3V.

Each of the main supply pins (VDDA, VDDR, VPP and VDDEx) has the option of being routed from either the EVB regulators (where VDDA has a dedicated linear regulator to ensure a accuracy) or from the SBC.

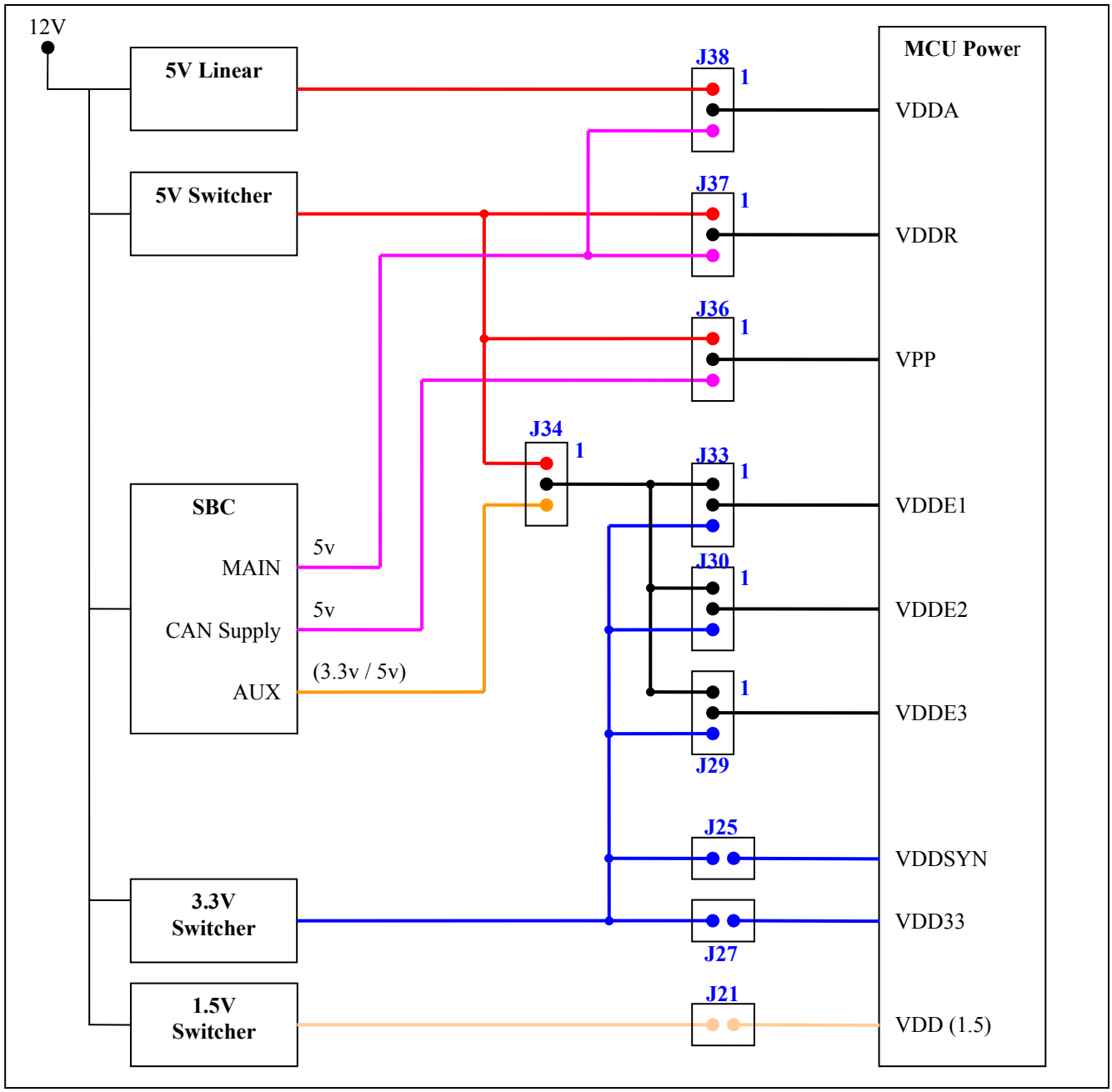


Figure 3-4 Power Supply Routing

Table 3-3 MCU Power Supply Jumpers

Power Domain	Jumper	Position	PCB Legend	Description
5.0V	J38 (VDDA)	1-2 **(D)** 2-3	5V-L SBC	MCU VDDA is powered from 5V linear regulator MCU VDDA is powered from SBC (VDD output)
	J37 (VDDR) *	1-2 **(D)** 2-3 *REMOVED**	5V-S SBC	MCU internal VREG is powered from 5.0V switching reg MCU internal VREG is powered from SBC (VDD output) *MCU regulator is not powered (See note below)*
	J36 (VPP)	1-2 **(D)** 2-3	5V-S SBC	MCU VPP is powered from 5.0V switching regulator MCU VPP is powered from SBC (VCAN output)
5.0V / 3.3V	J34 (VDDE SEL)	1-2 **(D)** 2-3	5V-S SBC	VDDEx jumpers are supplied from 5V switching regulator VDDEx jumpers are supplied from SBC (VAUX Output)
	J33 (VDDE1)	1-2 **(D)** 2-3	FRM J34 3.3V	MCU VDDE1 is powered from output of J34 MCU VDDE1 is powered from 3.3V switching regulator
	J30 (VDDE2)	1-2 **(D)** 2-3	FRM J34 3.3V	MCU VDDE2 is powered from output of J34 MCU VDDE2 is powered from 3.3V switching regulator
	J29 (VDDE3)	1-2 **(D)** 2-3	FRM J34 3.3V	MCU VDDE3 is powered from output of J34 MCU VDDE3 is powered from 3.3V switching regulator
3.3V	J27 (VDD33)	FITTED REMOVED **(D)**		MCU VDD33 pin is powered from switching regulator MCU VDD33 pin is not powered externally
	J25 (VDDSYN)	FITTED REMOVED **(D)**		MCU VDDSYN pin is powered from switching regulator MCU VDDSYN pin is not powered externally
1.5V	J21 (VDD15)	FITTED REMOVED **(D)**		MCU VDD pin is powered from 1.5v switching regulator MCU VDD pin is not powered externally

The jumper configuration shown in Table 3-3, details the default state of the EVB. In this configuration, the SBC is not used and all power is supplied from the Linear and Switching regulators.

- VDDA is connected to the 5.0V Linear regulator
- VDDR is connected to the 5.0V switching regulator, enabling the internal MCU 3.3V / 1.5V regulators
- VPP and VDDE[1..3] are connected to the 5.0V switching regulator
- VDD33, VDDSYN and VDD are not powered externally.

IMPORTANT

When jumper J37 (VDDR) is in position 1-2 (5V-S), the MCU internal voltage regulators are enabled and supply power to the 3.3V and 1.5V MCU power domains. In this case, jumpers J27 (VDD33), J25 (VDDSYN) and J21 (VDD15) ***must not be fitted.***

Similarly, when jumper J37 is removed, no power is supplied to the MCU internal voltage regulators and jumpers J27 (VDD33), J25 (VDDSYN) and J21 (VDD15) must be fitted to power the respective MCU pins. The 3.3V and 1.5v switching regulators must also be enabled in this case.

When the internal voltage regulator is disabled and power is applied to VDDSYN, VDD33 and VDD, a ferrite bead on VSSSYN needs to be activated. This is achieved by de-soldering a zero-ohm link on the bottom of the daughter card. See section 4.2.1 for details. Note that external regulator mode is not the intended mode of operation of the MCU and should be used for test purposes only.

3.1.6.1 VDDE[1..3] Voltage Groupings

Before changing the VDDEx voltage from the default 5.0V setting, you need to ensure that this will not impact any of the EVB peripherals that may be in use. The table below details what EVB peripherals are tied to a particular VDDEx grouping and also the MCU pin operating voltage suitable for that peripheral.

Table 3-4 VDDE[1..3] Pad Groupings

Item	Port Pins	VDDE Group	Required Pad Voltage
LED Dot Matrix Display	PortC[0..11]	VDDE1	5.0V or 3.3V
External Memory	PortG[0..15], PortF[0..15], PortH[14,15], PortJ[0..7]	VDDE2 VDDE2 / 3 VDDE2 VDDE2	5.0V
CANA and CANC	PortD [0..5]	VDDE1	5.0V
SCI / LIN A and B	PortD[6..9]	VDDE1	5.0V
Flexray	PortC[0..2, 7..9]	VDDE1	5.0V or 3.3V (J18 selects)
JTAG		VDDE3	5.0V
Nexus	PF[0..11]	VDDE2 / 3	5.0V

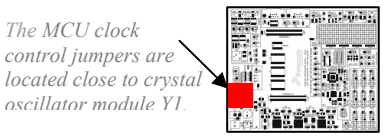
3.1.7 EVB Circuitry Power Domains

Before disabling any of the EVB regulators, it is worthwhile considering if any of the EVB components or peripherals you require will be affected. Table 3-5 details a list of the various EVB components and peripherals powered by the regulators. Note – the SBC powers the MCU only and does not supply power to any of the EVB circuitry.

Table 3-5 Power Supply Distribution

Regulator	Used On
1.5V (Switcher)	MCU VDD1.5 pins (ONLY use when on-chip MCU regulator is disabled) Daughter Card Connectors (1.5V) 1.5V Power section of Prototype area
3.3V (Switcher)	MCU VDD33 and VDDSYN pins (ONLY use when on-chip MCU regulator is disabled) MCU VDDEx pins (when run in 3.3v mode) Oscillator Module (Y1) GAL22V10 (EIM Control) Driver chip for LED Matrix I/O supply for Flexray interface when VIO is 3.3V Daughter Card Connectors (3.3V) 3.3V Power section of Prototype area
5.0V (Switcher)	MCU VDDEx (5v mode), VPP and VDDR pins LVI circuit main power (affecting Reset Switch) Reset-In / Reset-Out logic Reset configuration circuitry SRAM memory and address latches RS-232 Transceiver LIN transceiver CAN transceivers Flexray transceivers EIM signal pullup resistors Daughter Card Connectors (5.0V) 5.0V Power section of Prototype area eICE and Nexus connectors
5.0V (Linear)	MCU VDDA pin LVI circuit monitor

3.2 MCU Clock Control (J39 and J40)



3.2.1 Clock Selection

The EVB supports three possible MCU clock sources:

(1) The local ALC pierce oscillator circuit (on the MCU daughter card)
(2) An 8Mhz oscillator module on the EVB (Y1), driving the MCU EXTAL signal
(3) An external clock input to the EVB via the SMA connector (P27), driving the MCU EXTAL signal

The clock circuitry is shown in the diagram below. Please refer to section 4 for specific daughter card configuration details.

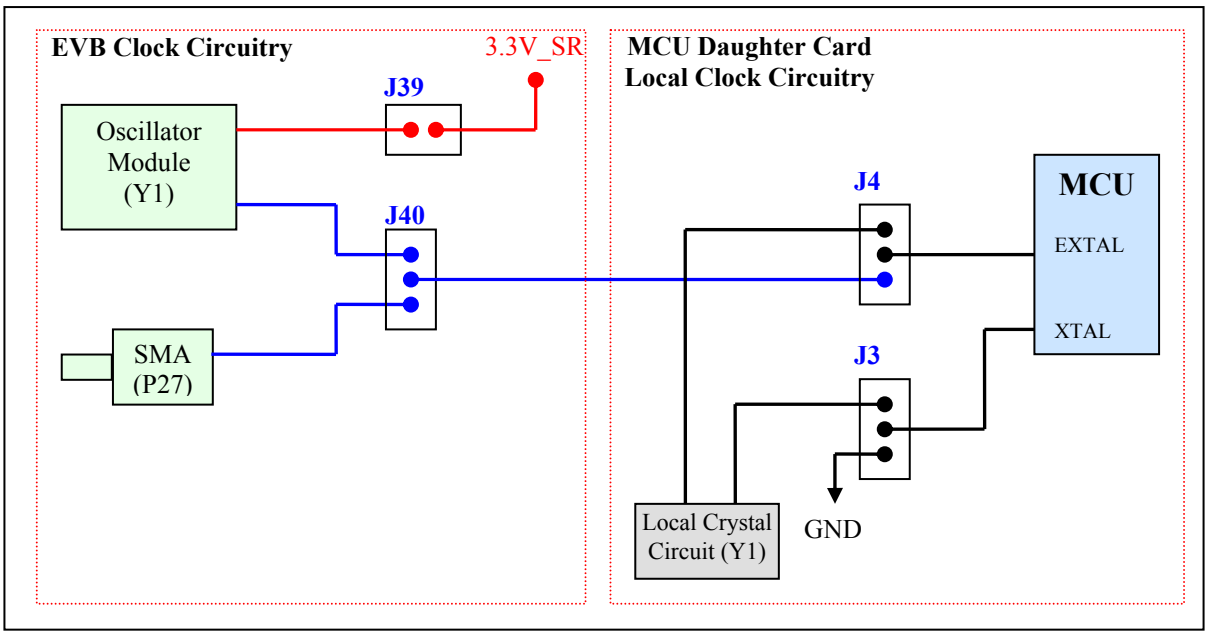


Figure 3-5 EVB Clock Selection

Table 3-6 Clock Source Jumper Selection

Jumper	Position	PCB Legend	Description
J39 (Y1 PWR)	FITTED **(D)** REMOVED		EVB oscillator module Y1 is powered EVB oscillator module Y1 is not powered
J40 (OSC SEL)	1-2 **(D)** 2-3	Y1 SMA	Daughter card EXT-CLK is routed from Y1 Daughter card EXT-CLK is routed from P27

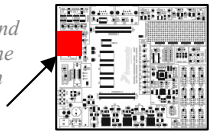
The default configuration provides power to the EVB oscillator module (Y1) and routes this clock signal to the MCU daughter card. Note that the 3.3V regulator must be enabled when using oscillator module Y1. In order to use the SMA connector (P27) to supply a clock signal, jumper J40 must be moved to position 2-3 (SMA). The selection between local clock circuitry or external oscillator is achieved using jumpers on the daughter card. See section 4 for details.

CAUTION

The MPC5510 clock circuitry is all 3.3v based. Any external clock signal driven into the SMA connector must have a maximum voltage of 3.3V

3.3 Reset Control (Jumpers J17, J19, J20, SW1)

The RESET switch (RED) and LVI circuitry is located in the top left corner of the EVB in the area titled "RESET "



The EVB incorporates an LVI (Low Voltage Inhibit) device to provide under-voltage protection for the two main 5.0V regulators (Linear and Switcher). The SBC has its on monitoring circuit so does not require external monitoring. When either of the 5.0V regulator voltages fall below a preset threshold level, the LVI will assert the MCU reset line to prevent incorrect operation of the MCU (or EVB circuitry).

The table below shows the approximate threshold voltages for each regulator

Table 3-7 LVI Monitor Threshold Voltages

Regulator	Minimum Voltage Before MCU reset
5.0V Linear	4.45V
5.0V Switcher	4.65V

The LVI is powered from the 5.0V switching regulator and monitors the 5.0V linear using a 2nd power fail monitor circuit. The LVI also provides a de-bounced input for EVB reset switch SW1.

Jumpers are provided to disable either the main LVI reset out (which affects the reset from the 5.0V switching regulator and from the reset switch) or the power fail out circuit (which only affects the reset from the 5.0V linear regulator). If the switching regulator LVI is disabled, the reset switch will not function.

Table 3-8 LVI Control Jumpers

Jumper	Position	PCB Legend	Description
J20 Posn 1-2	FITTED **(D)** REMOVED	MAIN	5.0V switching regulator is monitored, Reset switch active 5.0V switching regulator is not monitored, Reset switch inactive
J20 Posn 3-4	FITTED **(D)** REMOVED	LINEAR	5.0V linear regulator is monitored 5.0V linear regulator is not monitored

Notes:

- *If the 5.0V switching regulator is disabled for any reason, the LVI circuit will attempt to assert the MCU Reset signal. Jumper shunts on jumper J20 position 1-2 and 3-4 must be removed in this situation. This will also leave the reset switch SW1 inoperative.*
- *If the 5.0V linear regulator is disabled, the shunt on jumper J20 position 3-4 must be removed to prevent the LVI asserting reset.*

3.3.1 Reset LEDs

There are two reset LED's, DS1 (AMBER) and DS2 (RED), placed adjacent to the EVB RESET switch to indicate the RESET status of the EVB and MCU.

LED DS2, titled "RST", will illuminate if the MCU itself issues a reset. In this condition, LED DS1 will not illuminate.

LED DS1, titled "USR", will illuminate when one of the following external hardware devices issues a reset to the MCU:

- LVI circuitry (either an under-voltage detection or the reset switch is pressed).
- There is a reset being asserted from the user connectors or from the daughter card.
- There is a reset being driven from the Nexus or JTAG debug probe.

Note that LED DS2 (MCU Reset) will also illuminate during an external (user) reset!

3.3.2 Reset Buffering Scheme

The MPC5510 family has a single reset pin. This single pin functions as a dual purpose input / output signal, providing Reset-In and Reset-Out functionality.

There is a lot of circuitry on the EVB that has access to the reset pin. In order to reduce the loading on the MCU when driving the reset pin and also to allow connection of non open-drain reset inputs, a reset-in and reset-out buffering scheme is implemented as shown in Figure 3-6.

Reset-In - There are 3 possible external sources of reset:
- JTAG / Nexus connector reset
- User reset (from user connectors)
- LVI reset circuitry, including the reset switch.

Each of these reset sources is fed into the input of an AND gate and then converted to an open-drain output which is directly connected to the MCU reset pin.

Reset-Out - The MCU reset pin is buffered to provide a reset-out signal, capable of driving the reset LED and also all other devices requiring a reset input.

The reset buffering scheme is detailed below – note that the SBC also has an open drain reset in / out that is connected directly to the MCU reset line.

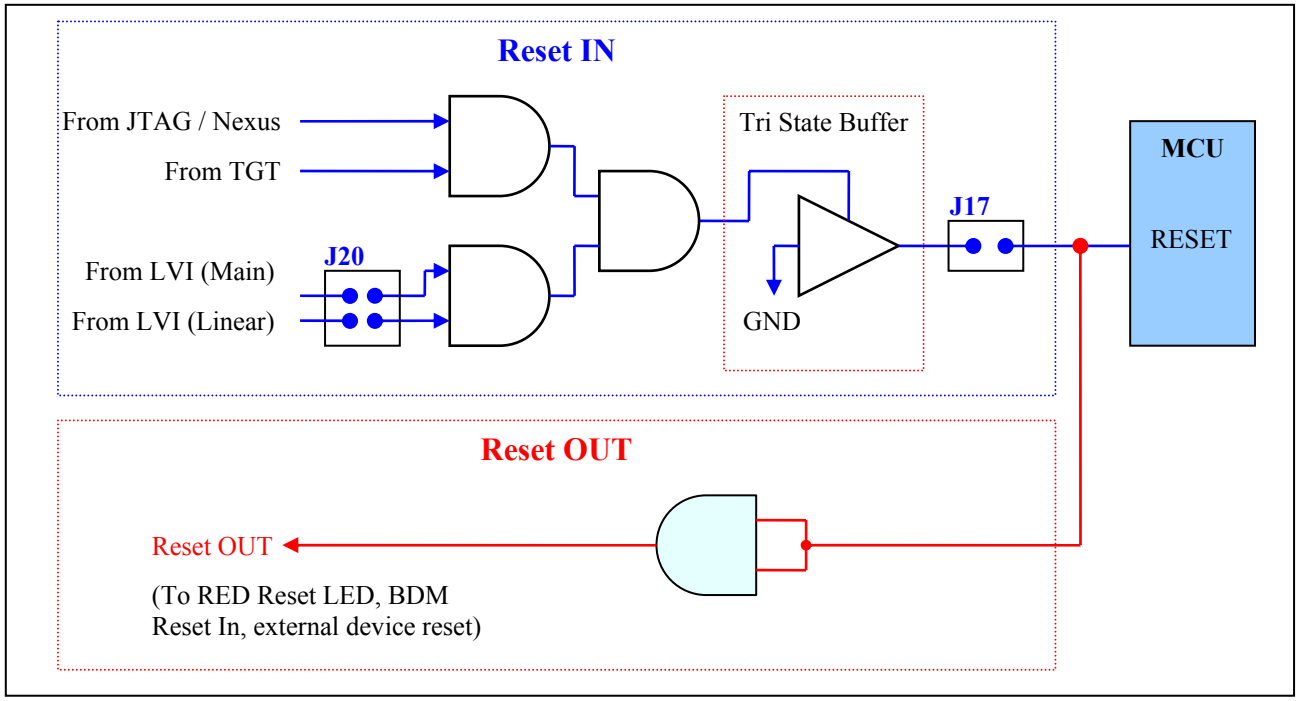


Figure 3-6 EVB Reset Buffering Scheme

Jumper J17 is used to completely disconnect the reset-in buffering if desired. This is for debug purposes only and should normally be left connected. Disconnecting this jumper will mean no external MCU reset can be achieved

Table 3-9 Reset-Out Control Jumper

Jumper	Position	PCB Legend	Description
J17 (RST-IN)	FITTED **(D)**		External reset source (LVI, Debug or Target) will be able to assert MCU reset
	REMOVED		External reset is disabled (Not recommended)

3.3.3 Reset Boot Configuration (J19)

The MPC5510 has a single boot configuration pin (BOOTCFG) which determines the boot location of the MCU based on the state of the pin at POR (Power On Reset). This is shown in the table below:

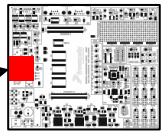
Table 3-10 BOOTCFG Control

Jumper	Position	PCB Legend	Description
J19 (BOOT CFG)	1-2 **(D)**	FSH	MCU boots from internal flash
	2-3	SERIAL	MCU boots from external serial source

Note – there have been some problems observed when application code is present in flash and an attempt is made to load and execute a different application from internal RAM. Depending on the configuration and speed of the debugger used, it is feasible that the application code in flash will already have started to execute by the time the debugger gains control. This has implications if the flash code has already done some configuration of the device that is in conflict with the operation of the code that is about to be loaded into RAM. To prevent this occurring, it is advised to either erase the internal flash or to prevent the MCU booting from flash by moving jumper J19 to position 2-3.

3.4 Debug Configuration (J24, J28, J31, J31B)

The ONCE and NEXUS connectors are located at the left hand edge of the EVB



The EVB supports a standard ONCE cable with a 14-pin 0.1" walled header footprint. There is also a 38-pin MICTOR connector for Nexus 2+ debug. Four generic jumpers are associated with both the ONCE and Nexus, as detailed below.

3.4.1 TCLK Configuration

Some debug manufacturers specify whether the debug TCLK signal is pulled low or high. Jumper J28 provides the ability to select whether TCLK is pulled to GND or 5V.

Table 3-11 ONCE / NEXUS TCLK Termination Control

Jumper	Position	PCB Legend	Description
J28 (TCLK PULL)	1-2 **(D)**	5V	TCLK signal is pulled to 5.0V via 10KΩ
	2-3	GND	TCLK signal is pulled to GND via 10KΩ

Notes:

- *J28 is located to the right of the reset switch, out-with the ONCE / Nexus connector area.*
- *To achieve accurate low power current measurements, TCLK should be pulled to GND*

3.4.2 Reset Buffering

Most debug probes only assert the MCU reset line but some also have the ability to also monitor the status of the reset line. This is not possible when the reset signal is buffered so jumper J31 is included to allow routing the debug reset signal direct to the MCU reset pin or via the EVB Reset-In buffering.

Table 3-12 JTAG / NEXUS Target Reset Routing

Jumper	Position	PCB Legend	Description
J31 (JRST)	1-2 **(D)**	BUFFER	JTAG reset signal is buffered to MCU RESET pin (connected to the MCU Reset-In circuitry)
	2-3	DIRECT	JTAG reset signal is connected direct to MCU RESET pin

The default configuration connects the JTAG reset signal to the MCU reset via a buffer so the probe cannot monitor the reset. If your debug probe has an open-drain reset capable of monitoring the reset signal, this can be enabled by moving jumper J31 to position 2-3.

CAUTION

If jumper J31 is positioned 2-3 and the debug probe actively drives the reset line high and low, nothing else will be able to assert the MCU reset (including the MCU itself).

3.4.3 PFO Selection

MCU pin PF0 has alternate functions of EVTI (debug control signal) and R/W. To prevent conflicts between the external memory and debug interface, jumper J31B is used to route PF0 to either the debug connectors or the external memory as shown in the table, below.

Table 3-13 PFO EVTI / R/W Function Selection

Jumper	Position	PCB Legend	Description
J31B (PFO Sel)	1-2 **(D)**	EVTI	MCU PFO is routed to the ONCE / Nexus debug connector
	2-3	RW	MCU PFO is routed to the external memory system

The default configuration connects PF0 to the debug connectors to act as EVTI. If the external bus is to be used then J31B must be moved to position 2-3 to route PF0 to the memory subsystem as the R/W signal.

Note – EVTI is optional for ONCE debug and generally not required so with the jumper configured in position 2-3 to enable RW, a "ONCE" debug session can still be established.

3.4.4 Vendor I/O Configuration

Some Nexus debug probes can use the "Vendor I/O2" signal to drive BOOTCFG reset configuration data at reset. The EVB is designed such that this will over-ride any BOOTCFG data supplied by jumper J19 (see section 3.3.3). A jumper is supplied to allow this feature to be enabled if desired.

Table 3-14 Vendor I/O2 Drive Control

Jumper	Position	PCB Legend	Description
J24	FITTED		Vendor I/O2 pin disconnected
(VEND-IO)	REMOVED **(D)**		Vendor I/O2 pin can drive BOOTCFG at reset

By default, the debug tool will not have the ability to over-ride the EVB BOOTCFG settings and J24 will be removed. To enable this feature, fit jumper J24.

Note – Be careful when fitting jumper J24 as this will override the EVB BOOTCFG setting when a nexus probe is fitted to the EVB.

3.4.5 Debug Connector Pinouts

The EVB is fitted with 14-pin JTAG / ONCE and 38-pin Nexus 2+ debug connectors. The following diagram shows the 14-pin JTAG / ONCE connector pinout (0.1" keyed header).

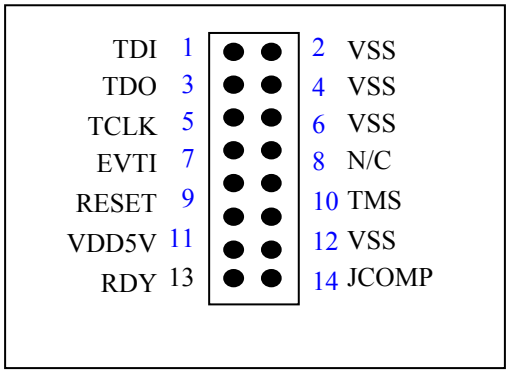


Figure 3-7 MPC5510 JTAG / ONCE Connector

The Nexus module used on the MPC5510 family uses the JTAG pins (for control of the Nexus block) along with additional Nexus pins for trace messages. Nexus mode is entered by a JTAG sequence whereby the Nexus EVTI pin is sampled on the rising edge of the JTAG TRST pin. If the EVTI is asserted on TRST, Nexus is enabled.

The table below shows the pinout of the 38-pin MICTOR Nexus connector for the MPC5510

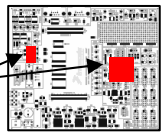
Table 3-15 NEXUS Debug Connector Pinout

Pin No	Function	Connection		Pin No	Function	Connection
1	Reserved	---		2	Reserved	---
3	Reserved	---		4	Reserved	---
5	Vendor I/O-0	---		6	CLKOUT	MCU PE6
7	Vendor I/O-2	BOOTCFG		8	Vendor I/O-3	---
9	Reset-In	Reset CCT		10	EVTI	MCU PF0
11	TDO	MCU TDO		12	VREF	P5V
13	Vendor I/O-4	---		14	RDY	---
15	TCLK	MCU TCK		16	MDO[7]	MCU PF11
17	TMS	MCU TMS		18	MDO[6]	MCU PF10
19	TDI	MCU TDI		20	MDO[5]	MCU PF9
21	TRST	JCOMP		22	MDO[4]	MCU PF8
23	Vendor I/O-1	---		24	MDO[3]	MCU PF7
25	Tool I/O-3	RST-OUT		26	MDO[2]	MCU PF6
27	Tool I/O-2	---		28	MDO[1]	MCU PF5
29	Tool I/O-1	---		30	MDO[0]	MCU PF4
31	UBATT	12V Vin		32	EVTO	MCU PF1
33	UBATT	12V Vin		34	MCK0	MCU PF3
35	Tool I/O-0	---		36	MSE1	----
37	VALTREF	P5V		38	MSEO	MCU PF2

Note - In order to preserve the ability to accurately measure power consumption on the MCU pins, the JTAG and Nexus connector reference voltages are sourced directly from the 5V regulator or from the 12V unregulated input.

3.5 External Memory Configuration

The external memory block is located on the right had side of EVB with some jumpers to right of the reset switch



The MPC5510 external bus interface supports a multiplexed address/data bus with a configurable data-port size of either 16-bits or 32-bits. The EVB uses 3 x 128Kbyte (16-bit) asynchronous SRAM memories to provide either 128Kbytes of memory in 16-bit port width mode or 256Kbytes of memory in 32-bit port width. A high speed PLD is used to control the routing of the relevant control signals depending on the selected port size.

Note that the SRAM does not supply a transfer acknowledge (TA) signal to the MCU at the end of a data cycle so the MCU external bus must be configured with auto TA acknowledge enabled. Additional wait states may be required depending on the MCU bus speed. See the relevant MCU reference manual for more details.

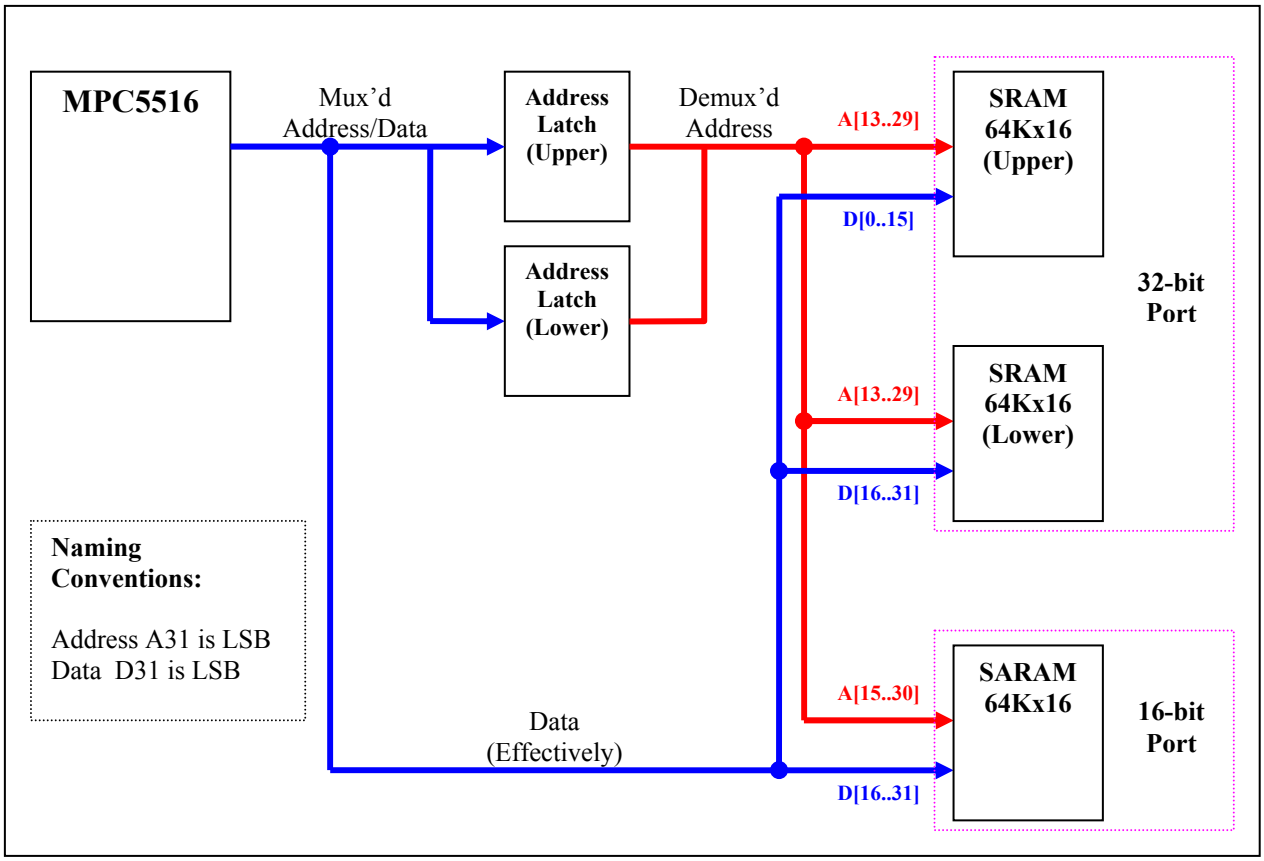


Figure 3-8 External Memory Subsystem

The MPC5510 family does not have an "expanded mode" of operation unlike other MCU families you may have encountered. Instead the individual port pins must be switched to the correct mode of operation for the external bus. The table below shows what MCU pins are required for correct bus operation in 16-bit and 32-bit port size modes.

Table 3-16 MCU pins required for EIM SRAM operation

SRAM Port Size Configuraiton	PortE	Port F	Port G	Port H	Port J
16-Bit	6	0, 1, 9, 10, 11, 12, 13, 14, 15	[0..15]		
32-Bit	6	[0..15]	[0..15]	14, 15	[0..7]

Notes:

- *PE6 is the MCU CLKOUT pin which is required for the operation of the external memory*
- *PortF is shared with the Nexus debug port so the external memory cannot be used at the same time as Nexus.*

Jumpers are provided as detailed in the following sections to enable the memory system and also to control the MCU chip select assignment and port size configuration. Note that the 3.3V and 5.0V switching regulators must be enabled for the external memory system to function.

3.5.1 Memory Power Control (J22, J32))

The memory subsystem has components operating at 3.3V and 5.0V. Each of these power domains has a separate power jumper as detailed below. The SRAM devices and address latch buffers operate at 5.0V, controlled by jumper J22. The PLD used to control the logic is powered from 3.3V (with 5.0V tolerant I/O). This has a separate power jumper J32.

Table 3-17 SRAM, and PLD Power Control Jumpers (J22, J32)

Jumper	Position	PCB Legend	Description
J22 (SRAM PWR)	FITTED **(D)** REMOVED		The SRAM and address latches are powered (enabled) The SRAM and latches are not powered (disabled)
J32 (GAL-PWR)	FITTED REMOVED **(D)**		The control PLD is powered (enabled) The control PLD is not powered (disabled)

By default the SRAM memory and latches are powered but the PLD is disabled. This ensures that outputs on the buffers and SRAM's are tri-stated so do not affect the corresponding GPIO signals. To power down the memory and latches if desired, remove jumper J22. In order to use the external SRAM, the memory, latches and GAL must all be powered by fitting jumpers J22 **and** J32.

Note – The SRAM and buffers are 5.0V devices so the corresponding MCU pins must be configured as 5.0V.

3.5.2 Port Size Select and Chip Select Control (J35)

Jumper J35 serves 2 purposes with a single jumper. Firstly it determines which MCU chip select (CS0 or CS1) is used to control the SRAM and secondly it determines whether the SRAM is configured for a 16-bit or 32-bit data port size.

Table 3-18 Chip select and Port-Size Control Jumper (J35)

Jumper	Position	PCB Legend	Description
J35	REMOVED		No SRAM system is enabled
	2-4 **(D)**	CS0 / 16-Bit	MCU chip select 0 is used to control 16-bit SRAM
	4-6	CS1 / 16-Bit	MCU chip select 1 is used to control 16-bit SRAM
	1-3	CS0 / 32-Bit	MCU chip select 0 is used to control 32-bit SRAM
	3-5	CS1 / 32-Bit	MCU chip select 1 is used to control 32-bit SRAM

Notes:

- *The jumper shunts should be placed horizontally! Any jumper combination other than those shown in the table above is invalid and will cause mal-function of the EVB or MCU.*
- *This jumper header has no effect unless jumper J22 and J32 are fitted.*

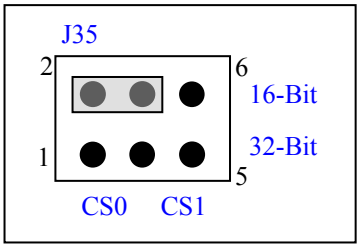


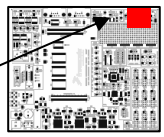
Figure 3-9 CS and Port-Size Control Jumper

By default, jumper header J35 is fitted to position 2-4. This enables the 16-bit SRAM system connected to MCU chip select CS0. Moving the jumper horizontally determines which chip select is used, whereas moving the jumper header vertically determines whether the 16-bit or 32-bit wide SRAM system is enabled.

Two LED's adjacent to the GAL (DS8 / DS9) indicate the GAL operation and status.
DS9 shows GAL is powered and programmed and goes out when the EVB or MCU is in reset.
DS8 illuminates when an external SRAM access is taking place.

3.6 CAN Configuration (J3, J4, J7)

The CAN section is located in the top right corner of the EVB in an area marked "CAN"



The EVB has a Philips PCA82C250T high speed CAN transceiver on each of the MCU CAN-A and CAN-C channels. The transceiver is pre-configured for high speed operation by tying pin 8 of each PCA82C250T to ground via a zero ohm resistor. If required, these resistors can be exchanged to provide slope control mode of operation. See the EVB schematics at the end of this manual for details on the resistor to change.

For flexibility, the CAN transceiver I/O is connected to a standard 0.1" connector at the top edge of the PCB. Connector P3 provides the CAN bus level signal interface for CAN-A and connector P4 for CAN-B. The pinout for these connectors is shown below.

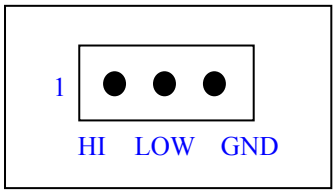


Figure 3-10 CAN Physical Interface Connector

Each of the MCU signals to the CAN transceivers is jumpered, allowing the transceiver to be isolated if the respective MCU pin is not configured or used for CAN operation. There is a 2x2 jumper for each CAN channel (one for Rx, one for Tx), as shown in the table below. The Global power jumper (J7) physically removes power from both CAN transceivers.

Table 3-19 CAN Control Jumpers (J3, J4, J7)

Jumper	Position	PCB Legend	Description
J7 (VDD-CAN)	FITTED **(D)** REMOVED		Power is applied to both CAN transceivers No power is applied to CAN transceivers
J3 (CAN-A) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU CNTX-A is connected to CAN controller A MCU CNTX-A is NOT routed to CAN controller .
J3 (CAN-A) Posn 3-4	FITTED **(D)** REMOVED	RX	MCU CNRX-A is connected to CAN controller A MCU CNRX-A is NOT routed to CAN controller.
J4 (CAN-C) Posn 1-2	FITTED **(D)** REMOVED	TX	MCU CNTX-C is connected to CAN controller C MCU CNTX-C is NOT routed to CAN controller .
J4 (CAN-C) Posn 3-4	FITTED **(D)** REMOVED	RX	MCU CNRX-C is connected to CAN controller C MCU CNRX-C is NOT routed to CAN controller.

The default configuration is with all jumpers fitted. This fully enables both CAN-A and CAN-C, with all MCU signals routed to the transceivers. If the MCU is configured such that a CAN channel is used as GPIO, then the respective jumpers must be removed from J3 or J4 or conflicts will occur.

Notes

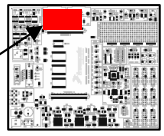
- *Both CAN channels are available on all current package derivatives (see table below)*
- *Care should be taken when fitting the jumper headers to the 2x2 jumper blocks J3 and J4 as they can easily be fitted in the incorrect orientation. Jumpers J3 and J4 are fitted **horizontally**.*

Table 3-20 CAN Pin Availability

CAN	1ST Alternate		Pin Availability		
	TX	RX	144 Pin	176 Pin	208 Pin
A	PD0	PD1	✔	✔	✔
B	PD3	PD2	✔	✔	✔
C	PD4	PD5	✔	✔	✔

3.7 RS232 Configuration (J9, J10, J11)

The RS232 circuitry is located at the top edge of the EVB in an area titled "SCI"



The EVB has a single MAX232CSE RS232 transceiver device, providing RS232 signal translation for MCU SCI channels A and B.

Each of the two RS232 outputs from the MAX232 device is connected to a 9-way female D-Type connector, allowing a direct RS232 connection to a PC or terminal. Connector P5 provides the RS232 level interface for MCU SCI-A and P6 for MCU SCI-B. The pinout of these connectors is detailed below. Note that hardware flow control is not supported on this implementation.

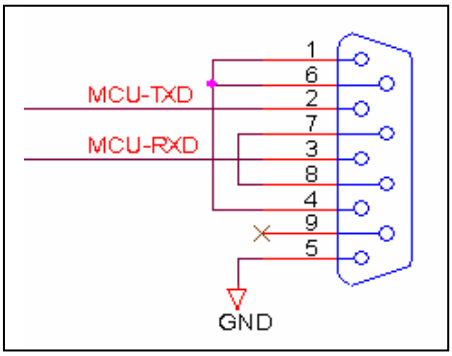


Figure 3-11 RS232 Physical Interface Connector

The MPC5516 eSCI also provides hardware LIN master capability which is supported on the EVB via LIN transceivers (see section 3.8 for details). Jumpers J10 and J11 are provided to route the MCU SCI signals to either the RS232 or LIN physical interfaces as described below. There is also a global power jumper (J9) controlling the power to the RS232 transceivers.

Table 3-21 RS232 Control Jumpers

Jumper	Position	PCB Legend	Description
J9 (SCI-PWR)	FITTED **(D)** REMOVED		Power is applied to the MAX232 transceiver No power is applied to the MAX232 transceiver
J10 (SCI-A) Top Row	2-4 (D) 4-6 REMOVED	TXD	MCU TXD-A is routed via MAX232 to P5 MCU TXD-A is routed via LIN transceiver to P8 MCU TXD-A signal is disconnected from CAN/LIN
J10 (SCI-A) Bottom Row	1-3 (D) 3-5 REMOVED	RXD	MCU RXD-A is routed via MAX232 to P5 MCU RXD-A is routed via LIN transceiver to P8 MCU RXD-A signal is disconnected from CAN/LIN
J11 (SCI-B) Top Row	2-4 (D) 4-6 REMOVED	TXD	MCU TXD-B is routed via MAX232 to P6 MCU TXD-B is routed via LIN transceiver to P7 MCU TXD-B signal is disconnected from CAN/LIN
J11 (SCI-B) Bottom Row	1-3 (D) 3-5 REMOVED	RXD	MCU RXD-B is routed via MAX232 to P6 MCU RXD-B is routed via LIN transceiver to P7 MCU RXD-B signal is disconnected from CAN/LIN

The default configuration enables SCI-A and SCI-B channels. RS232 compliant interfaces (with no hardware flow control) are available at DB9 connectors P5 and P6. If the MCU is configured such that the pins used on SCI-A or SCI-B are used for GPIO (see Table 3-22), then the relevant jumpers must be removed to avoid any conflicts occurring. If required, jumper J9 can be used to completely disable the SCI transceiver.

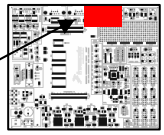
*Note - Care should be taken when fitting the jumper headers to the 2x3 jumper blocks J10 and J11 as they can easily be fitted in the incorrect orientation. Jumpers J10 and J11 are fitted **horizontally**.*

Table 3-22 SCI Pin Availability

SCI	1ST Alternate		Pin Availability		
	TX	RX	144 Pin	176 Pin	208 Pin
A	PD6	PD7	✔	✔	✔
B	PD8	PD9	✔	✔	✔
C	PF10	PF11	✔	✔	✔
D	PF12	PF13	✔	✔	✔
E	PH4	PH5	✔	✔	✔
F	PH6	PH7	✔	✔	✔
G	PB12	PB13	x	✔	✔
h	PB14	PB15	x	✔	✔

3.8 LIN Configuration (J1, J2, J5, J6)

The LIN circuitry is located in the top edge of the EVB in an area titled "LIN"



The EVB is fitted with two freescale MC33399 LIN transceivers. The MCU SCI channels incorporate a hardware controlled LIN master, and as such, the LIN transceiver is connected to the same MCU pins as the RS232 transceiver. Jumpers J10 and J11 are used as described in section 3.7 (and in the table below) to determine whether the relevant MCU pins are connected to the LIN transceiver or the SCI transceiver.

For flexibility, the LIN transceivers are connected to a standard 0.1" connector (P8 for LIN-A and P7 for LIN-B) at the top edge of the PCB as shown in the figure below. For ease of use, the 12V EVB supply is fed to pin1 of the connectors and the LIN transceiver power input to pin 2. This allows the LIN transceiver to be powered directly from the EVB supply by simply linking pins 1 and 2 of connector P7/P8 using a 0.1" jumper shunt.

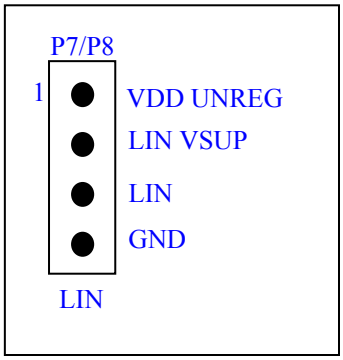


Figure 3-12 LIN Physical Interface Connector

Along with the MCU signal routing jumpers (J10 / J11), there are jumpers (J5 / J6) to enable or disable the LIN transceiver and jumpers (J1 and J2) which determine if the LIN transceiver is operating in master or slave mode, as defined in the table below.

Table 3-23 LIN Control Jumpers

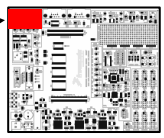
Jumper	Position	PCB Legend	Description
J1 (LINB-M)	FITTED **(D)** REMOVED		LIN-B transceiver is configured for LIN Master mode LIN-B transceiver is configured for LIN Slave mode
J2 (LINA-M)	FITTED **(D)** REMOVED		LIN-A transceiver is configured for LIN Master mode LIN-A transceiver is configured for LIN Slave mode
J5* **(LINB-EN)**	FITTED **(D)** REMOVED		The LIN-B transceiver is enabled The LIN-B transceiver is disabled
J6* **(LINA-EN)**	FITTED **(D)** REMOVED		The LIN-A transceiver is enabled The LIN-A transceiver is disabled
J10 (SCI-A) Top Row	2-4 (D) 4-6 REMOVED	TXD	MCU TXD-A is routed via MAX232 to P5 MCU TXD-A is routed via LIN transceiver to P8 MCU TXD-A signal is disconnected from CAN/LIN
J10 (SCI-A) Bottom Row	1-3 (D) 3-5 REMOVED	RXD	MCU RXD-A is routed via MAX232 to P5 MCU RXD-A is routed via LIN transceiver to P8 MCU RXD-A signal is disconnected from CAN/LIN
J11 (SCI-B) Top Row	2-4 (D) 4-6 REMOVED	TXD	MCU TXD-B is routed via MAX232 to P6 MCU TXD-B is routed via LIN transceiver to P7 MCU TXD-B signal is disconnected from CAN/LIN
J11 (SCI-B) Bottom Row	1-3 (D) 3-5 REMOVED	RXD	MCU RXD-B is routed via MAX232 to P6 MCU RXD-B is routed via LIN transceiver to P7 MCU RXD-B signal is disconnected from CAN/LIN

* *Note – Jumpers J5/J6 do NOT route power to LIN transceivers, they only control an enable line on the LIN device. Power to the LIN transceiver is supplied via connectors P7 / P8, pin 2.*

The Default LIN configuration is with the module enabled in master mode. By default, the EVB SCI/LIN signals are routed to the SCI transceivers. To use the LIN interface, the corresponding RX and TX pins must be routed to the LIN transceivers by re-configuring jumpers J10 and J11 with the shunts positioned on pins 2-3 and 5-6. LIN slave mode can be enabled by removing jumpers J1 / J2.

3.9 Flexray Configuration (J12, J13, J14, J15, J16, J18)

The Flexray circuitry is located in the top edge of the EVB in an area titled "Flexray"



The EVB is fitted with 2 flexray physical interfaces connected to MCU flexray channels A and B. Jumpers J12 and J14 are provided to route the respective MCU signals to the physical interfaces as described below.

Table 3-24 Flexray MCU Signal Routing Jumpers (J12, J14)

Jumper	Position	PCB Legend	Description
J12 (Flex-A) Posn 1-2	FITTED REMOVED **(D)**	TX	MCU PC1 is connected to Flexray A transceiver TX MCU PC1 is not connected to Flexray A transceiver TX
J12 (Flex-A) Posn 3-4	FITTED REMOVED **(D)**	TXEN	MCU PC0 is connected to Flexray A transceiver TXEN MCU PC1 is not connected to Flexray A transceiver TXEN
J12 (Flex-A) Posn 5-6	FITTED REMOVED **(D)**	RX	MCU PC2 is connected to Flexray A transceiver RXEN MCU PC2 is not connected to Flexray A transceiver RXEN
J14 (Flex-A) Posn 1-2	FITTED REMOVED **(D)**	TX	MCU PC8 is connected to Flexray B transceiver TX MCU PC8 is not connected to Flexray B transceiver TX
J14 (Flex-A) Posn 3-4	FITTED REMOVED **(D)**	TXEN	MCU PC9 is connected to Flexray B transceiver TXEN MCU PC9 is not connected to Flexray B transceiver TXEN
J14(Flex-A) Posn 5-6	FITTED REMOVED **(D)**	RX	MCU PC7 is connected to Flexray B transceiver RXEN MCU PC7 is not connected to Flexray B transceiver RXEN

The power to the Flexray physical interface is controlled via jumper J16 to allow disconnection if required. The Flexray physical interface is capable of interfacing with MCU I/O voltages of 3.3V or 5.0V as defined by the voltage supplied to VIO via jumper J18. On the MPC5516, the MCU pad voltage is controlled by the voltage supplied to VDDE[1..3]. The user must ensure that the voltage on the respective PortC pads is the same as VIO supplied to the flexray interface.

Table 3-25 Flexray Power Control Jumpers (J16, J18)

Jumper	Position	PCB Legend	Description
J16 (Flex-PWR) Posn 1-2	FITTED REMOVED **(D)**	12V	12V Flexray circuitry is powered from main 12Vinput 12V Flexray circuitry is not powered
J16 (Flex-PWR) Posn 3-4	FITTED REMOVED **(D)**	5V	5V Flexray circuitry is powered from 5.0V switching reg 5V Flexray circuitry is not powered
J16 (Flex-PWR) Posn 5-6	FITTED REMOVED **(D)**	VIO	VIO Flexray circuitry is powered from J18 VIO Flexray circuitry is not powered
J18 (VIO)	1-2 **(D)** 2-3 REMOVED	5V 3.3V	VIO is selected as 5.0V. VIO is selected as 3.3V No Power is applied to the VIO jumper J16, posn 5-6

The flexray interface has 4 pins which are used for configuration and are pulled high or low controlled by a jumper as described in the table below. By default, all of the jumper headers are fitted. Please consult the Flexray physical interface specification before changing any of these jumpers.

Table 3-26 Flexray Control Jumpers (J13, J15)

Jumper	Position	PCB Legend	Description
J13 (Flex-A) Posn 1-2	FITTED **(D)** REMOVED	BGE	Flexray-A interface BGE signal is pulled to VIO Flexray-A interface BGE signal is unterminated
J13 (Flex-A) Posn 3-4	FITTED **(D)** REMOVED	EN	Flexray-A interface EN signal is pulled to VIO Flexray-A interface EN signal is unterminated
J13 (Flex-A) Posn 5-6	FITTED **(D)** REMOVED	STBEN	Flexray-A interface STBN signal is pulled to VIO Flexray-A interface STBN signal is unterminated
J13 (Flex-A) Posn 7-8	FITTED **(D)** REMOVED	WAKE	Flexray-A interface WAKE signal is pulled to GND Flexray-A interface WAKE signal is unterminated
J15 (Flex-B) Posn 1-2	FITTED **(D)** REMOVED	BGE	Flexray-B interface BGE signal is pulled to VIO Flexray-B interface BGE signal is unterminated
J15 (Flex-B) Posn 3-4	FITTED **(D)** REMOVED	EN	Flexray-B interface EN signal is pulled to VIO Flexray-B interface EN signal is unterminated
J15 (Flex-B) Posn 5-6	FITTED **(D)** REMOVED	STBEN	Flexray-B interface STBN signal is pulled to VIO Flexray-B interface STBN signal is unterminated
J15 (Flex-B) Posn 7-8	FITTED **(D)** REMOVED	WAKE	Flexray-B interface WAKE signal is pulled to GND Flexray-B interface WAKE signal is unterminated

Notes:

- *The default configuration has the flexray controller disabled. Flexray A and B are a second alternate function of PortC (as shown in the table below). Before enabling Flexray, you must ensure that none of the associated port pins are being used for any other function. On the EVB, PortC is shared with the LED Dot matrix display.*
- *The flexray physical interfaces use molex 1.25mm shrouded 2-pin connectors to connect to the flexray bus (as are standard fit on many Freescale development platforms using flexray).*

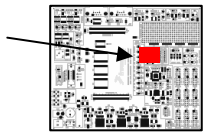
Important:
A 40Mhz oscillator is required for the correct operation of the flexray controller. Please ensure that an appropriate crystal is fitted to the MCU daughter card or use a 40Mhz external clock source.

Table 3-27 Flexray Pin Availability

Flexray	2nd Alternate			Pin Availability		
	TXEN	TX	RX	144 Pin	176 Pin	208 Pin
A	PC0	PC1	PC2	✔	✔	✔
B	PC9	PC8	PC7	✔	✔	✔

3.10 LED Dot Matrix (J23)

The LED matrix is located beneath the prototype area



The EVB includes a 5x7 LED dot matrix display connected via a 16244 buffer to MCU PortC / eMIOS [0..11] pins. The PWM ability on the pins allows strobing effects or the brightness of the matrix to be controlled if desired.

The LED matrix does not have any automatic character generation circuitry so to generate characters, the 7 rows of the display must be written row at a time with sufficient scan speed to form the character without flicker. This is potentially a good background task for the Z0 core on the 5510!

The diagram below shows how the matrix is connected. Note that this is a common anode display so is illuminated by asserting the columns "high" and the rows "low". If desired, the top two rows can be disabled for use with GPIO leaving 5 rows enabled which is still sufficient for most characters.

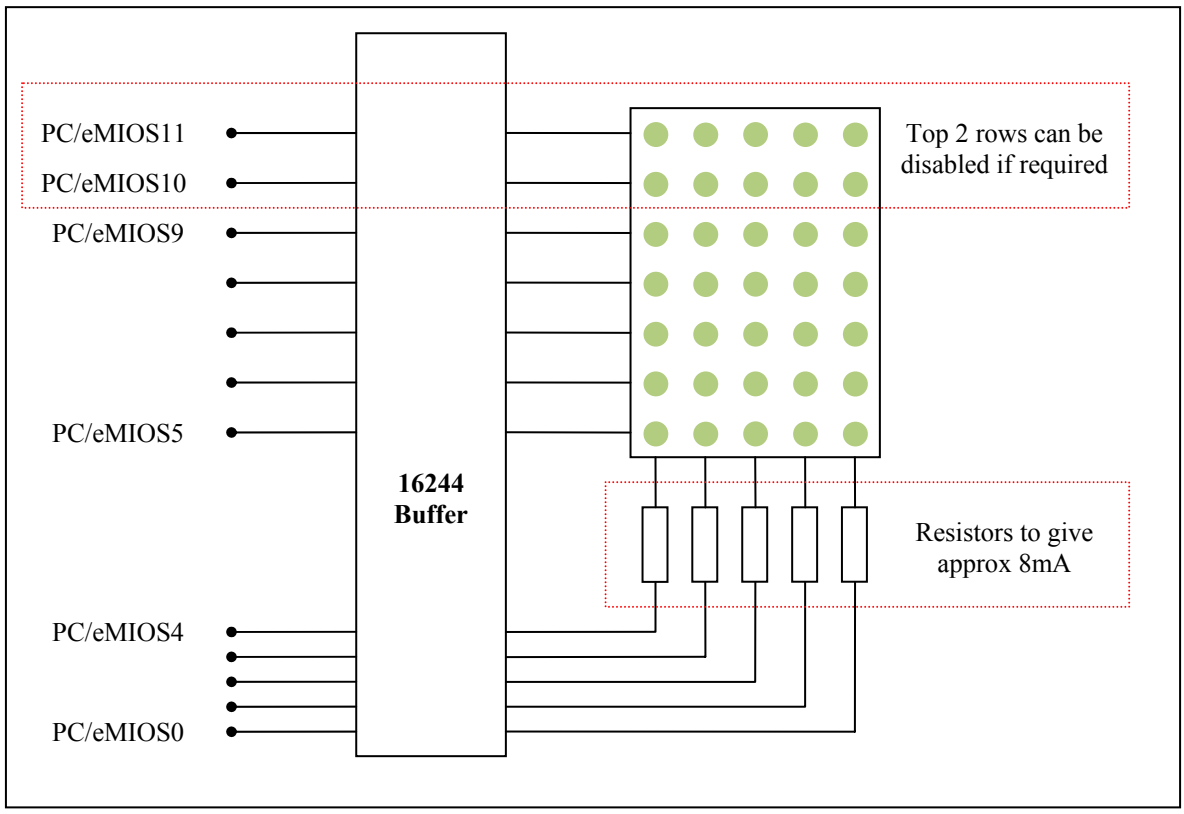


Figure 3-13 LED Matrix Control

The 16244 buffers provide 4 separate output enable blocks. These have been configured such that one block controls PortC outputs 10 and 11 and the remaining 3 blocks control PortC outputs [0..9]. This allows the top two rows to be disabled if required. A single jumper provides this functionality as described below.

Table 3-28 LED Matrix Control

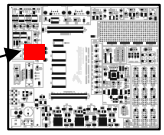
Jumper	Position	PCB Legend	Description
J23 (LED-Enable) Posn 1-2	FITTED (D)	HIGH	MCU PortC[10..11] signals are connected to LED Matrix
	REMOVED		MCU PortC[10..11] are not connected to LED Matrix
J23 (LED-Enable) Posn 3-4	FITTED (D)	LOW	MCU PortC[1..9] signals are connected to LED Matrix
	REMOVED		MCU PortC[1..9] are not connected to LED Matrix

By default, the LED matrix is fully enabled with MCU PortC[0..11] signals being routed to the LED Matrix. If you don't wish to use the matrix, both jumpers should be removed from J23.

Caution – PortC is also used by the Flexray interface so the LED matrix and flexray interface cannot be used concurrently. See section 5 for more details.

3.11 Termination Resistor Control (J26)

The termination control jumper is located to the right of the Reset switch. .



When using the external bus, there are some of the MCU control signals that must be pulled high. In most normal circumstances these signals can also be left pulled high when the external bus is not used, however a jumper (J26) is provided to disconnect the power to these pulllup resistors if desired.

Table 3-29 EIM Pullup Resistor Control (J26)

Jumper	Position	PCB Legend	Description
J26 (EIM Pullup)	FITTED (D)		The external bus pullup resistors are powered (enabled)
	REMOVED		The external bus pullup resistors are not powered (disabled)

4. Daughtercards

This section of the user manual details how to configure, install and remove the MCU daughtercards. Failure to follow the installation and removal instructions could cause damage to the daughtercard connectors. There are 3 daughtercards available as shown in the picture below. The jumper naming has been standardised between the daughtercards so the configuration steps are identical, making it extremely easy to migrate between cards.

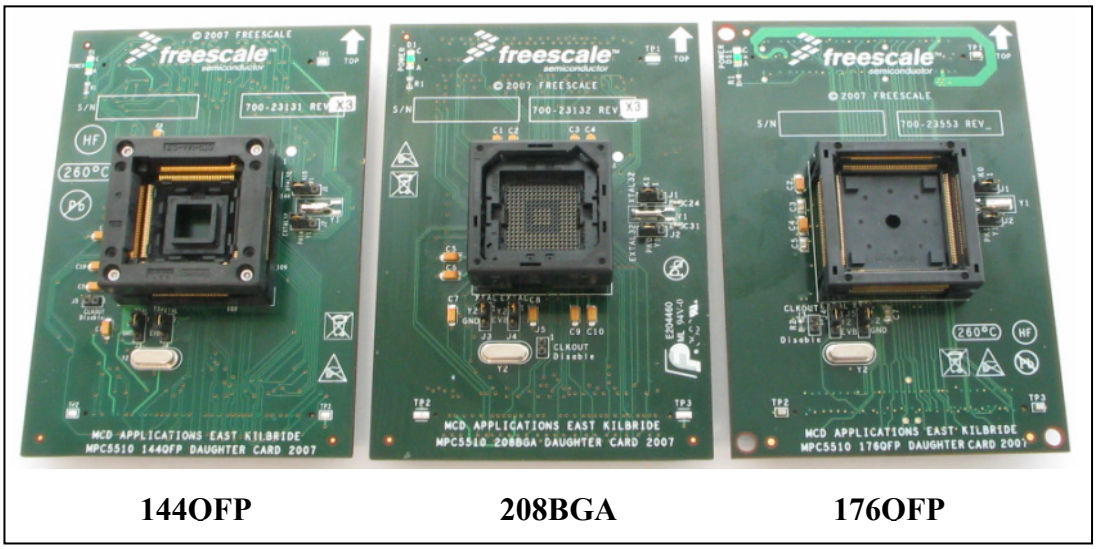


Figure 4-1 Daughter Cards

4.1 Installation and Removal Instructions

The MPC5510EVB daughtercard connectors have a unique placement footprint meaning that only daughtercards from the MPC5510 family can be fitted.

To fit the daughtercard:

- Ensure that the EVB is powered off
- With the white arrow on the daughtercard pointing towards the top of the EVB, carefully line up the connectors on the underside of the daughtercard with those on the EVB and gently press down to fit the daughtercard. Ensure the connectors are fully mated by pushing down on all corners of the daughtercard, or the EVB may not function as expected.

To remove the daughtercard:

- Ensure the EVB is powered off
- Gently rock the daughter card along the axis shown in the picture below. Note that attempting to pull the daughtercard off the board in any other manner will probably cause damage to the connectors.

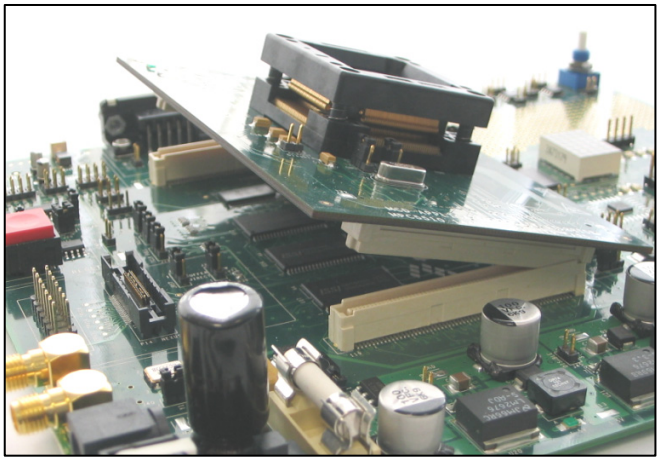


Figure 4-2 Daughter Card Removal

4.2 Daughtercard Configuration

4.2.1 External VREG Configuration

The default (and recommended) mode of operation of the MCU is to use the internal voltage regulators. If you need to bypass the internal voltage regulators and supply 3.3V and 1.5V externally, then a modification is required to the daughtercard to enable a ferrite bead on VSSSYN.

This is performed by de-soldering a zero ohm link located on the underside of the board.

Table 4-1 VSSSYN Ferrite Control

Daughtercard	Zero Ohm link to remove
144QFP	R6
176QFP	R103
208BGA	R6

CAUTION

Please ensure that any solder modifications to the daughter cards are carried out in an anti-static environment with the correct equipment and personnel for the job.

4.2.2 Main Clock Configuration

Each daughtercard contains a local crystal oscillator circuit and jumpers to allow the source of the clock to be selected from either the EVB or from the local crystal circuit.

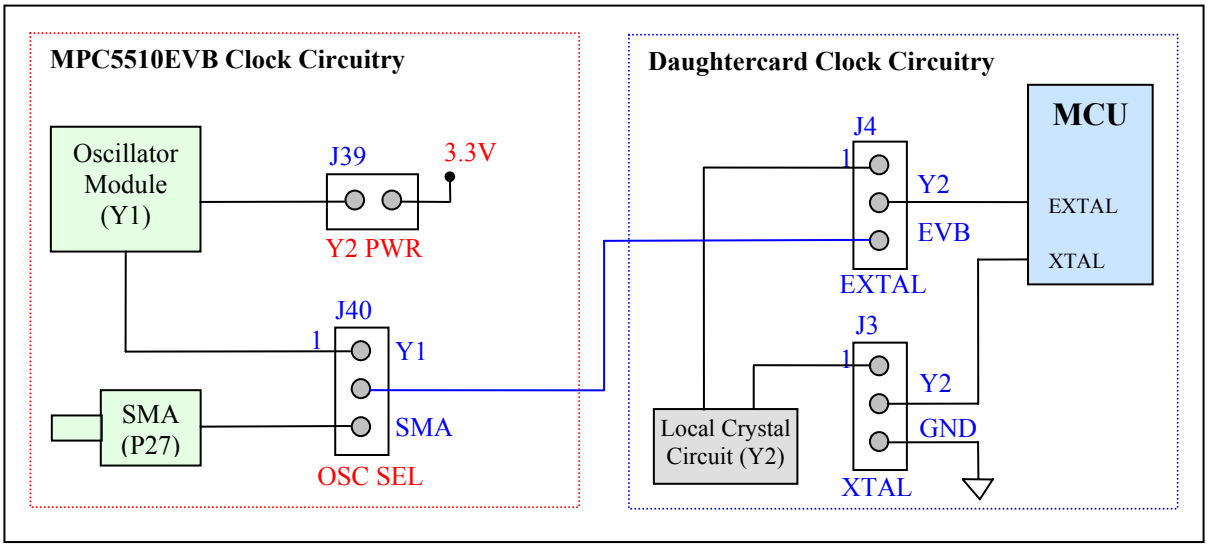


Figure 4-3 Daughtercard Clock Selection

Table 4-2 Daughtercard Clock Selection

Jumper	Position	PCB Legend	Description
J3	1-2 (**D**)	Y2	Clock is sourced from daughtercard crystal circuit
XTAL	2-3	GND	XTAL is grounded. Use when J4 is in posn 2-3
J4	1-2 (**D**)	Y2	Clock is sourced from daughtercard crystal circuit
EXTAL	2-3	EVB	Clock is sourced from EVB clock (oscillator or SMA)

The default configuration uses the local daughtercard clock. If you wish to drive a clock into the MCU EXTAL line from the EVB (either via the SMA connector or using the 8Mhz oscillator module), move both the EXTAL and XTAL jumpers to position 2-3.

4.2.3 32Khz Clock Configuration

The MPC5510 supports an optional 32Khz oscillator circuit used to drive an RTC (Real Time Counter). The 32Khz clock circuitry is populated on the daughtercard with 2 jumpers to allow selection of the 32Khz oscillator if required.

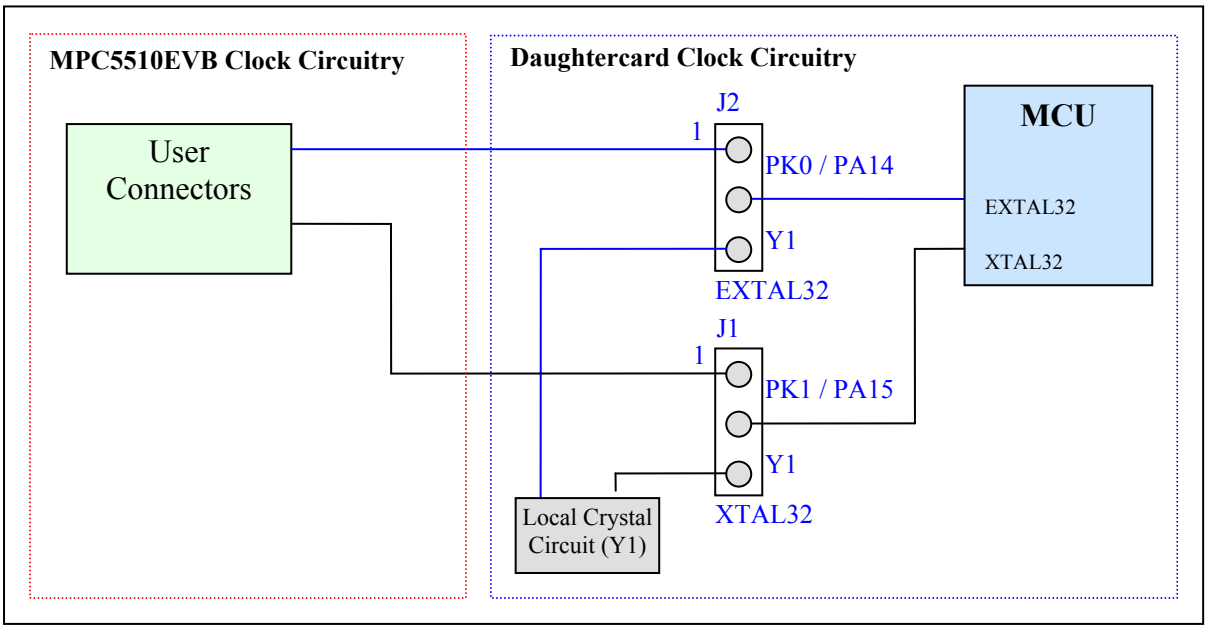


Figure4-4 Daughtercard 32Khz Clock Selection

Table 4-3 Daughtercard 32KHz Clock Selection

Jumper	Position	PCB Legend	Description
J1	1-2 (**D**)	PK0 / PF14	MCU pin is routed to EVB user connectors
XTAL32	2-3	Y1	MCU pin is connected to 32Khz crystal
J2	1-2 (**D**)	PK1 / PF15	MCU pin is routed to EVB user connectors
EXTAL32	2-3	Y1	MCU pin is connected to 32Khz crystal

The default configuration has the MCU EXTAL32 / XTAL32 pins connected to the MCU ports (PortH or PortF depending on the package used). If you wish to use the 32KHz crystal, jumpers J1 and J2 must both be moved to position 2-3.

4.2.4 CLKOUT Impedance Matching Control

The MCU PE6/CLKOUT line has a 33ohm series resistor close to the MCU in order to provide CLKOUT impedance matching. If required, this resistor can be shorted out (bypassed) by fitting a jumper header. To minimise the effect of radiated emissions, it is recommended this jumper is removed when PE6 is used for CLKOUT.

Table 4-4 Clkout Impedance Matchuing

Jumper	Position	PCB Legend	Description
J5 CLKOUT DISABLE	FITTED REMOVED (**D**)		MCU PE6 has no series termination MCU PE6 has in line 33ohm series resistor.

By default the jumper is removed to enable CLKOUT impedance matching. To disable impedance matching, fit the jumper.

CAUTION

Fitting daughtercard jumper J5 when CLKOUT is enabled on MCU PE6 will result in increased radiated emissions. Ensure this jumper is removed when CLKOUT is active.

4.2.5 Power LED

There is a green power LED fitted to the top left corner of the daughtercard. If the daughtercard is connected to the EVB and power is applied, this LED should illuminate. If the LED does not illuminate, please check the daughtercard is installed correctly and follow the main EVB power fault-finding tips detailed in section 3.1.4

5. MCU Pin Usage Map

The table below provides a useful cross reference to see what MCU port pins are used by the various EVB peripherals and functions. Note that there are some overlapping functions for example the Nexus and External bus as shown by the shaded boxes in the table below.

Table 5-1 EVB MCU Pin Usage

Function	PortA	PortB	PortC	PortD	PortE	PortF	PortG	PortH	PortJ
Enabled By Default									
Nexus					PE[6]	PF0..11]			
CANA				PD[0..1]					
CANC				PD[4..5]					
SCI / LINA				PD[6..7]					
SCI / LINB				PD[8..9]					
Reset Config				PD[2]					
Led Matrix			PC[0..11]						
User RVAR	PA[0]								
Disabled By Default									
SRAM					PE[6]	PF[0..15]	PG[0..15]	PH[14,15]	PJ[0..7]
Flexray A			PC[0..2]						
Flexray B			PC[7..9]						

6. Default Jumper Summary Table

The following table details the DEFAULT jumper configuration of the EVB as explained in detail in section 3.

Table 6-1 Default Jumper Positions

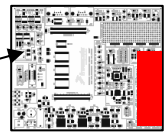
Jumper	Default Posn	PCB Legend	Description
J1 (LINB-M)	FITTED		LIN-B transceiver is configured for LIN Master mode
J2 (LINA-M)	FITTED		LIN-A transceiver is configured for LIN Master mode
J3 (CAN-A)	1-2 3-4	TX RX	MCU CNTX-A is connected to CAN controller A MCU CNRX-A is connected to CAN controller A
J4 (CAN-C)	1-2 3-4	TX RX	MCU CNTX-C is connected to CAN controller C MCU CNRX-C is connected to CAN controller C
J5 (LINB-EN)	FITTED		The LIN-B transceiver is enabled
J6 (LINA-EN)	FITTED		The LIN-A transceiver is enabled
J7 (VDD-CAN)	FITTED		Power is applied to both CAN transceivers
J8 (RV1)	FITTED		Output from variable resistor RV1 is applied to MCU PA0
J9 (SCI-PWR)	FITTED		Power is applied to the MAX232 transceiver
J10 (SCI-A)	2-4 1-3	TXD RXD	MCU TXD-A is routed via MAX232 to P5 MCU RXD-A is routed via MAX232 to P5
J11 (SCI-B)	2-4 1-3	TXD RXD	MCU TXD-B is routed via MAX232 to P6 MCU RXD-B is routed via MAX232 to P6
J12 (Flex-A)	REMOVED		All 3 shunts removed. No MCU signals connected to Flexray
J13 (Flex-A)	1-2 3-4 5-6 7-8	BGE EN STBEN WAKE	Flexray-A interface BGE signal is pulled to VIO Flexray-A interface EN signal is pulled to VIO Flexray-A interface STBN signal is pulled to VIO Flexray-A interface WAKE signal is pulled to GND
J14 (Flex-B)	REMOVED		All 3 shunts removed. No MCU signals connected to Flexray
J15 (Flex-B)	1-2 3-4 5-6 7-8	BGE EN STBEN WAKE	Flexray-B interface BGE signal is pulled to VIO Flexray-B interface EN signal is pulled to VIO Flexray-B interface STBN signal is pulled to VIO Flexray-B interface WAKE signal is pulled to GND
J16 (Flex-PWR)	REMOVED		All 3 flexray power supply voltages are disconnected
J17 (RST-IN)	FITTED		External reset source can assert MCU reset
J18 (VIO)	1-2	5V	
J19 (BOOT CFG)	1-2	FSH	MCU boots from internal flash
J20	1-2 3-4	MAIN LINEAR	5.0V switching regulator is monitored, Reset switch active 5.0V linear regulator is monitored
J21 (VDD15)	REMOVED		MCU VDD pin is not powered externally
J22 (SRAM PWR)	FITTED		The SRAM and latches are powered
J23 (LED-Enable)	1-2 3-4	HIGH LOW	MCU PortC[10..11] signals are connected to LED Matrix MCU PortC[1..9] signals are connected to LED Matrix
J24 (VEND-IO)	REMOVED		Vendor I/O2 pin can drive BOOTCFG at reset
J25 (VDDSYN)	REMOVED		MCU VDDSYN pin is not powered externally
J26 (EIM Pullup)	FITTED		The external bus pull-up resistors are powered (enabled)
J27 (VDD33)	REMOVED		MCU VDD33 pin is not powered externally
J28 (TCLK PULL)	1-2	5V	JTAG / NEXUS TCLK signal is pulled to 5.0V via 10KΩ
J29 (VDDE3)	1-2	FRM J34	MCU VDDE3 is powered from output of J34
J30 (VDDE2)	1-2	FRM J34	MCU VDDE2 is powered from output of J34
J31 (JRST)	1-2	BUFFER	JTAG reset signal is buffered to MCU RESET pin
J31B (PFO SEL)	1-2	EVTI	PFO is routed to Nexus for use as EVTI
J32 (GAL-PWR)	REMOVED		The control PLD is not powered (disabled)
J33 (VDDE1)	1-2	FRM J34	MCU VDDE1 is powered from output of J34
J34 (VDDE SEL)	1-2	5V-S	VDDEx jumpers are supplied from 5V switching regulator

Default Jumper Positions Continued

Jumper	Default Posn	PCB Legend	Description
J35	2-4	CS0 / 16-Bit	MCU chip select 0 is used to control 16-bit SRAM
J36 (VPP)	1-2	5V-S	MCU VPP is powered from 5.0V switching regulator
J37 (VDDR)	1-2	5V-S	MCU internal VREG is powered from 5.0V switching reg
J38 (VDDA)	1-2	5V-L	MCU VDDA is powered from 5V linear regulator
J39 (Y1 PWR)	FITTED		EVB oscillator module Y1 is powered
J40 (OSC SEL)	1-2	Y1	Daughter card EXT-CLK is routed from Y1
J41 (SBC-PWR)	REMOVED		SBC linear regulator output is Disabled
J42 (5.0V-LINEAR)	FITTED	ENABLE	5.0V linear regulator output is Enabled
J43 Not Impelemted			
J44 (1.5V)	REMOVED	DISABLE	1.5V switching regulator output is Enabled
J45 (3.3V)	REMOVED	DISABLE	3.3V switching regulator output is Enabled
J46 (5.0V)	REMOVED	DISABLE	5.0V switching regulator output is Enabled

7. User Connector Descriptions

The user connectors are located on the right hand side of the PCB



This section details the pinout of the EVB user connectors. The connectors are 0.1 inch pitch turned pin headers and are located to the right hand side of the EVB. Pins are grouped by port functionality and the PCB legend shows the respective port number adjacent to each pin.

Shaded GREEN areas represent pins that are shared with the Nexus port
Shaded BLUE areas represent a GPIO pin that is also used on the EVB for another purpose

Note that not all of the port functionality is available on all of the derivatives. Please consult your particular MCU documentation for details on available ports.

7.1.1 Port A / ADC (Connector P16, RV1 and J8)

Table 7-1 Port A Connector Pinout (P16)

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PA0	AN0	✓	✓	✓	2	PA1	AN1	✓	✓	✓
3	PA2	AN2	✓	✓	✓	4	PA3	AN3	✓	✓	✓
5	PA4	AN4	✓	✓	✓	6	PA5	AN5	✓	✓	✓
7	PA6	AN6	✓	✓	✓	8	PA7	AN7	✓	✓	✓
9	PA8	AN8	✓	✓	✓	10	PA9	AN9	✓	✓	✓
11	PA10	AN10	✓	✓	✓	12	PA11	AN11	✓	✓	✓
13	PA12	AN12	✓	✓	✓	14	PA13	AN13	✓	✓	✓
15	PA14	AN14	✓	✓	✓	16	PA15	AN15	✓	✓	✓
17	GND					18	GND				

To provide a quick means of supplying input to the ATD (Analogue To Digital converter), a 2KΩ variable resistor (RV1) will be connected between P5V and GND, with the output (centre tap) connected to PA0 / AN0 via jumper J8. By removing jumper J8, PA0 is disconnected from the variable resistor and can function as a normal I/O port. J8 and RV1 are located in the top right hand corner of the EVB

Table 7-2 RV1 Connection Jumper J8

Jumper	Position	PCB Legend	Description
J8 (RV1)	FITTED (D)		Output from variable resistor RV1 is applied to MCU PA0
	REMOVED		Output from RV1 is not connected to MCU (disabled)

Note - PA14 and PA15 can also be used for the EXTAL32 and XTAL32 32Khz reference clock. If these pins are used for this purpose, they will not be available for GPIO / ADC input. See section 4.2.3 for details.

7.1.2 Port B / ADC / SCI (P30)

Table 7-3 Port B Connector Pinout (P30)

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PB0	AN28	✓	✓	✓	2	PB1	AN29	✓	✓	✓
3	PB2	AN30	✓	✓	✓	4	PB3	AN31	✓	✓	✓
5	PB4	AN32	✓	✓	✓	6	PB5	AN33	✓	✓	✓
7	PB6	AN34	✓	✓	✓	8	PB7	AN35	✓	✓	✓
9	PB8	AN36	✓	✓	✓	10	PB9	AN37	✓	✓	✓
11	PB10	AN38	✓	✓	✓	12	PB11	AN39	✓	✓	✓
13	PB12	TXD_G		✓	✓	14	PB13	RXD_G		✓	✓
15	PB14	TXD_H		✓	✓	16	PB15	RXD_H		✓	✓
17	GND					18	GND				

7.1.3 Port C / ADC / SCI (P24)

Table 7-4 PortC Connector Pinout (P24)

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PC0	eMIOS[0]	✓	✓	✓	2	PC1	eMIOS[1]	✓	✓	✓
3	PC2	eMIOS[2]	✓	✓	✓	4	PC3	eMIOS[3]	✓	✓	✓
5	PC4	eMIOS[4]	✓	✓	✓	6	PC5	eMIOS[5]	✓	✓	✓
7	PC6	eMIOS[6]	✓	✓	✓	8	PC7	eMIOS[7]	✓	✓	✓
9	PC8	eMIOS[8]	✓	✓	✓	10	PC9	eMIOS[9]	✓	✓	✓
11	PC10	eMIOS[10]	✓	✓	✓	12	PC11	eMIOS[11]	✓	✓	✓
13	PC12	eMIOS[12]	✓	✓	✓	14	PC13	eMIOS[13]	✓	✓	✓
15	PC14	eMIOS[14]	✓	✓	✓	16	PC15	eMIOS[15]	✓	✓	✓
17	GND					18	GND				

Notes:

- *PC[0..11] is used to drive the LED dot matrix display if enabled. See section 3.10 for details.*
- *PC[0..2] and PC[7..9] are also used for the flexray interface. See section 3.9 for details.*

7.1.4 Port D / CAN / SCI / SPI (P15)

Table 7-5 PortD Connector Pinout (P15)

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PD0	CNTX_A	✓	✓	✓	2	PD1	CNRX_A	✓	✓	✓
3	PD2	CNRX_B	✓	✓	✓	4	PD3	CNTX_B	✓	✓	✓
5	PD4	CNTX_C	✓	✓	✓	6	PD5	CNRX_C	✓	✓	✓
7	PD6	TXD_A	✓	✓	✓	8	PD7	RXD_A	✓	✓	✓
9	PD8	TXD_B	✓	✓	✓	10	PD9	RXD_B	✓	✓	✓
11	PD10	PCS_B[2]	✓	✓	✓	12	PD11	PCS_B[1]	✓	✓	✓
13	PD12	PCS_B[0]	✓	✓	✓	14	PD13	SCK_B	✓	✓	✓
15	PD14	SOUT_B	✓	✓	✓	16	PD15	SIN_B	✓	✓	✓
17	GND					18	GND				

Notes:

- *PD2 is used for BOOTCFG data. See section 3.3.3*
- *PD0, PD1, PD4 and PD5 are used for the EVB CAN interface. See section 3.6*
- *PD6, PD7, PD8 and PD9 are used on the EVB SCI / LIN Physical Interfaces. See sections 3.7 and 3.8*
- *PD12, PD13, PD14, PD15 are used by the SBC SPI communication. See section 3.1.5*
-

7.1.5 PortE / SPI / eMIOS / EIM (Connector P31)

Table 7-6 PortE Connector Pinout (P31)

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PE0	PCS_A[2]	✓	✓	✓	2	PE1	PCS_A[1]	✓	✓	✓
3	PE2	PCS_A[0]	✓	✓	✓	4	PE3	SCK_A	✓	✓	✓
5	PE4	SOUT_A	✓	✓	✓	6	PE5	SIN_A	✓	✓	✓
7	PE6	CLKOUT	✓	✓	✓	8	PE7	---			✓
9	PE8	eMIOS[24]			✓	10	PE9	eMIOS[25]			✓
11	PE10	eMIOS[26]		✓	✓	12	PE11	eMIOS[27]		✓	✓
13	PE12	eMIOS[28]		✓	✓	14	PE13	eMIOS[29]		✓	✓
15	PE14	eMIOS[30]		✓	✓	16	PE15	eMIOS[31]		✓	✓
17	GND					18	GND				

Note – Port PE6 has a 33ohm series resistor close to the MCU on the MCU daughter-card to provide some CLKOUT impedance matching. This can be disabled with a jumper if required. See the daughter-card user manual for details.

7.1.6 Port F / EIM (Connector P17)

Table 7-7 Port F Connector Pinout (P17)

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PF0	RD_WR	✓	✓	✓	2	PF1	TA	✓	✓	✓
3	PF2	AD[8]	✓	✓	✓	4	PF3	AD[9]	✓	✓	✓
5	PF4	AD[10]	✓	✓	✓	6	PF5	AD[11]	✓	✓	✓
7	PF6	AD[12]	✓	✓	✓	8	PF7	AD[13]	✓	✓	✓
9	PF8	AD[14]	✓	✓	✓	10	PF9	AD[15]	✓	✓	✓
11	PF10	CS[1]	✓	✓	✓	12	PF11	CS[0]	✓	✓	✓
13	PF12	TS	✓	✓	✓	14	PF13	OE	✓	✓	✓
15	PF14	WE[0]	✓	✓	✓	16	PF15	WE[1]	✓	✓	✓
17	GND					18	GND				

Notes

- *PF[0..15] are used to drive the EBI. See section 3.5*
- *PF[0..11] are used for the Nexus interface. When using Nexus, the EBI must be disabled and nothing connected to these GPIO pins. See section 3.4*

7.1.7 Port G / EIM (Connector P25)

Table 7-8 Port F Connector Pinout (P25)

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PG0	AD[16]	✓	✓	✓	2	PG1	AD17]	✓	✓	✓
3	PG2	AD[18]	✓	✓	✓	4	PG3	AD[19]	✓	✓	✓
5	PG4	AD[20]	✓	✓	✓	6	PG5	AD[21]	✓	✓	✓
7	PG6	AD[22]	✓	✓	✓	8	PG7	AD[23]	✓	✓	✓
9	PG8	AD[24]	✓	✓	✓	10	PG9	AD[25]	✓	✓	✓
11	PG10	AD[26]	✓	✓	✓	12	PG11	AD[27]	✓	✓	✓
13	PG12	AD[28]	✓	✓	✓	14	PG13	AD[29]	✓	✓	✓
15	PG14	AD[30]	✓	✓	✓	16	PG15	AD[31]	✓	✓	✓
17	GND					18	GND				

Note – PG[0..15] are used to drive the EBI. See section 3.5

7.1.8 Port H / ADC / API / EIM (Connector P29)

Table 7-9 Port H Connector Pinout

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PH0	AN[27]	✓	✓	✓	2	PH1	AN[26]	✓	✓	✓
3	PH2	AN[25]	✓	✓	✓	4	PH3	AN[24]	✓	✓	✓
5	PH4	AN[23]	✓	✓	✓	6	PH5	AN[22]	✓	✓	✓
7	PH6	AN[21]	✓	✓	✓	8	PH7	AN[20]	✓	✓	✓
9	PH8	AN[19]	✓	✓	✓	10	PH9	AN[18]	✓	✓	✓
11	PH10	AN[17]	✓	✓	✓	12	PH11	AN[16]	✓	✓	✓
13	PH12	PCS_D[5]			✓	14	PH13	---			✓
15	PH14	WE[2]		✓	✓	16	PH15	WE[3]		✓	✓
17	GND					18	GND				

Note – PH[14..15] are used to drive the EBI (32-bit data port mode). See section 3.5

7.1.9 Port J / EIM / SPI (Connector P23)

Table 7-10 Port J Connector Pinout

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	144	176	208		GPIO	1st Alt	144	176	208
1	PJ0	AD[0]			✓	2	PJ1	AD[1]			✓
3	PJ2	AD[2]			✓	4	PJ3	AD[3]			✓
5	PJ4	AD[4]		✓	✓	6	PJ5	AD[5]		✓	✓
7	PJ6	AD[6]		✓	✓	8	PJ7	AD[7]		✓	✓
9	PJ8	PCS_D[4]		✓	✓	10	PJ9	PCS_D[3]		✓	✓
11	PJ10	PCS_D[2]		✓	✓	12	PJ11	PCS_D[1]		✓	✓
13	PJ12	PCS_D[0]		✓	✓	14	PJ13	SCK_D		✓	✓
15	PJ14	SOUT_D		✓	✓	16	PJ15	SIN_D		✓	✓
17	GND					18	GND				

Note –PJ[0..7]are used to drive the EBI (32-bit data port mode). See section 3.5

7.1.10 Port K / EXTAL32 / XTAL32 (Connector P33)

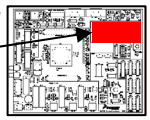
Table 7-11 Port K Connector Pinout

Pin	Function		Availability			Pin	Function		Availability		
	GPIO	1st Alt	100	144	208		GPIO	1st Alt	100	144	208
1	PK0	EXTAL32			✓	2	PK1	EXTAL32			✓
17	GND					18	GND				

Note – The EXTAL32 and XTAL32 function is available on pins PA14 and PA15 for all packages that do not provide PortK.

7.2 Prototyping Area and User LED's / Switches

The prototyping area is located on the right hand side of the EVB, above the user connectors.



There is a rectangular prototype area on the EVB, consisting of a 0.1inch pitch array of through-hole plated pads. Power from all three voltage regulators is readily accessible along with GND. This area is ideal for the addition of any custom circuitry. Adapters are available to convert SMD devices to 0.1inch pitch through-hole.

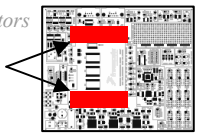
Note the power supply lines to the prototype area are connected directly to the regulator outputs and not connected to the jumpered MCU supply.

There are 4 active low user LED's DS4, DS5, DS6 and DS7, These are driven by connecting a logic 0 signal to the corresponding pin on 0.1" header P10 (user LED's).

There are 4 active high pushbutton switches SW2, SW3, SW4 and SW5 which will drive 5V onto the respective pins on 0.1" connector P11 when pressed. The switch outputs are pulled to GND with a 10K resistor network.

8. Daughter Card Connectors (P9, P22)

The daughter card connectors are located roughly in the centre of the board. .



As mentioned previously, there are two 120-way expansion connectors fitted to the EVB, allowing connection of an MCU daughter card or another board providing functionality enhancement.

The part numbers of possible connectors are detailed in Table 8-1 below.

Table 8-1 Expansion Connector Part Numbers

Connector Location	Height	Pitch	TYCO / AMP Part Number
EVB	8mm	0.8mm	179031-5
Daughter Card	9mm	0.8mm	5-179009-5
	13mm	0.8mm	5-179010-5

The pinout of the expansion connectors is detailed below for reference.

Table 8-2 Daughter Card Connector 1

Pin Number	Signal Name (0dd)	Signal Name (Even)
1	PB2	PB12
3	PK0	PA13
5	PA8	3.3V-SR
7	VDDA	VDDA
9	VDD	VDD
11	3.3V-SR	PB3
13	PB13	PK1
15	VDD	VDD
17	PA12	GND
19	PB4	PB0
21	PA15	PA11
23	GND	PA9
25	PA6	PA7
27	PB5	PB1
29	PA14	GND
31	PA10	PA3
33	PA4	PA5
35	GND	MCU-RST
37	--	PA0
39	PA1	PA2
41	PH10	GND
43	PH11	PH12
45	PH13	PJ13
47	GND	PJ14
49	PH9	PJ15
51	VDDE2	VDDE2
53	PJ11	GND
55	PJ12	PH8
57	PJ10	PH5
59	GND	PH6

Pin Number	Signal Name (0dd)	Signal Name (Even)
61	PH7	PH3
63	PH4	PJ8
65	PJ9	GND
67	VDDE2	VDDE2
69	PH0	PH1
71	GND	PH2
73	PG12	PG13
75	PG14	PG15
77	PF8	GND
79	PF12	PF15
81	VDDE2	VDDE2
83	GND	PG9
85	PG10	PG11
87	PF7	PF11
89	PF14	GND
91	PG0	PG3
93	VDDE2	VDDE2
95	5.0V-SR	PG8
97	PJ7	PF10
99	PF13	PH15
101	PG2	5.0V-SR
103	PG5	PG7
105	VDD	VDD
107	P12V	PF6
109	PF9	PH14
111	VDDR	VDDR
113	PG1	P12V
115	PG4	PG6
117	VDD	VDD
119	TGT-RST	RST-OUT

Table 8-3 Daughter Card Connector 2

Pin Number	Signal Name (0dd)	Signal Name (Even)
1	PB6	PB10
3	PB15	PC3
5	PC7	GND
7	VDDE1	VDDE1
9	VDD	VDD
11	GND	PC10
13	PB7	PB11
15	PC0	PC4
17	PC8	GND
19	VDD	VDD
21	PC11	PC12
23	GND	PB8
25	PB14	PC1
27	PC5	PC9
29	PC13	GND
31	PC14	PB9
33	VDDE1	VDDE1
35	GND	PC2
37	PC6	PC15
39	PD0	PD1
41	PD2	GND
43	VDDE1	VDDE1
45	PD3	PD4
47	GND	PD5
49	PD6	PD7
51	PD9	PD8
53	PD10	GND
55	VDDE1	VDDE1
57	PD11	PD12
59	PE7	PD13

Pin Number	Signal Name (0dd)	Signal Name (Even)
61	PE8	PE9
63	PD14	PE11
65	PE10	GND
67	PE12	PD15
69	VDDE1	VDDE1
71	GND	PE0
73	PE13	PE1
75	PE2	PE14
77	PE3	GND
79	PE15	PE5
81	VDDE3	VDDE3
83	GND	PJ2
85	PJ0	PF0
87	VDD33	VDD33
89	PE4	GND
91	CLK-IN	PJ6
93	PJ4	PJ1
95	GND	PF1
97	VPP	VPP
99	PE6	PF5
101	PJ3	GND
103	PF2	TDI
105	VDD	VDD
107	1.5V-SR	TCLK
109	VDDSYN	VDDSYN
111	PJ5	PF4
113	VDDE3	1.5V-SR
115	VDDE3	PF3
117	JCOMP	TDO
119	TMS	VDD

Notes:

- *Power connections shown with red shading are from the outputs of the respective MCU power jumpers. The power connections shown in orange shading (1.5V-SR, 3.3V-SR, 5.0V-SR and P12V) are direct outputs from the regulators / main power input and are not jumpered. These are designed to drive any non-MCU daughter card circuitry.*
- *The TGT-RESET signal provides a mechanism of driving the MCU reset line from a non open-drain source. This can be used by a target system to control the system reset. RST-OUT is a driven reset signal which should be connected to Reset-in of any custom devices on the daughter card. The MCU-Reset line provides a direct connection to the bidirectional MCU Reset pin. Extreme caution should be exercised if this pin is used.*
- *All of the MCU signals with the exception of VRH, VRL, EXTAL, XTAL, and REFBYPC, are routed to the connectors.*

Appendix

The EVB and daughtercard BOM (Bill of Materials) and Schematics are detailed in the Appendix as shown below.

Appendix ID	Description
Appendix A -	EVB Schematics (Rev E0)
Appendix B -	EVB Bill Of Materials
Appendix C -	144QFP Daughtercard Schematics (Rev B1)
Appendix D -	144QFP Daughtercard Bill Of Materials
Appendix E -	176QFP Daughtercard Schematics (Rev C0)
Appendix F -	176QFP Daughtercard Bill Of Materials
Appendix G -	208BGA Daughtercard Schematics (Rev B1)
Appendix H -	208BGA Daughtercard Bill Of Materials

Appendix A - EVB Schematics

MPC5510 Evaluation Board

Table Of Contents:

POWER SUPPLY 1 (INPUT, LINEAR AND SWITCHERS)	SHEET 2
POWER SUPPLY 2 (SBC AND VOLTAGE ROUTING)	SHEET 3
EVB CLOCK OSCILLATOR AND SMA CONNECTORS	SHEET 4
RESET GENERATION, CONTROL AND BOOTCFG	SHEET 5
JTAG AND NEXUS CONNECTORS	SHEET 6
SRAM	SHEET 7
CAN TRANSCEIVERS	SHEET 8
SCI AND LIN TRANSCEIVERS	SHEET 9
FLEXRAY TRANSCEIVERS	SHEET 10
DAUGHTERCARD CONNECTORS	SHEET 11
USER IO CONNECTORS (PORT HEADERS)	SHEET 12
USER (PROTOTYPE) AREA AND I/O PEIPHERALS	SHEET 13
TERMINATION RESISTORS	SHEET 14

Revision Information

Rev	Date	Designer	Comments
0.1	10 Dec 2006	A. Robertson	Provisional (Pre Back Annotation)
0.2	03 Jan 2007	A. Robertson	Additional power on DC. Proto Release - PCB RevA
B0	03 Jul 2007	A. Robertson	FCL Prodn Release - PCB RevB
C0	11 Jul 2007	A. Robertson	Fixed connectivity on Power Jack (P28)
D0	31 Jul 2007	A. Robertson	Changed Power Supply Caps (C13, C14, C15 & C20)
D1	07 Aug 2007	A. Robertson	Changed P3 and P4 from 2mm to 2.54mm
D2	10 Sept 2007	A. Robertson	Post FCL Tidy Up. Correction to J13 / J15
E0	12 Sept 2007	A. Robertson	Released to Production - PCB RevE

Notes:

- All components and board processes are to be ROHS compliant
- Resistor networks are donated RNx. All resistor networks are SMD 1206 style package.
- Variable resistors are denoted RVx
- All decoupling caps less than 0.1uF are COG unless otherwise stated
- All decoupling caps greater than 0.1uF are X7R unless otherwise stated
- All connectors are denoted Px. All connectors and headers are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2
- All Switches are denoted SWx
- All test points are denoted TPx
- Test Point Vias are denoted TPVx

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Note:

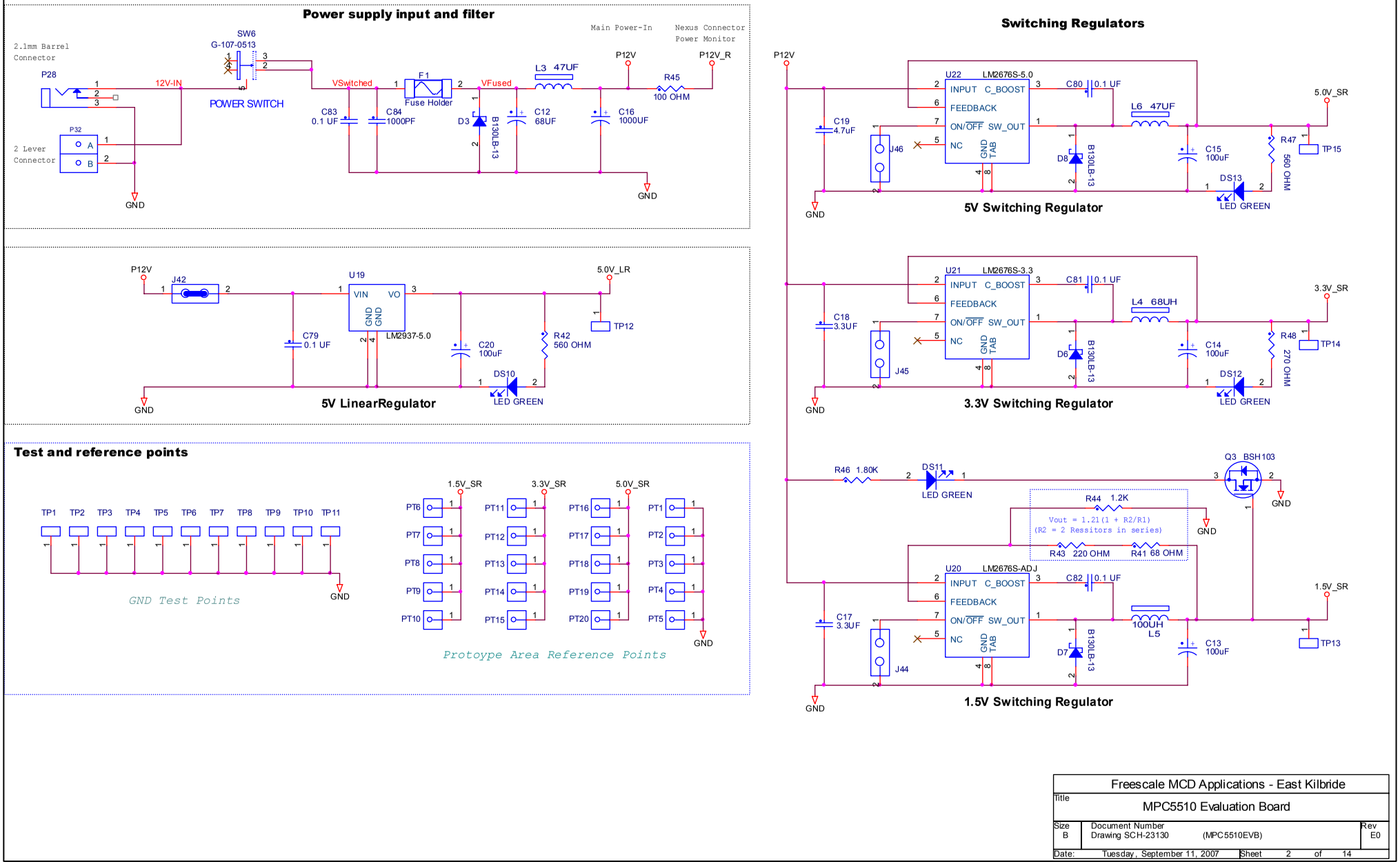
These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale MPC5510 family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

freescale semiconductor

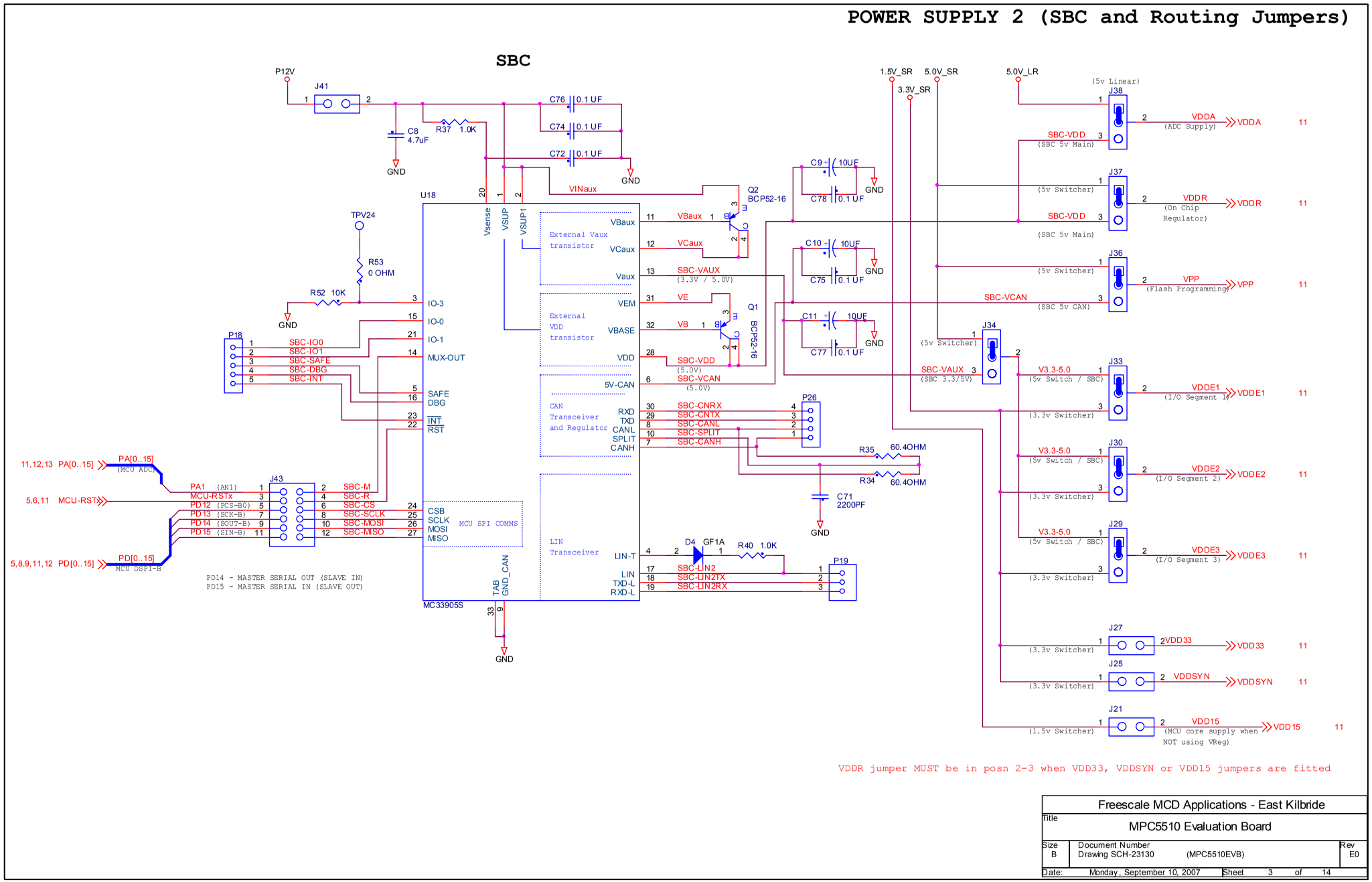
Transportation & Standard Products Group
MCD Applications East Kilbride
Colvilles Road, Kelvin Industrial Estate, East Kilbride G75 0TG

Designer: A. Robertson	Drawing Title: MPC5510 Evaluation Board	
Drawn by: A. Robertson	Page Title: Front Page Contents and Notes	
Approved: A. Robertson	Size: B	Document Number: SCH-23130 PDF: SPF-23130 — Rev: E0
	Date: Wednesday, September 12, 2007	Sheet 1 of 14

POWER SUPPLY 1 (Input and Non-SBC)



Freescale MCD Applications - East Kilbride		
Title: MPC5510 Evaluation Board		
Size: B	Document Number: Drawing SCH-23130 (MPC5510EVB)	Rev: E0
Date: Tuesday, September 11, 2007	Sheet 2 of 14	


POWER SUPPLY 2 (SBC and Routing Jumpers)
SBC
P12V
J41
C8 4.7uF
R37 1.0K
C76 0.1 UF
C74 0.1 UF
C72 0.1 UF
GND
VINaux
U18
TPV24
R53 0 OHM
R52 10K
P18
SBC-IO0
SBC-IO1
SBC-SAFE
SBC-DBG
SBC-INT
IO-3
IO-0
IO-1
MUX-OUT
SAFE
DBG
INT
RST
Vsense
VSUP
VSUP1
External Vaux transistor
VBaux
VCaux
Vaux
External VDD transistor
VEM
VBASE
VDD
5V-CAN
CAN Transceiver and Regulator
RXD
TXD
CANL
SPLIT
CANH
LIN Transceiver
LIN-T
LIN
TXD-L
RXD-L
CSB
SCLK
MOSI
MISO
MCU SPI COMMS
TAB
GND_CAN
MC33905S
Q2 BCP52-16
Q1 BCP52-16
SBC-VAUX (3.3V / 5.0V)
SBC-VDD (5.0V)
SBC-VCAN (5.0V)
SBC-CNRX
SBC-CNTX
SBC-CANL
SBC-SPLIT
SBC-CANH
P26
R35 60.4OHM
R34 60.4OHM
C71 2200PF
D4 GF1A
R40 1.0K
P19
SBC-LIN2
SBC-LIN2TX
SBC-LIN2RX
11,12,13 PA[0..15]
PA[0..15] (MCU ADC)
5,6,11 MCU-RST
5,8,9,11,12 PD[0..15]
PD[0..15] MCU DSPI-B
J43
PA1 (AN1)
MCU-RSTx
PD12 (PCS-B0)
PD13 (SCK-B)
PD14 (SOUT-B)
PD15 (SIN-B)
SBC-M
SBC-R
SBC-CS
SBC-SCLK
SBC-MOSI
SBC-MISO
PD14 - MASTER SERIAL OUT (SLAVE IN)
PD15 - MASTER SERIAL IN (SLAVE OUT)
1.5V_SR
3.3V_SR
5.0V_SR
5.0V_LR
C9 10UF
C78 0.1 UF
C10 10UF
C75 0.1 UF
C11 10UF
C77 0.1 UF
J34
(5v Switcher)
SBC-VAUX (SBC 3.3/5V)
SBC-VCAN (SBC 5v CAN)
(5v Linear)
J38
VDDA
(ADC Supply)
SBC-VDD (SBC 5v Main)
J37
VDDR
(On Chip Regulator)
J36
VPP
(Flash Programming)
J33
V3.3-5.0
(5v Switch / SBC)
VDDE1
(I/O Segment 1)
(3.3v Switcher)
J30
VDDE2
(I/O Segment 2)
J29
VDDE3
(I/O Segment 3)
J27
VDD33
J25
VDDSYN
J21
VDD15
(MCU core supply when NOT using VReg)
VDDR jumper MUST be in posn 2-3 when VDD33, VDDSYN or VDD15 jumpers are fitted
Freescale MCD Applications - East Kilbride
Title
MPC5510 Evaluation Board
Size B
Document Number Drawing SCH-23130 (MPC5510EVB)
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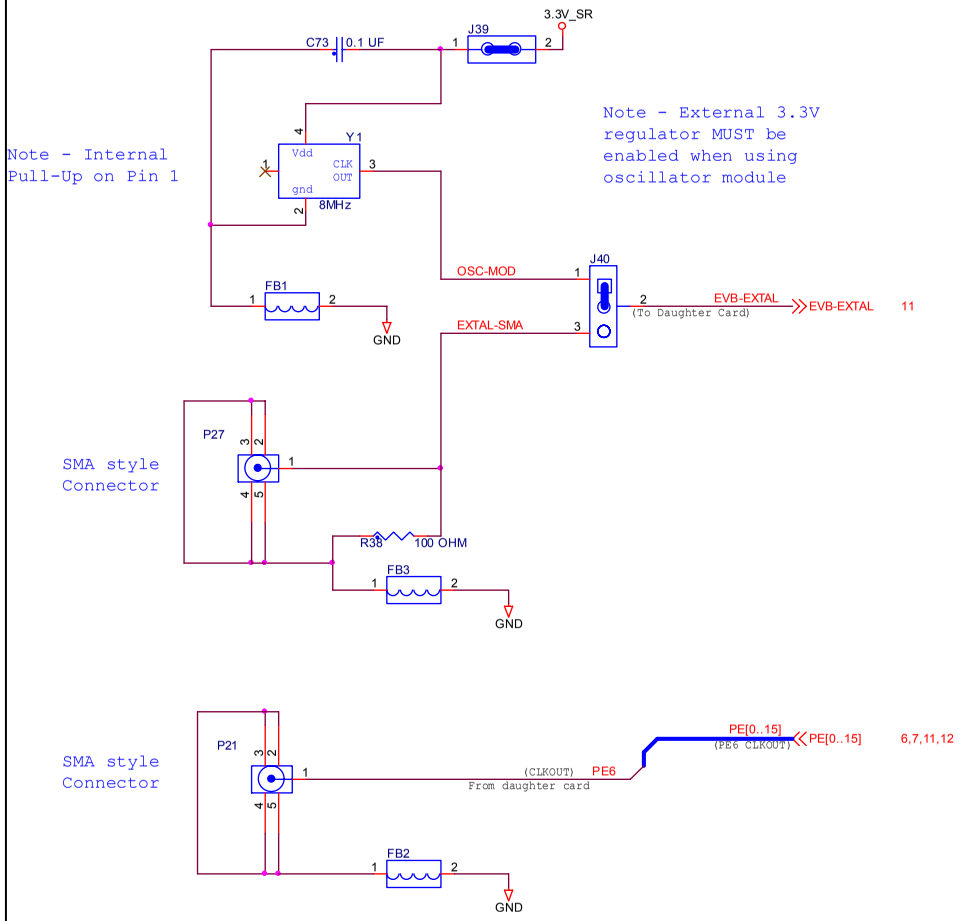
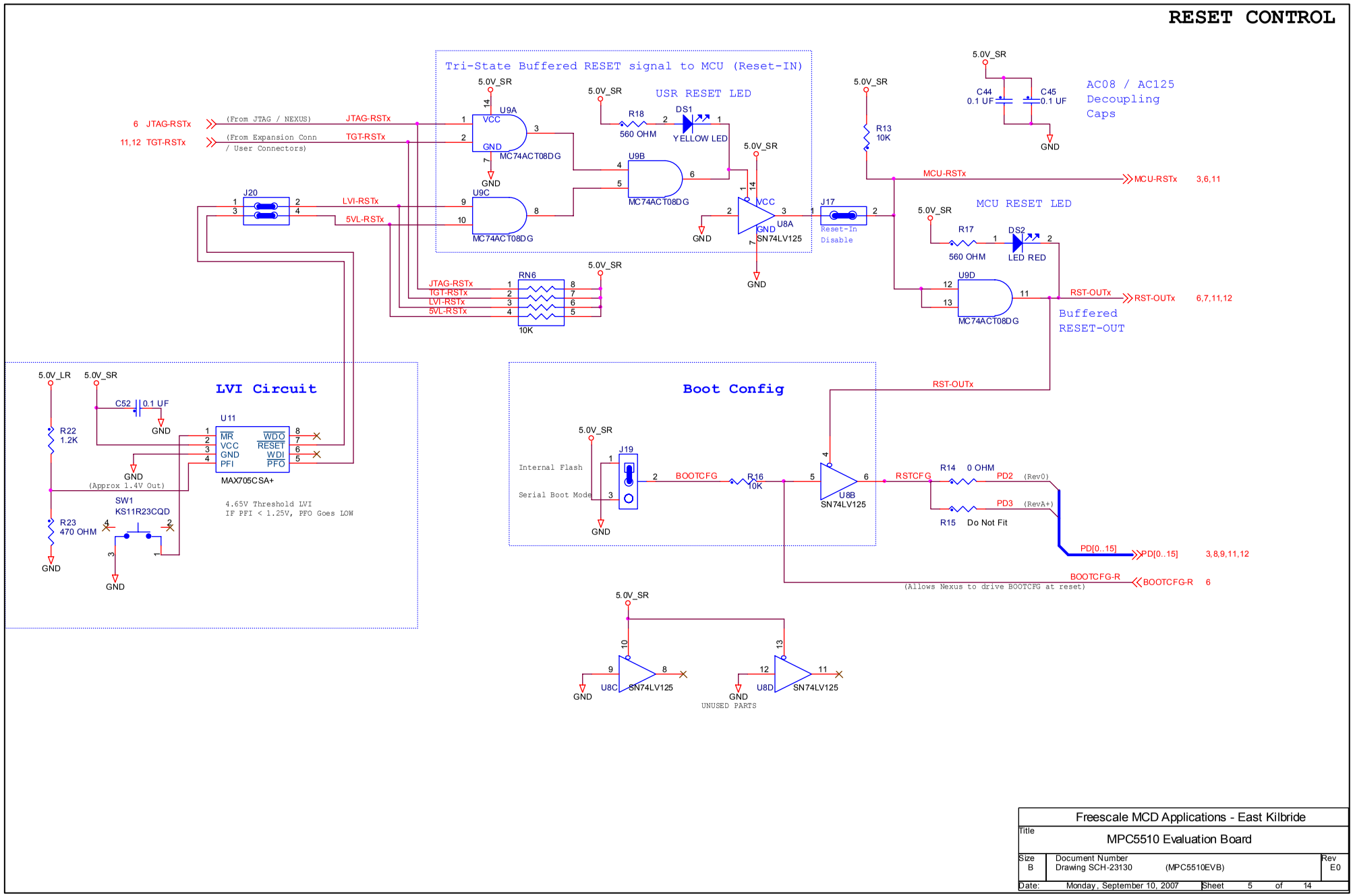
CLOCK CIRCUITRY



Freescale MCD Applications - East Kilbride		
Title: MPC5510 Evaluation Board		
Size: B	Document Number: Drawing SCH-23130 (MPC5510EVB)	Rev: E0
Date: Monday, September 10, 2007	Sheet 4 of 14	


RESET CONTROL
Tri-State Buffered RESET signal to MCU (Reset-IN)
USR RESET LED
MCU RESET LED
AC08 / AC125 Decoupling Caps
LVI Circuit
Boot Config
Buffered RESET-OUT
5.0V_SR
5.0V_LR
6 JTAG-RSTx
11,12 TGT-RSTx
(From JTAG / NEXUS)
(From Expansion Conn / User Connectors)
JTAG-RSTx
TGT-RSTx
LVI-RSTx
5VL-RSTx
U9A
U9B
U9C
U8A
MC74ACT08DG
SN74LV125
R18 560 OHM
DS1 YELLOW LED
R13 10K
C44 0.1 UF
C45 0.1 UF
GND
J20
J17
Reset-In Disable
MCU-RSTx
MCU-RSTx 3,6,11
R17 560 OHM
DS2 LED RED
U9D
RST-OUTx
RST-OUTx 6,7,11,12
RN6 10K
C52 0.1 UF
U11
MAX705CSA+
R22 1.2K
R23 470 OHM
SW1 KS11R23CQD
(Approx 1.4V Out)
4.65V Threshold LVI
IF PFI < 1.25V, PFO Goes LOW
J19
Internal Flash
Serial Boot Mode
BOOTCFG
R16 10K
U8B
RSTCFG
R14 0 OHM
PD2 (Rev0)
PD3 (RevA+)
R15 Do Not Fit
PD[0..15]
PD[0..15] 3,8,9,11,12
BOOTCFG-R
BOOTCFG-R 6
(Allows Nexus to drive BOOTCFG at reset)
U8C
U8D
UNUSED PARTS
Freescale MCD Applications - East Kilbride
Title
MPC5510 Evaluation Board
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Rev E0
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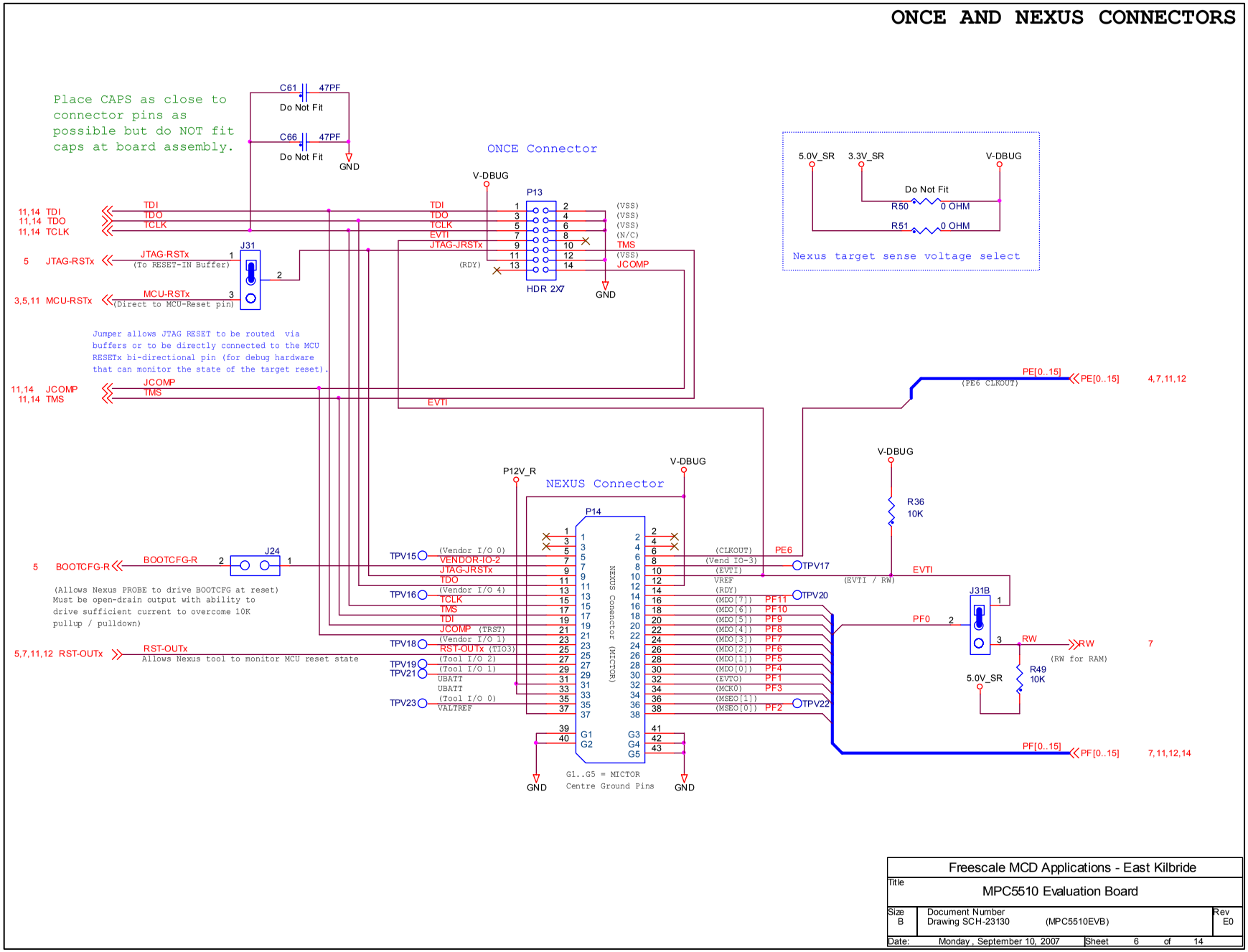
ONCE AND NEXUS CONNECTORS
Place CAPS as close to connector pins as possible but do NOT fit caps at board assembly.
C61 47PF
Do Not Fit
C66 47PF
Do Not Fit
GND
ONCE Connector
V-DBUG
P13
HDR 2X7
TDI
TDO
TCLK
EVTI
JTAG-JRSTx
TMS
JCOMP
(VSS)
(N/C)
(RDY)
11,14 TDI
11,14 TDO
11,14 TCLK
5 JTAG-RSTx
JTAG-RSTx
(To RESET-IN Buffer)
J31
3,5,11 MCU-RSTx
MCU-RSTx
(Direct to MCU-Reset pin)
Jumper allows JTAG RESET to be routed via buffers or to be directly connected to the MCU RESETx bi-directional pin (for debug hardware that can monitor the state of the target reset).
11,14 JCOMP
11,14 TMS
5.0V_SR
3.3V_SR
V-DBUG
Do Not Fit
R50 0 OHM
R51 0 OHM
Nexus target sense voltage select
PE[0..15]
(PE6 CLKOUT)
PE[0..15] 4,7,11,12
V-DBUG
R36
10K
P12V_R
NEXUS Connector
P14
NEXUS Connector (MICTOR)
TPV15
TPV16
TPV17
TPV18
TPV19
TPV20
TPV21
TPV22
TPV23
(Vendor I/O 0)
VENDOR-IO-2
(Vendor I/O 4)
(Vendor I/O 1)
RST-OUTx (TIO3)
(Tool I/O 2)
(Tool I/O 1)
UBATT
(Tool I/O 0)
VALTREF
(CLKOUT)
(Vend IO-3)
(EVTI)
VREF
(RDY)
(MDO[7]) PF11
(MDO[6]) PF10
(MDO[5]) PF9
(MDO[4]) PF8
(MDO[3]) PF7
(MDO[2]) PF6
(MDO[1]) PF5
(MDO[0]) PF4
(EVTO) PF1
(MCKO) PF3
(MSEO[1])
(MSEO[0]) PF2
PE6
EVTI
(EVTI / RW)
J24
5 BOOTCFG-R
BOOTCFG-R
(Allows Nexus PROBE to drive BOOTCFG at reset) Must be open-drain output with ability to drive sufficient current to overcome 10K pullup / pulldown)
5,7,11,12 RST-OUTx
RST-OUTx
Allows Nexus tool to monitor MCU reset state
J31B
PF0
RW
RW 7
(RW for RAM)
R49
10K
5.0V_SR
PF[0..15]
PF[0..15] 7,11,12,14
G1..G5 = MICTOR Centre Ground Pins
Freescale MCD Applications - East Kilbride
Title
MPC5510 Evaluation Board
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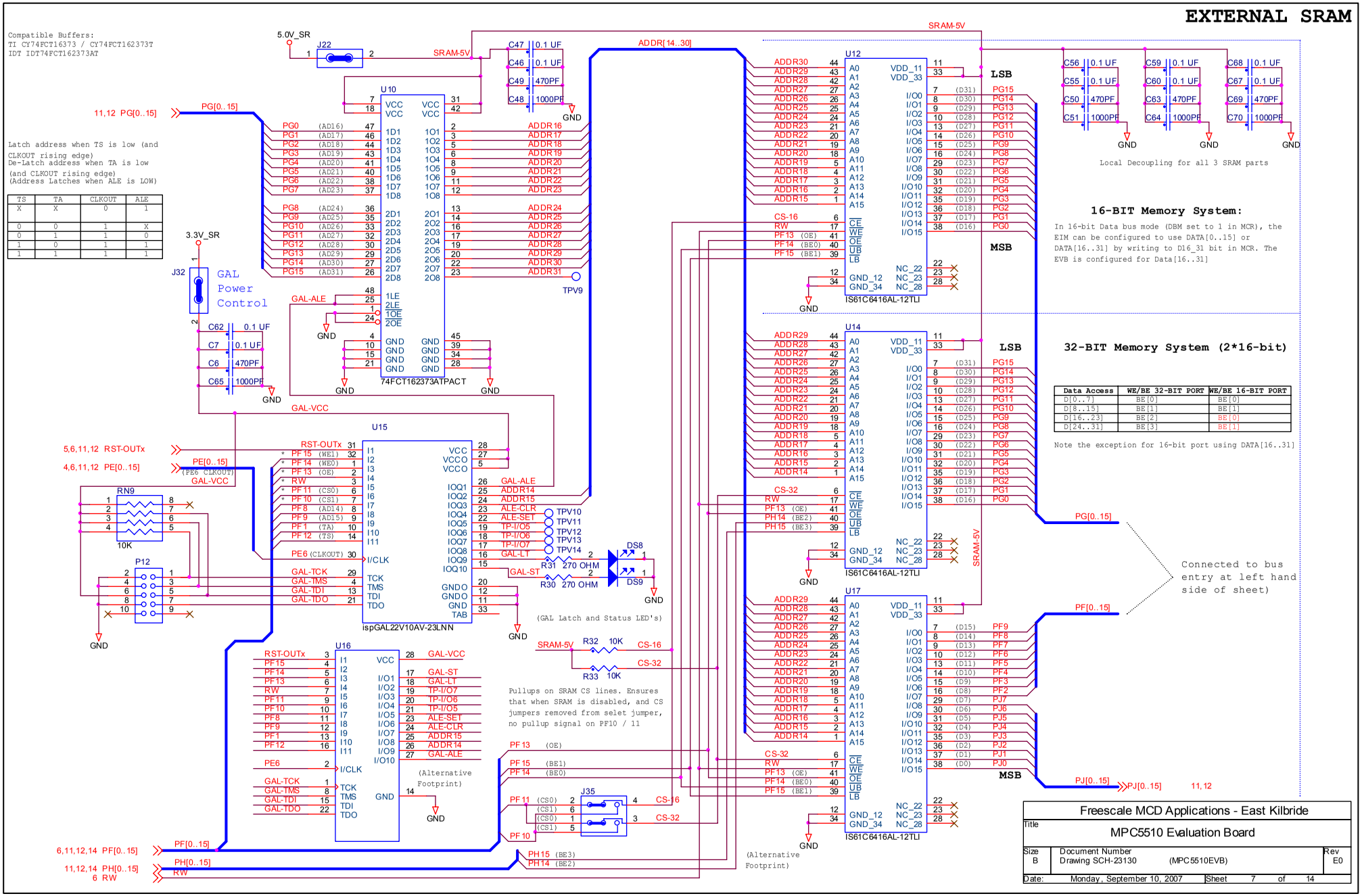
EXTERNAL SRAM
Compatible Buffers:
TI CY74FCT16373 / CY74FCT162373T
IDT IDT74FCT162373AT
Latch address when TS is low (and CLKOUT rising edge)
De-Latch address when TA is low (and CLKOUT rising edge)
(Address Latches when ALE is LOW)
TS TA CLKOUT ALE
X X 0 1
0 0 1 X
0 1 1 0
1 0 1 1
1 1 1 1
5.0V_SR
3.3V_SR
SRAM-5V
GAL Power Control
GAL-VCC
ADDR[14..30]
PG[0..15]
74FCT162373ATPACT
ispGAL22V10AV-23LNN
IS61C6416AL-12TLI
LSB
MSB
Local Decoupling for all 3 SRAM parts
16-BIT Memory System:
In 16-bit Data bus mode (DBM set to 1 in MCR), the EIM can be configured to use DATA[0..15] or DATA[16..31] by writing to D16_31 bit in MCR. The EVB is configured for Data[16..31]
32-BIT Memory System (2*16-bit)
Data Access | WE/BE 32-BIT PORT | WE/BE 16-BIT PORT
D[0..7] | BE[0] | BE[0]
D[8..15] | BE[1] | BE[1]
D[16..23] | BE[2] | BE[0]
D[24..31] | BE[3] | BE[1]
Note the exception for 16-bit port using DATA[16..31]
Connected to bus entry at left hand side of sheet)
(GAL Latch and Status LED's)
Pullups on SRAM CS lines. Ensures that when SRAM is disabled, and CS jumpers removed from selet jumper, no pullup signal on PF10 / 11
(Alternative Footprint)
Freescale MCD Applications - East Kilbride
MPC5510 Evaluation Board
Size B
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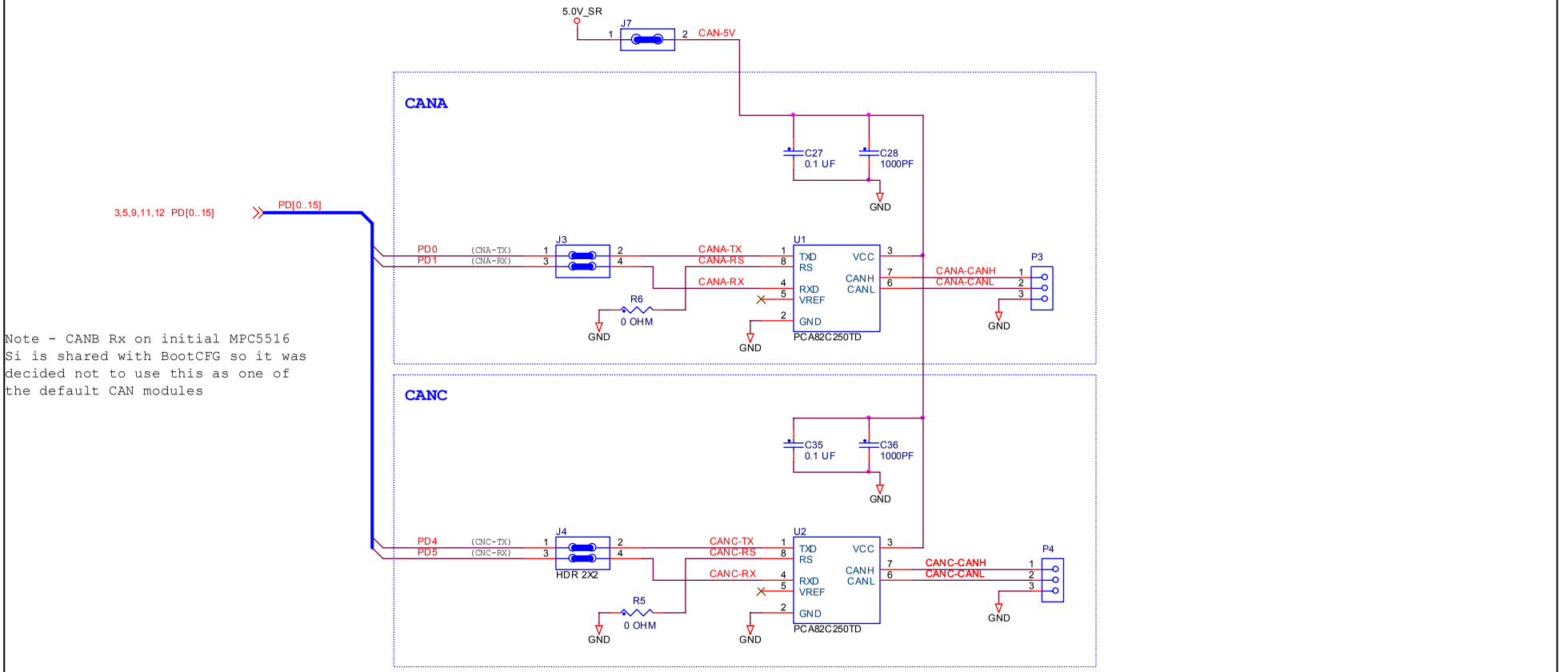
CAN PHYSICAL INTERFACE



Freescale MCD Applications - East Kilbride		
Title: MPC5510 Evaluation Board		
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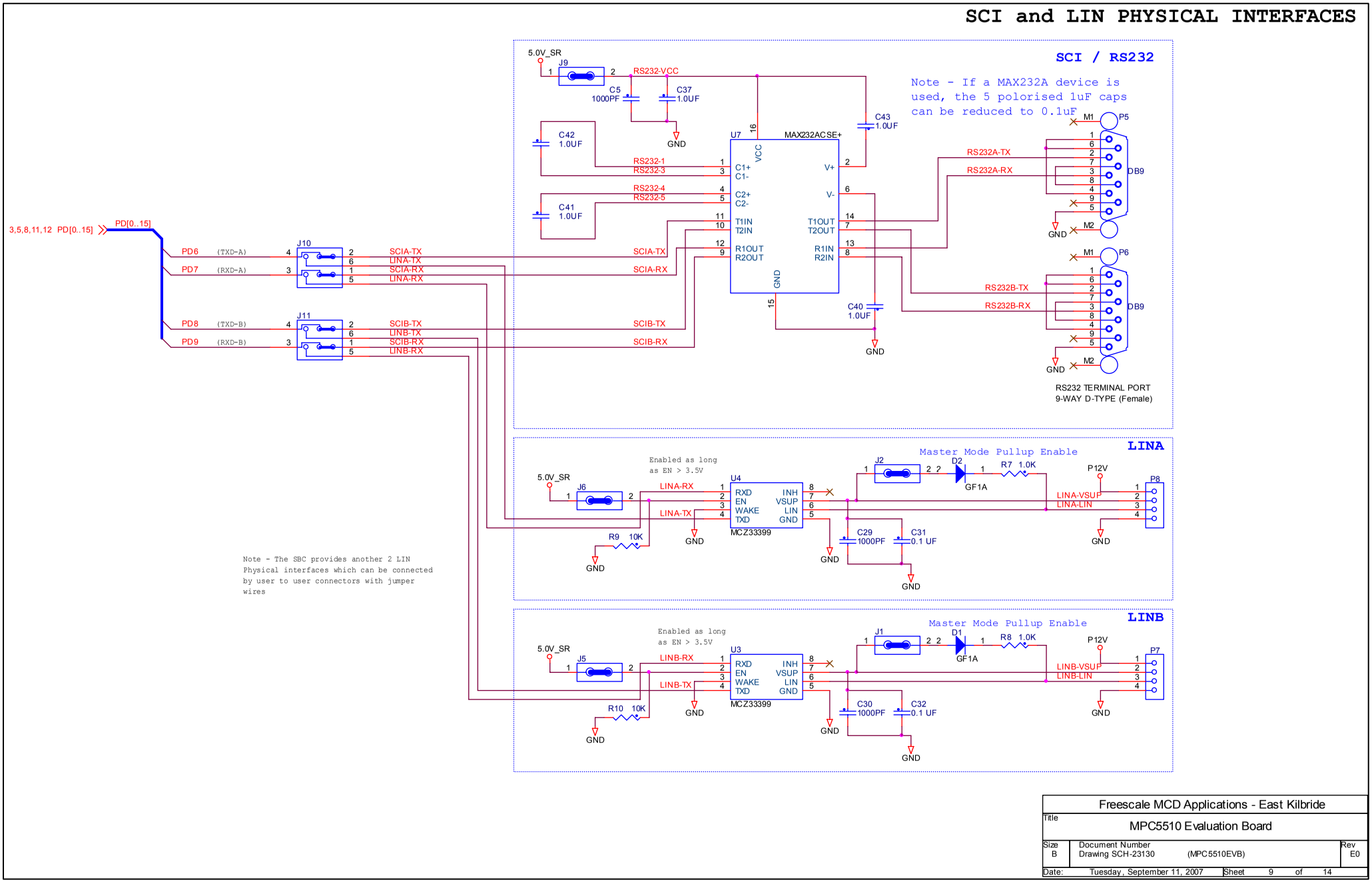
SCI and LIN PHYSICAL INTERFACES
SCI / RS232
Note - If a MAX232A device is used, the 5 polorised 1uF caps can be reduced to 0.1uF
5.0V_SR
J9
RS232-VCC
C5 1000PF
C37 1.0UF
C43 1.0UF
C42 1.0UF
C41 1.0UF
C40 1.0UF
U7
MAX232ACSE+
VCC
GND
C1+
C1-
C2+
C2-
V+
V-
T1IN
T2IN
T1OUT
T2OUT
R1OUT
R2OUT
R1IN
R2IN
RS232-1
RS232-3
RS232-4
RS232-5
SCIA-TX
SCIA-RX
SCIB-TX
SCIB-RX
RS232A-TX
RS232A-RX
RS232B-TX
RS232B-RX
P5
P6
DB9
M1
M2
RS232 TERMINAL PORT
9-WAY D-TYPE (Female)
3,5,8,11,12 PD[0..15]
PD[0..15]
PD6 (TXD-A)
PD7 (RXD-A)
PD8 (TXD-B)
PD9 (RXD-B)
J10
J11
LINA-TX
LINA-RX
LINB-TX
LINB-RX
LINA
Master Mode Pullup Enable
Enabled as long as EN > 3.5V
J6
J2
D2
GF1A
R7 1.0K
R9 10K
U4
RXD
EN
WAKE
TXD
INH
VSUP
LIN
GND
MCZ33399
C29 1000PF
C31 0.1 UF
P12V
P8
LINA-VSUP
LINA-LIN
LINB
J5
J1
D1
R8 1.0K
R10 10K
U3
C30 1000PF
C32 0.1 UF
P7
LINB-VSUP
LINB-LIN
Note - The SBC provides another 2 LIN Physical interfaces which can be connected by user to user connectors with jumper wires
Freescale MCD Applications - East Kilbride
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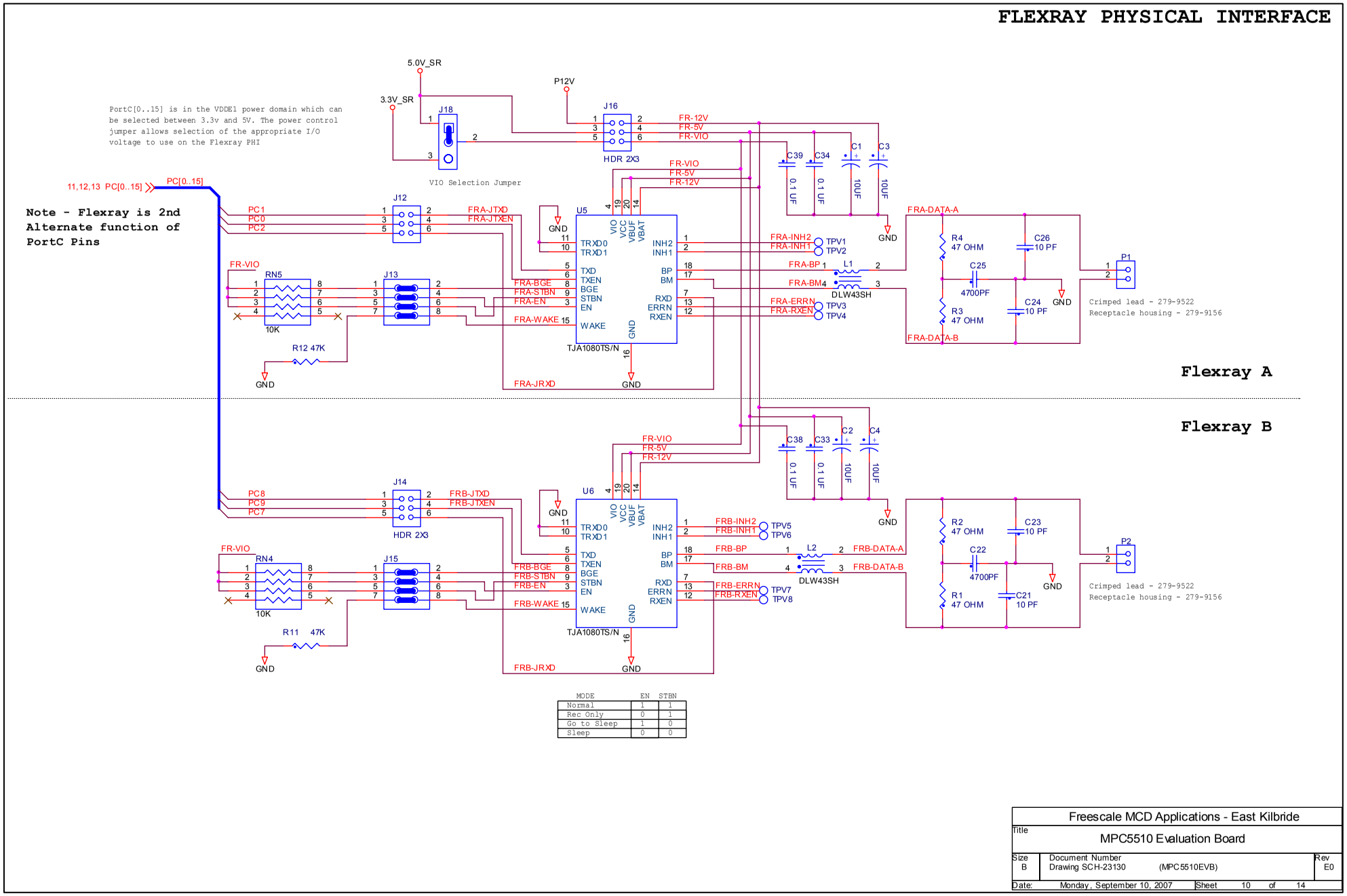
FLEXRAY PHYSICAL INTERFACE
PortC[0..15] is in the VDDE1 power domain which can be selected between 3.3v and 5V. The power control jumper allows selection of the appropriate I/O voltage to use on the Flexray PHI
VIO Selection Jumper
Note - Flexray is 2nd Alternate function of PortC Pins
11,12,13 PC[0..15]
PC[0..15]
Flexray A
Flexray B
TJA1080TS/N
DLW43SH
HDR 2X3
Crimped lead - 279-9522
Receptacle housing - 279-9156
MODE EN STBN
Normal 1 1
Rec Only 0 1
Go to Sleep 1 0
Sleep 0 0
Freescale MCD Applications - East Kilbride
MPC5510 Evaluation Board
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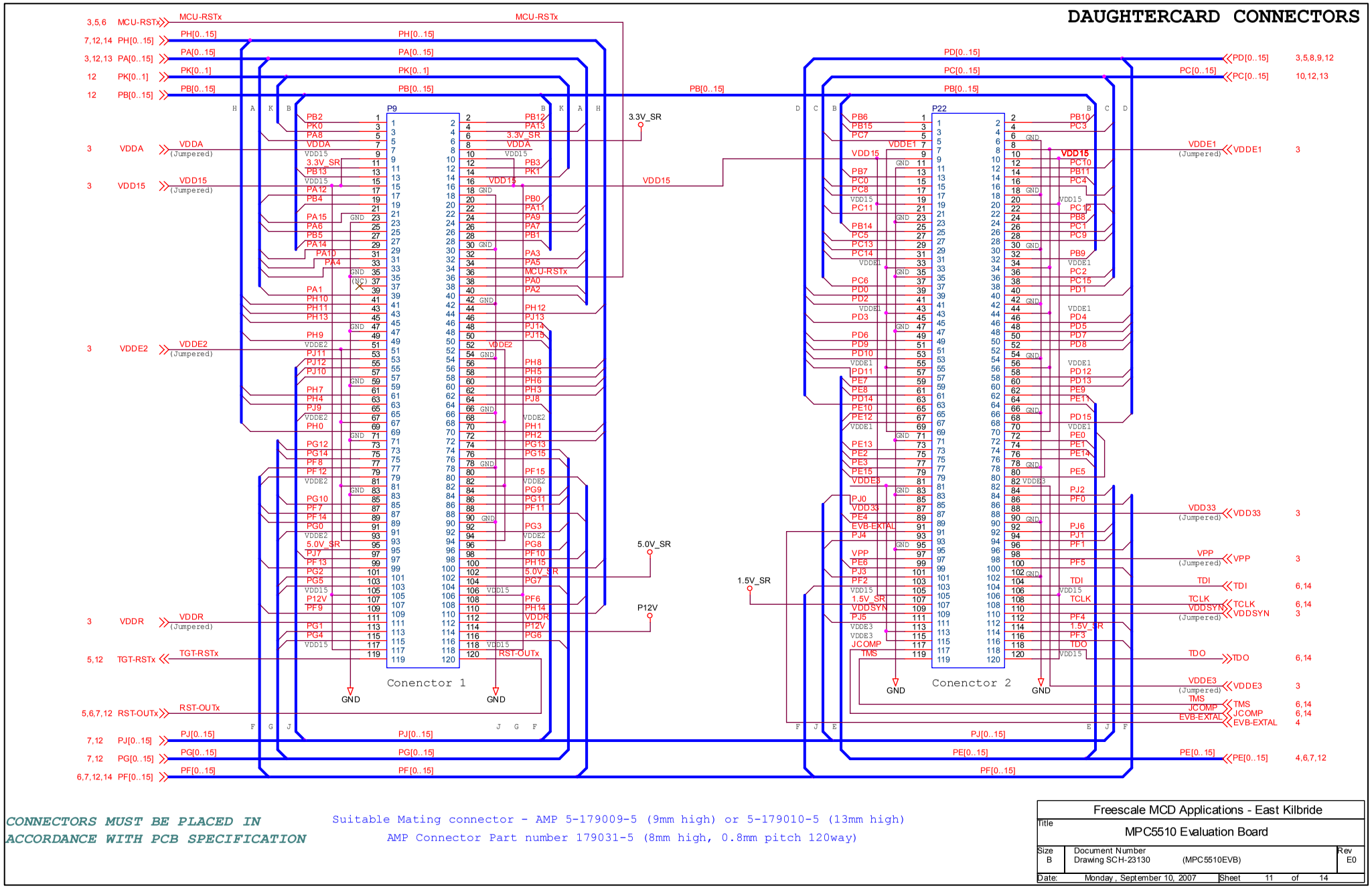
DAUGHTERCARD CONNECTORS
MCU-RSTx
PH[0..15]
PA[0..15]
PK[0..1]
PB[0..15]
PD[0..15]
PC[0..15]
3.3V_SR
VDDA
VDD15
VDDE2
5.0V_SR
P12V
VDDR
TGT-RSTx
RST-OUTx
PJ[0..15]
PG[0..15]
PF[0..15]
1.5V_SR
VDDE1
VDD33
VPP
TDI
TCLK
VDDSYN
TDO
VDDE3
TMS
JCOMP
EVB-EXTAL
P9
P22
Conenctor 1
Conenctor 2
GND
Suitable Mating connector - AMP 5-179009-5 (9mm high) or 5-179010-5 (13mm high)
AMP Connector Part number 179031-5 (8mm high, 0.8mm pitch 120way)
CONNECTORS MUST BE PLACED IN ACCORDANCE WITH PCB SPECIFICATION
Freescale MCD Applications - East Kilbride
MPC5510 Evaluation Board
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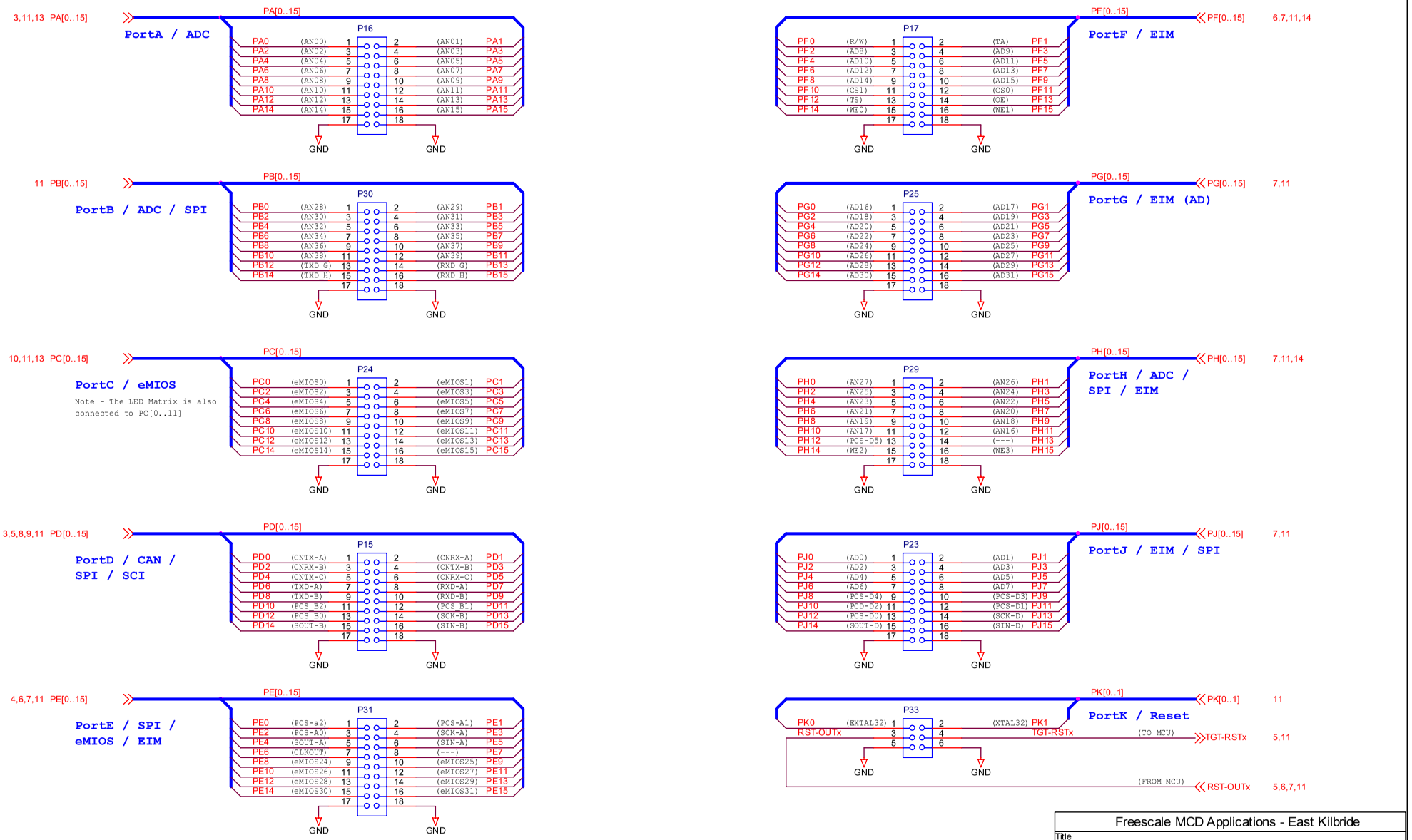
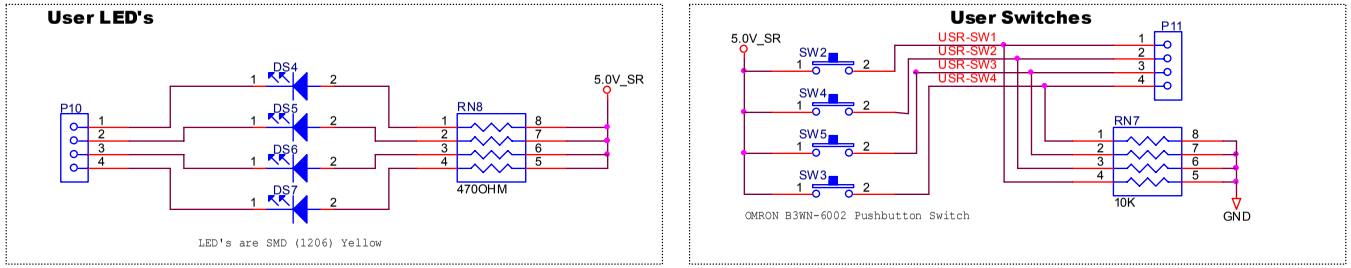
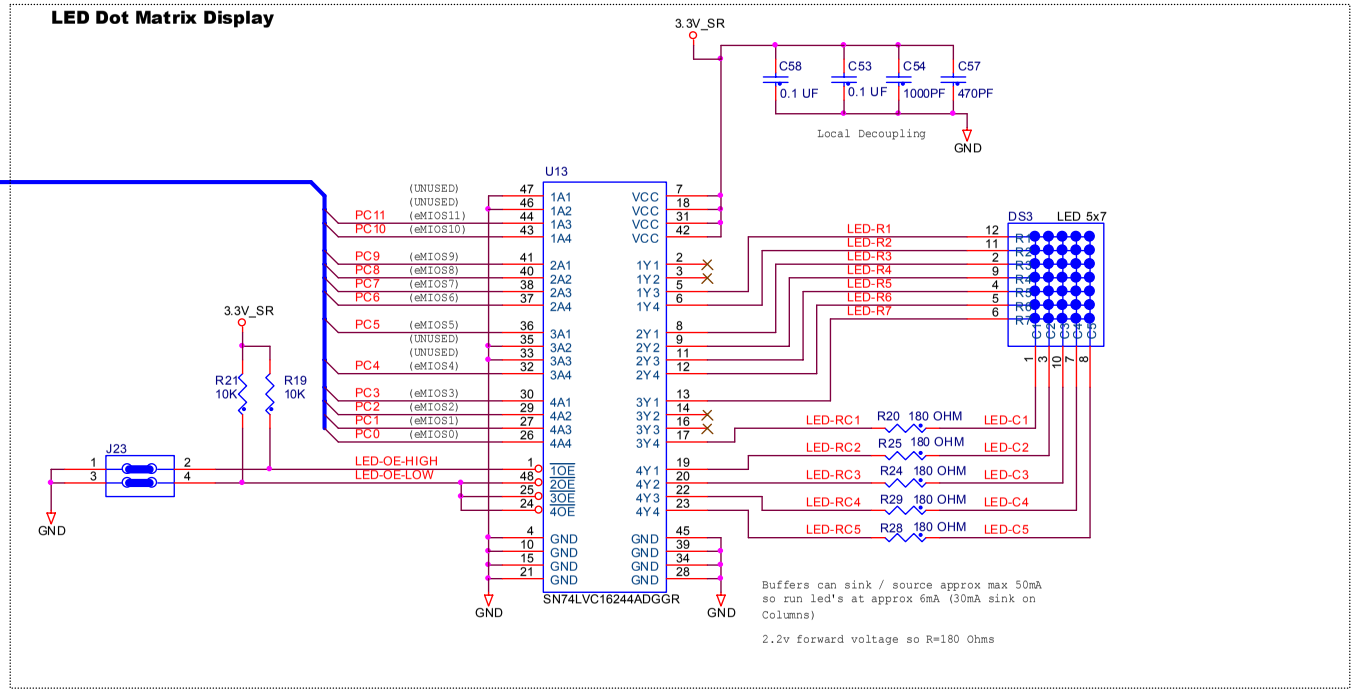
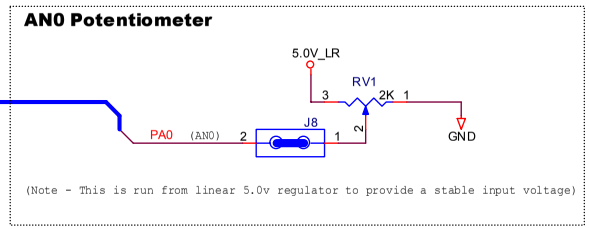
USER CONNECTORS



User Peripherals Inc Prototyping







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Size: B	Document Number: Drawing SCH-23130 (MPC5510EVB)	Rev: E0
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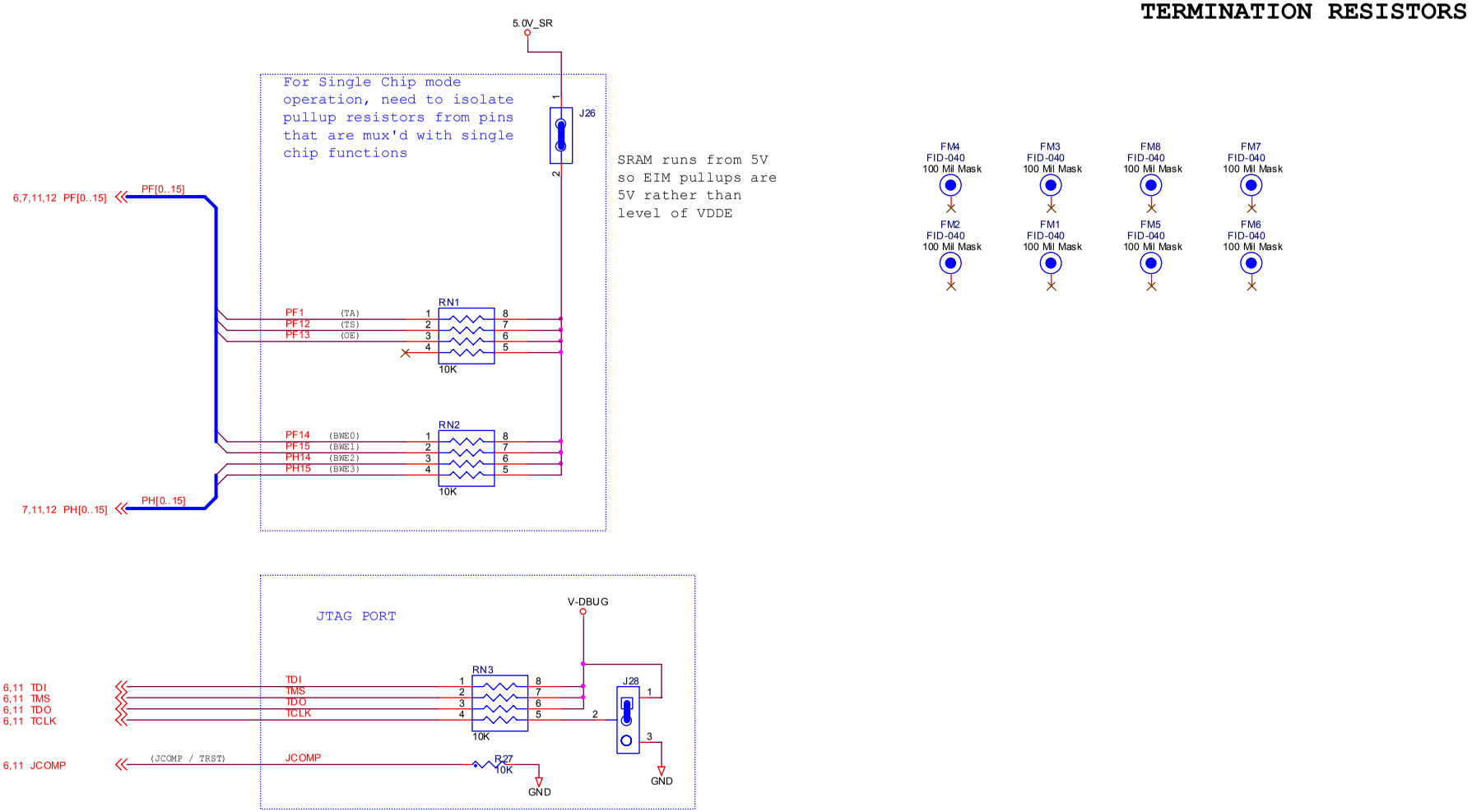
TERMINATION RESISTORS



All RESET Pullup Resistors are shown on Reset Circuitry page

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Appendix B - EVB Bill Of Materials

Qty	Refdes	Value	Manufacturer	Part Number
4	C1,C2,C3,C4	10UF	PANASONIC	EEE1CS100SR
12	C5,C28,C29,C30,C36,C48,C51,C54,C64,C65,C70,C84	1000PF	VENKEL COMPANY	C0805COG500-102JNE
6	C6,C49,C50,C57,C63,C69	470PF	KEMET	C0805C471J5GAC
35	C7,C27,C31,C32,C33,C34,C35,C38,C39,C44,C45,C46,C47,C52,C53,C55,C56,C58,C59,C60,C62,C67,C68,C72,C73,C74,C75,C76,C77,C78,C79,C80,C81,C82,C83	0.1 UF	KEMET	C0805C104K5RAC
2	C8,C19	4.7uF	MURATA	GRM32ER71H475K
3	C9,C10,C11	10UF	VISHAY INTERTECHNOLOGY	293D106X9010A2TE3
1	C12	68UF	AVX	TPSE686K025R0125
4	C13,C14,C15,C20	100uF	PANASONIC	EEEFC1V101AP
1	C16	1000UF	NICHICON	UVZ1H102MHD
2	C17,C18	3.3UF	MURATA	GRM32DR71H335KA88L
4	C21,C23,C24,C26	10 PF	KEMET	C0805C100J5GAC
2	C22,C25	4700PF	MURATA	GRM2165C1H472JA01D
5	C37,C40,C41,C42,C43	1.0UF	TAIYO YUDEN	TMK316BJ105ML
2	C61,C66	47PF	VENKEL COMPANY	C0805C0G500470JNE
1	C71	2200PF	SMEC	MCCE222J2NOTF
7	DS1,DS4,DS5,DS6,DS7,DS8,DS9	YELLOW LED	KINGBRIGHT	APT3216SYC
1	DS2	LED RED	KINGBRIGHT	APT3216SURCK
1	DS3	LED 5x7	KINGBRIGHT	TA07-11GWA
4	DS10,DS11,DS12,DS13	LED GREEN	KINGBRIGHT	K/APT-3216SGD
3	D1,D2,D4	GF1A	VISHAY INTERTECHNOLOGY	GF1A-E3
4	D3,D6,D7,D8	B130LB-13	DIODES INC	B130LB-13
3	FB1,FB2,FB3	BLM31AJ601SN1L	MURATA	BLM31AJ601SN1L
8	FM1,FM2,FM3,FM4,FM5,FM6,FM7,FM8	FID-040	GENERIC	FID-040
1	F1	Fuse Holder	BUSSMANN	MCHTC-15M

21	J1,J2,J5,J6,J7,J8,J9,J17,J21,J22,J24,J25,J26,J27,J32,J39,J41,J42,J44,J45,J46	HDR 1X2	SAMTEC	TMM-102-02-G-S
4	J3,J4,J20,J23	HDR 2X2	SAMTEC	TMM-102-02-G-D
6	J10,J11,J12,J14,J16,J35	HDR 2X3	SAMTEC	TMM-103-02-G-D
2	J13,J15	HDR_2X4	SAMTEC	TMM-104-02-G-D
14	J18,P19,J19,J28,J29,J30,J31B,J31,J33,J34,J36,J37,J38,J40	HDR 3X1	SAMTEC	TMM-103-02-G-S
1	J43	HDR2X6	SAMTEC	TMM-106-01-G-D
2	L1,L2	DLW43SH	MURATA	DLW43SH101XK2
2	L3,L6	47UF	COOPER ELECTRONICS TECHNOLOGIES	DR73-470-R
1	L4	68UH	COOPER ELECTRONICS TECHNOLOGIES	DR125-680-R
1	L5	100UH	COOPER ELECTRONICS TECHNOLOGIES	DR74-101-R
20	PT1,PT2,PT3,PT4,PT5,PT6,PT7,PT8,PT9,PT10,PT11,PT12,PT13,PT14,PT15,PT16,PT17,PT18,PT19,PT20	HDR_1X1	SAMTEC	HTSW-101-07-SM-S
2	P1,P2	HDR 1X2	MOLEX	53047-0210
2	P3,P4	HDR_1X3	SAMTEC	HTSW-103-07-SM-S
2	P5,P6	DB9	TYCO ELECTRONICS	5747844-6
5	P7,P8,P10,P11,P26	1X4HDR	SAMTEC	TSW-104-07-G-S
2	P9,P22	CON2X60	TYCO ELECTRONICS	5179031-5
1	P12	HDR_2X5	SAMTEC	TSW-105-08-G-D
1	P13	HDR 2X7	3M	N2514-6002RB
1	P14	HDR_2X19_F	TYCO ELECTRONICS	2-5767004-2
9	P15,P16,P17,P23,P24,P25,P29,P30,P31	HDR 2X9	SAMTEC	TSW-109-07-S-D
1	P18	HDR_1X5_M	TYCO ELECTRONICS	5-146276-5
2	P21,P27	1053378-1	TYCO ELECTRONICS	1053378-1
1	P28	POWER_JACK	SWITCHCRAFT	RAPC722X
1	P32	TB2	TYCO ELECTRONICS	1437671-1
1	P33	HDR_2X3	SAMTEC	TSW-103-07-S-D
2	Q1,Q2	BCP52-16	PHILIPS SEMICONDUCTOR	BCP52-16
1	Q3	BSH103	PHILIPS SEMICONDUCTOR	BSH103
8	RN1,RN2,RN3,RN4,RN5,RN6,RN7,RN9	10K	BOURNS	CAT16-1002F4LF

1	RN8	470OHM	CTS	742C083471JP
1	RV1	2K	BOURNS	3310Y-001-202L
4	R1,R2,R3,R4	47 OHM	YAGEO AMERICA	232273464709L
7	R5,R6,R14,R15,R50,R51,R53	0 OHM	BOURNS	CR0805-J/-000ELF
4	R7,R8,R37,R40	1.0K	KOA SPEER	RK73H2ATTD1001F
12	R9,R10,R13,R16,R19,R21,R27,R32,R33,R36,R49,R52	10K	VENKEL COMPANY	CR0805-8W-103JT
2	R11,R12	47K	BOURNS	CR0805-FX-4702ELF
4	R17,R18,R42,R47	560 OHM	YAGEO AMERICA	232273465601L
5	R20,R24,R25,R28,R29	180 OHM	YAGEO AMERICA	232273461801L
2	R22,R44	1.2K	KOA SPEER	RK73B2ATTD122J
1	R23	470 OHM	BOURNS	CR0805-FX-4700ELF
3	R30,R31,R48	270 OHM	SMEC	RC73L2D271JTF
2	R34,R35	60.4OHM	YAGEO AMERICA	232273466049L
2	R38,R45	100 OHM	VENKEL COMPANY	CR08058W1000FSNT
1	R41	68 OHM	YAGEO AMERICA	232273466809L
1	R43	220 OHM	YAGEO AMERICA	RC0805JR-07220RL
1	R46	1.80K	BOURNS	CR0805-FX-1801ELF
1	SW1	KS11R23CQD	ITT CANNON	KS11R23CQD
4	SW2,SW3,SW4,SW5	B3WN-6002	OMRON	B3WN-6002
1	SW6	G-107-0513	CW INDUSTRIES	G-107-0513
24	TPV1,TPV2,TPV3,TPV4,TPV5,TPV6,TPV7,TPV8,TPV9,TPV10,TPV11,TPV12,TPV13,TPV14,TPV15,TPV16,TPV17,TPV18,TPV19,TPV20,TPV21,TPV22,TPV23,TPV24	TEST POINT	NA	NA
15	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15	TEST POINT	NICOMATIC	C12000B
2	U1,U2	PCA82C250TD	PHILIPS SEMICONDUCTOR	PCA82C250TD
2	U3,U4	MCZ33399	FREESCALE SEMICONDUCTOR	MCZ33399EF
2	U5,U6	TJA1080TS/N	PHILIPS SEMICONDUCTOR	TJA1080TS/N
1	U7	MAX232ACSE+	MAXIM	MAX232ACSE+
1	U8	SN74LV125	TEXAS INSTRUMENTS	SN74LV125AD
1	U9	MC74ACT08DG	ON SEMICONDUCTOR	MC74ACT08DG
1	U10	74FCT162373ATPACT	TEXAS INSTRUMENTS	74FCT162373ATPACT

1	U11	MAX705CSA+	MAXIM	MAX705CSA+
3	U12,U14,U17	IS61C6416AL-12TLI	ISSI	IS61C6416AL-12TLI
1	U13	SN74LVC16244ADGGR	TEXAS INSTRUMENTS	SN74LVC16244ADGGR
1	U15	ispGAL22V10AV-23LNN	LATTICE SEMICONDUCTOR CORPORATION	ISPGAL22V10AV-23LNNC
1	U16	ispGAL22V10AV-28LJC	LATTICE SEMICONDUCTOR CORPORATION	ISPGAL22V10AV-28LJC
1	U18	MC33905S	FREESCALE SEMICONDUCTOR	MC33905S
1	U19	LM2937-5.0	NATIONAL SEMICONDUCTOR	LM2937IMP-5.0/NOPB
1	U20	LM2676S-ADJ	NATIONAL SEMICONDUCTOR	LM2676S-ADJ/NOPB
1	U21	LM2676S-3.3	NATIONAL SEMICONDUCTOR	LM2676S-3.3/NOPB
1	U22	LM2676S-5.0	NATIONAL SEMICONDUCTOR	LM2676S-5.0/NOPB
1	Y1	8MHz	ECS INC. INTERNATIONAL	ECS-3953C-080B

Appendix C - 144QFP Daughtercard Schematics

MPC5510 144QFP MCU Daughter Card

Table Of Contents:

MPC5510 144 PIN MCU (1of2) - I/O	SHEET 2
MPC5510 144 PIN MCU (2of2) - Power	SHEET 3
CLOCK AND PLL CIRCUITRY	SHEET 4
EXPANSION CONNECTORS (DAUGHTERCARD)	SHEET 5

Revision Information

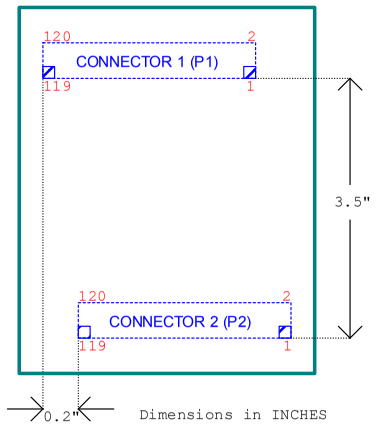
Rev	Date	Designer	Comments
0.1	04 Jan 07	M. Stewart	Provisional release
0.2	15 Jan 07	M. Stewart	Provisional release (post layout)
0.3	16 Jan 07	M. Stewart	Provisional release (post layout fix). PCB RevA
B0	29 Mar 07	M. Stewart	Production Release
B1	12 Sep 07	A. Robertson	Cosmetic changes optimised for A4 - PCB RevB

Notes:

- Resistor networks are donated RNx. All resistor networks are SMD 1206 style package.
- All decoupling caps less than 0.1uF are COG unless otherwise stated
- All decoupling caps greater than 0.1uF are X7R unless otherwise stated
- All connectors are denoted Px. All connectors and headers are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2
- All Switches are denoted SWx
- All test points are denoted TPx
- All unpopulated test points (vias) are denoted as TPVx

User notes are given throughtout the schematics.
Specific PCB LAYOUT notes are detailed in ITALICS

Connectors fitted to UNDERSIDE of PCB but viewed and numbered from TOP side in this diagram



ADAPTER BOARD LAYOUT INSTRUCTIONS

Important Note:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale MPC5510 family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

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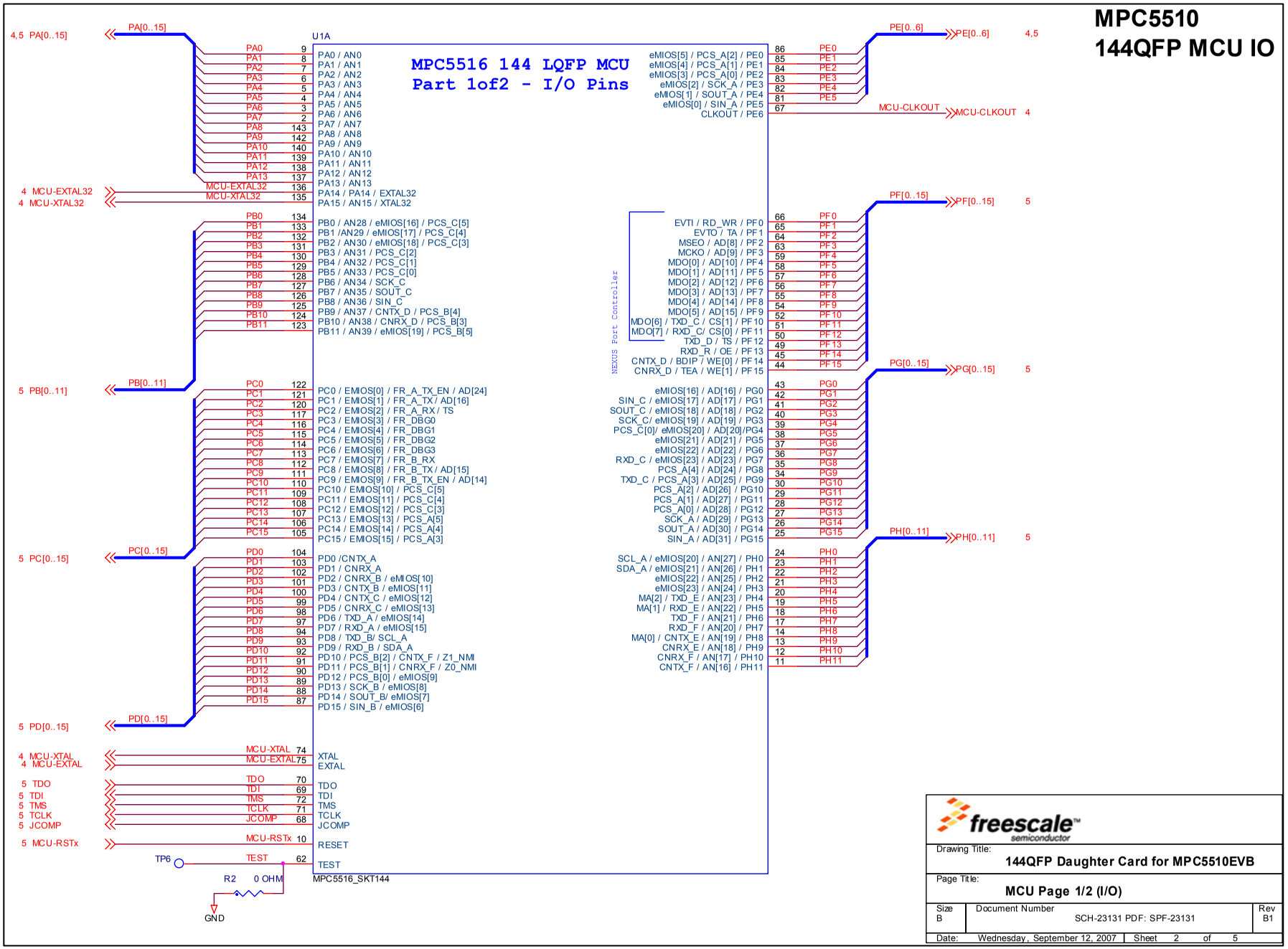
MCD Applications East Kilbride
Colvilles Road, Kelvin Industrial Estate, East Kilbride G75 0TG

Designer: M. Stewart	Drawing Title: 144QFP Daughter Card for MPC5510EVB		
Drawn by: M. Stewart	Page Title: Front Page Contents and Notes		
Approved: M. Stewart	Size B	Document Number SCH-23131 PDF: SPF-23131	Rev B1
	Date: Wednesday, September 12, 2007	Sheet 1 of 5	


MPC5510
144QFP MCU IO
MPC5516 144 LQFP MCU
Part 1of2 - I/O Pins
U1A
MPC5516_SKT144
NEXUS Port Controller
PA[0..15]
PB[0..11]
PC[0..15]
PD[0..15]
PE[0..6]
PF[0..15]
PG[0..15]
PH[0..11]
MCU-CLKOUT
MCU-EXTAL32
MCU-XTAL32
MCU-XTAL
MCU-EXTAL
TDO
TDI
TMS
TCLK
JCOMP
MCU-RSTx
TEST
TP6
R2
0 OHM
GND
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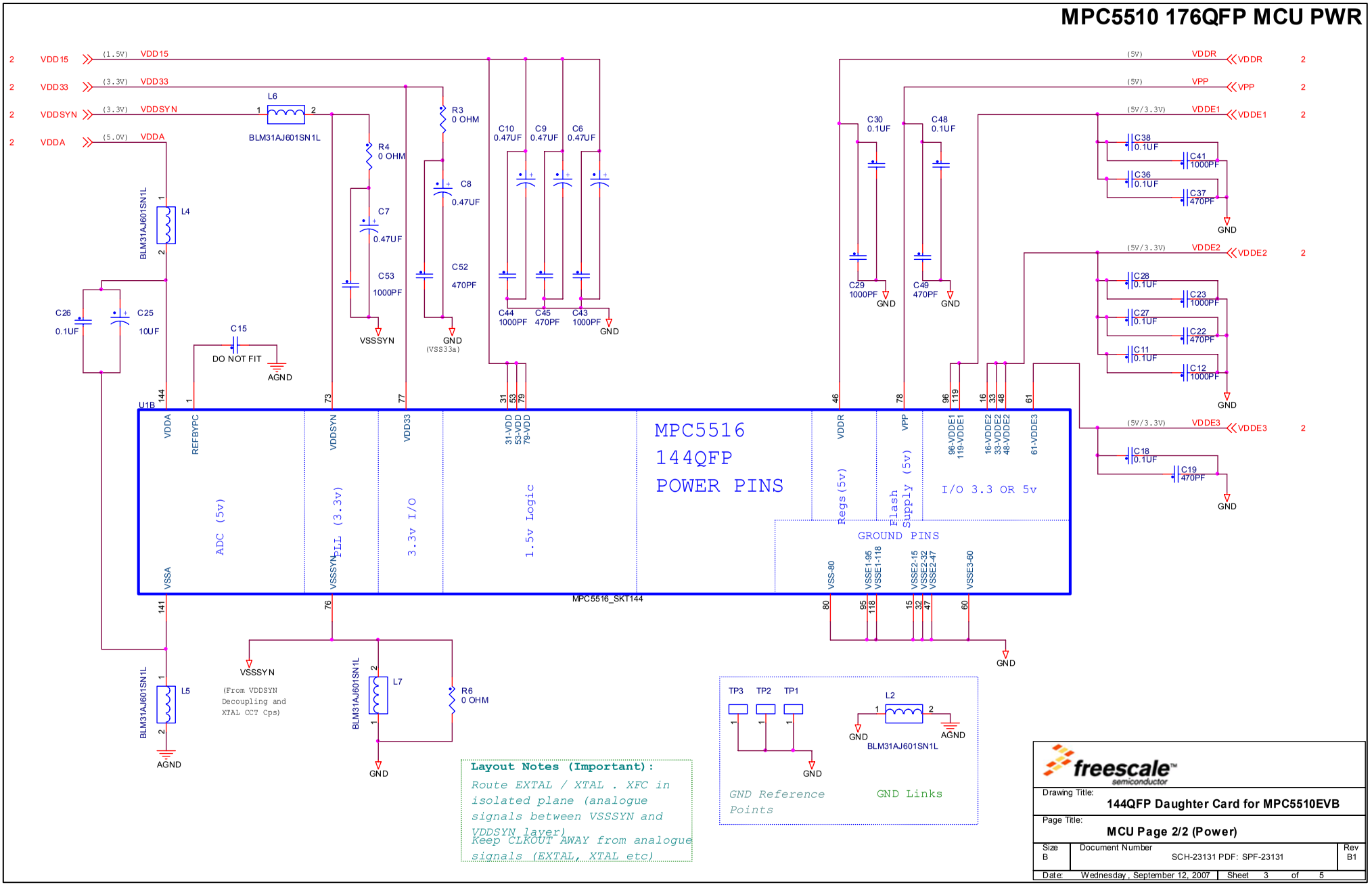
Drawing Title:
144QFP Daughter Card for MPC5510EVB
Page Title:
MCU Page 1/2 (I/O)
Size B
Document Number SCH-23131 PDF: SPF-23131
Rev B1
Date: Wednesday, September 12, 2007
Sheet 2 of 5


MPC5510 176QFP MCU PWR
VDD15
VDD33
VDDSYN
VDDA
L6
BLM31AJ601SN1L
R3 0 OHM
R4 0 OHM
C10 0.47UF
C9 0.47UF
C6 0.47UF
C8 0.47UF
C7 0.47UF
C53 1000PF
C52 470PF
C44 1000PF
C45 470PF
C43 1000PF
C26 0.1UF
C25 10UF
C15 DO NOT FIT
AGND
VSSSYN
GND
(VSS33a)
L4
U1B
MPC5516 144QFP POWER PINS
ADC (5v)
PLL (3.3v)
3.3v I/O
1.5v Logic
Regs(5v)
Flash Supply (5v)
I/O 3.3 OR 5v
GROUND PINS
MPC5516_SKT144
VDDR
VPP
VDDE1
VDDE2
VDDE3
C30 0.1UF
C48 0.1UF
C29 1000PF
C49 470PF
C38 0.1UF
C41 1000PF
C36 0.1UF
C37 470PF
C28 0.1UF
C23 1000PF
C27 0.1UF
C22 470PF
C11 0.1UF
C12 1000PF
C18 0.1UF
C19 470PF
L5
L7
R6 0 OHM
(From VDDSYN Decoupling and XTAL CCT Cps)
TP3
TP2
TP1
L2
GND Reference Points
GND Links
Layout Notes (Important):
Route EXTAL / XTAL . XFC in isolated plane (analogue signals between VSSSYN and VDDSYN layer)
Keep CLKOUT AWAY from analogue signals (EXTAL, XTAL etc)
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Drawing Title: 144QFP Daughter Card for MPC5510EVB
Page Title: MCU Page 2/2 (Power)
Size B
Document Number SCH-23131 PDF: SPF-23131
Rev B1
Date: Wednesday, September 12, 2007
Sheet 3 of 5

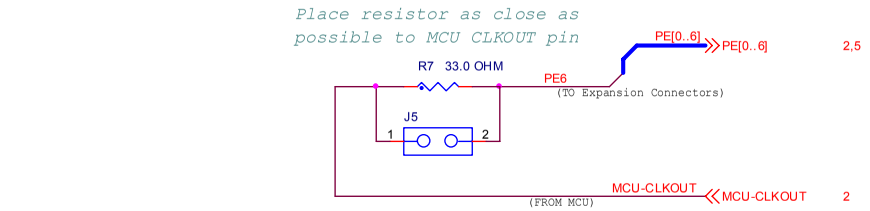
CLOCK CIRCUITRY

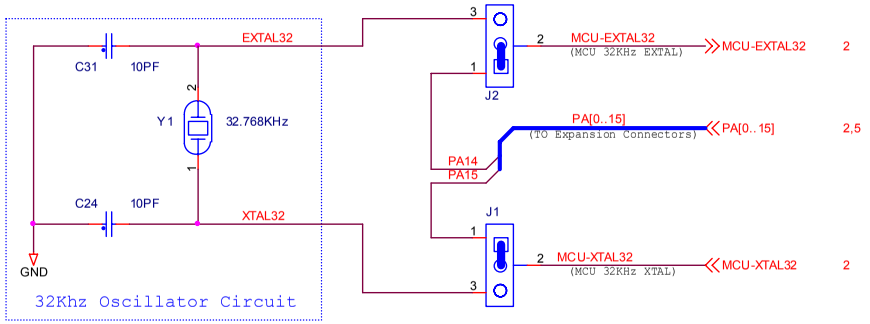
FID1 FID2 FID3 FID4

FID5 FID6 FID7 FID8

Layout Notes (Important):

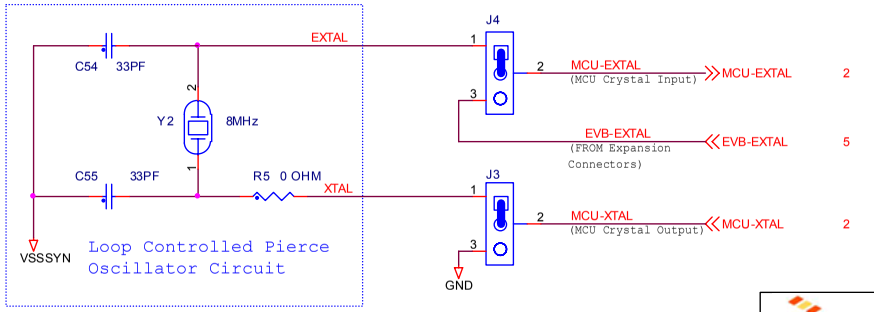
Route EXTAL / XTAL in isolated plane (analogue signals between VSSSYN and VDDSYN layer)
Keep MCU-CLKOUT AWAY from analoguesignals (EXTAL, XTAL etc)





REMOVE XTAL jumper when driving EXTAL from Oscilaltor Module or External Source (PLL Enabled)

Connect XTAL jumper to GND when driving EXTAL from Oscilaltor Module or External Source (PLL Bypass Mode)



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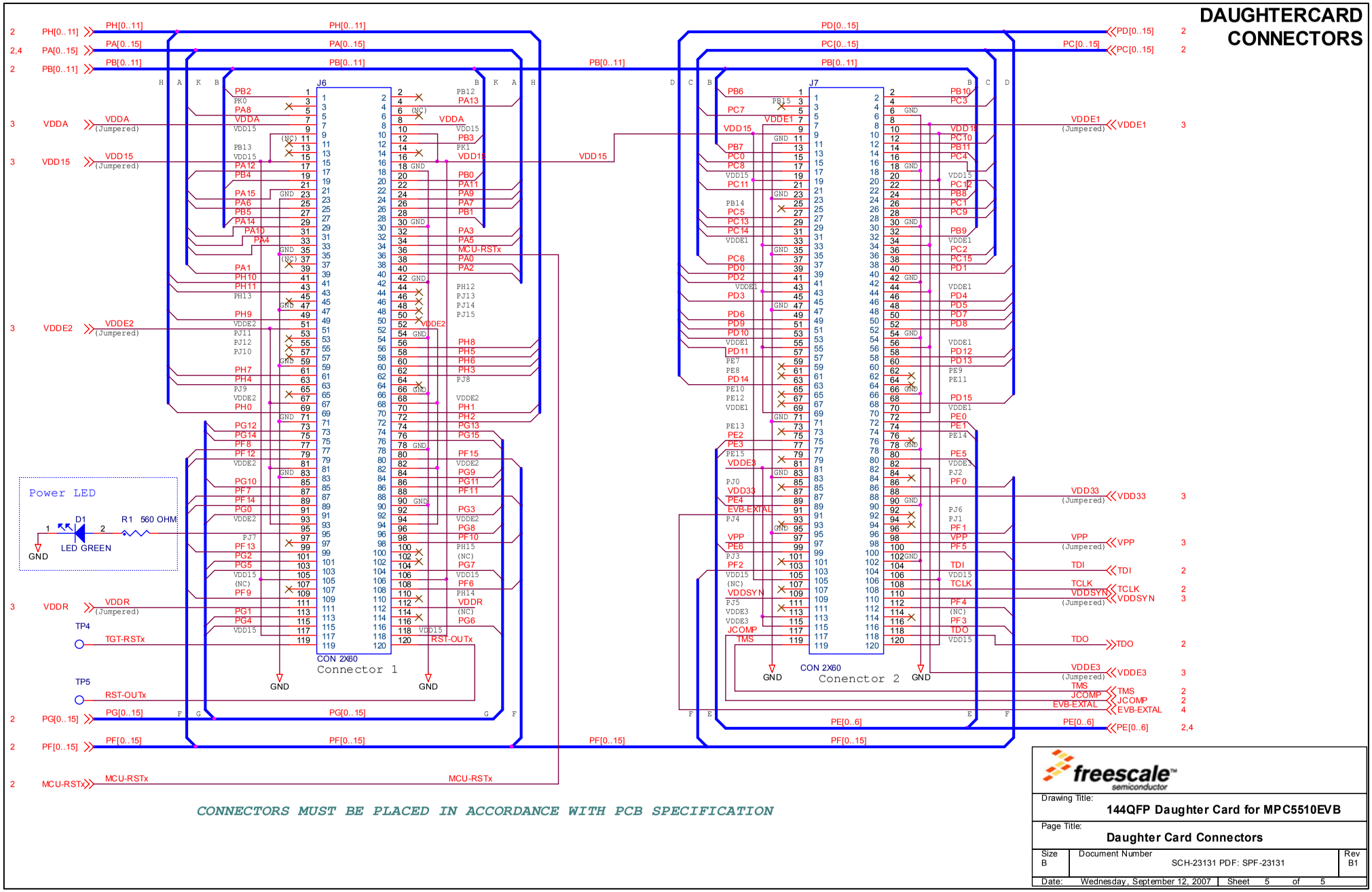
Drawing Title:	144QFP Daughter Card for MPC5510EVB
Page Title:	Clock Circuitry
Size B / Document Number	SCH-23131 PDF: SPF-23131 / Rev B1
Date: Wednesday, September 12, 2007	Sheet 4 of 5


DAUGHTERCARD CONNECTORS
J6
CON 2X60
Connector 1
J7
CON 2X60
Conenctor 2
Power LED
D1
LED GREEN
R1 560 OHM
TP4
TGT-RSTx
TP5
RST-OUTx
VDDA (Jumpered)
VDD15 (Jumpered)
VDDE2 (Jumpered)
VDDR (Jumpered)
VDDE1 (Jumpered)
VDD33 (Jumpered)
VPP (Jumpered)
VDDSYN (Jumpered)
VDDE3 (Jumpered)
MCU-RSTx
PH[0..11]
PA[0..15]
PB[0..11]
PC[0..15]
PD[0..15]
PE[0..6]
PF[0..15]
PG[0..15]
GND
TDI
TCLK
TDO
TMS
JCOMP
EVB-EXTAL
CONNECTORS MUST BE PLACED IN ACCORDANCE WITH PCB SPECIFICATION
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Drawing Title: 144QFP Daughter Card for MPC5510EVB
Page Title: Daughter Card Connectors
Size B
Document Number SCH-23131 PDF: SPF-23131
Rev B1
Date: Wednesday, September 12, 2007
Sheet 5 of 5

Appendix D - 144QFP Daughtercard Bill Of Materials

Qty	Refdes	Value	Manufacturer	Part Number
5	C6,C7,C8,C9,C10	0.47UF	AVX	TAJA474M025R
10	C11,C15,C18,C26,C27,C28,C30,C36,C38,C48	0.1UF	MURATA	GRM188R71H104KA93D
7	C12,C23,C29,C41,C43,C44,C53	1000PF	VENKEL COMPANY	C0805COG500-102JNE
6	C19,C22,C37,C45,C49,C52	470PF	PANASONIC	ECJ1VC1H471J
2	C24,C31	10PF	KEMET	C0603C100F5GAC
1	C25	10UF	VISHAY INTERTECHNOLOGY	293D106X9010A2TE3
2	C54,C55	33PF	VENKEL COMPANY	C0603C0G500-330JNE
1	D1	LED GREEN	KINGBRIGHT	K/APT-3216SGD
8	FID1,FID2,FID3,FID4,FID5,FID6,FID7,FID8	FID-040	GENERIC	FID-040
4	J1,J2,J3,J4	HDR 3X1	SAMTEC	TMM-103-02-G-S
1	J5	HDR 1X2	SAMTEC	TMM-102-02-G-S
2	J6,J7	CON 2X60	TYCO ELECTRONICS	5-5179009-5
5	L2,L4,L5,L6,L7	BLM31AJ601SN1L	MURATA	BLM31AJ601SN1L
1	R1	560 OHM	KOA SPEER	RK73H1JTTD5600F
5	R2,R3,R4,R5,R6	0 OHM	THYE MING TECH CO LTD	CR-03JL7-0R

Appendix E - 176QFP Daughtercard Schematics

MPC5510 176QFP MCU Daughter Card

Table Of Contents:

MPC5510 176 PIN MCU (1of2) - I/O	SHEET 2
MPC5510 176 PIN MCU (2of2) - Power	SHEET 3
CLOCK AND PLL CIRCUITRY	SHEET 4
EXPANSION CONNECTORS (DAUGHTERCARD)	SHEET 5

Revision Information

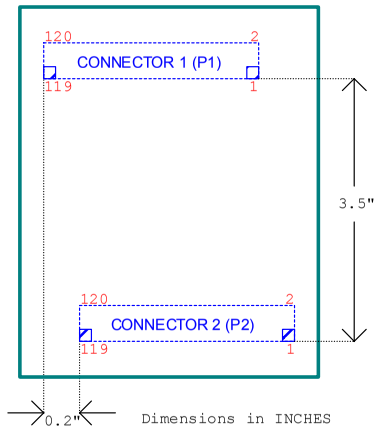
Rev	Date	Designer	Comments
0.1	13 Jun 07	A. Robertson	Prototype release - PCB RevA
B0	08 Aug 07	A. Robertson	Correction to VDDE1 short
B1	15 Aug 07	A. Robertson	Production Release - PCB RevB (Not manufactured)
B2	20 Aug 07	A. Robertson	Correction to Clock Selection Jumpers
C0	12 Sept 07	A. Robertson	Production Release - PCB RevC

Notes:

- Resistor networks are donated RNx. All resistor networks are SMD 1206 style package.
- All decoupling caps less than 0.1uF are COG unless otherwise stated
- All decoupling caps greater than 0.1uF are X7R unless otherwise stated
- All connectors are denoted Px. All connectors and headers are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2
- All Switches are denoted SWx
- All test points are denoted TPx
- All unpopulated test points (vias) are denoted as TPVx

User notes are given throughtout the schematics.
Specific PCB LAYOUT notes are detailed in ITALICS

Connectors fitted to UNDERSIDE of PCB but viewed and numbered from TOP side in this diagram



ADAPTER BOARD LAYOUT INSTRUCTIONS

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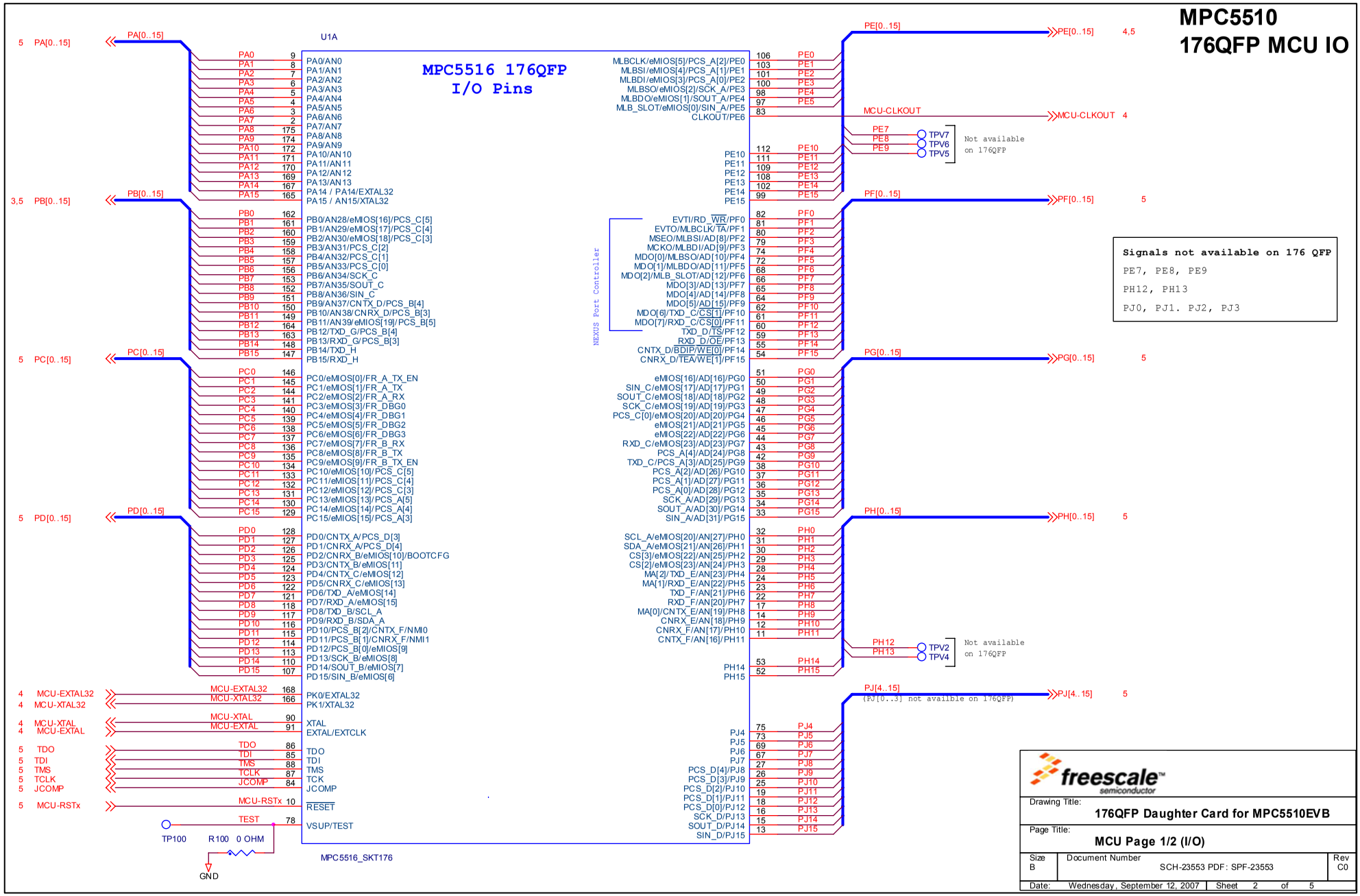
MCD Applications East Kilbride
Colvilles Road, Kelvin Industrial Estate, East Kilbride G75 0TG

Designer: A. Robertson	Drawing Title: 176QFP Daughter Card for MPC5510EVB	
Drawn by: A. Robertson	Page Title: Front Page Contents and Notes	
Approved: A. Robertson	Size B	Document Number SCH-23553 PDF: SPF-23553 Rev C0
	Date: Wednesday, September 12, 2007	Sheet 1 of 5


MPC5510
176QFP MCU IO
MPC5516 176QFP
I/O Pins
U1A
MPC5516_SKT176
NEXUS Port Controller
PA[0..15]
PB[0..15]
PC[0..15]
PD[0..15]
PE[0..15]
PF[0..15]
PG[0..15]
PH[0..15]
PJ[4..15]
(PJ[0..3] not availble on 176QFP)
MCU-CLKOUT
MCU-EXTAL32
MCU-XTAL32
MCU-XTAL
MCU-EXTAL
TDO
TDI
TMS
TCLK
JCOMP
MCU-RSTx
TEST
TP100
R100 0 OHM
GND
TPV7
TPV6
TPV5
TPV2
TPV4
Not available
on 176QFP
Signals not available on 176 QFP
PE7, PE8, PE9
PH12, PH13
PJ0, PJ1. PJ2, PJ3
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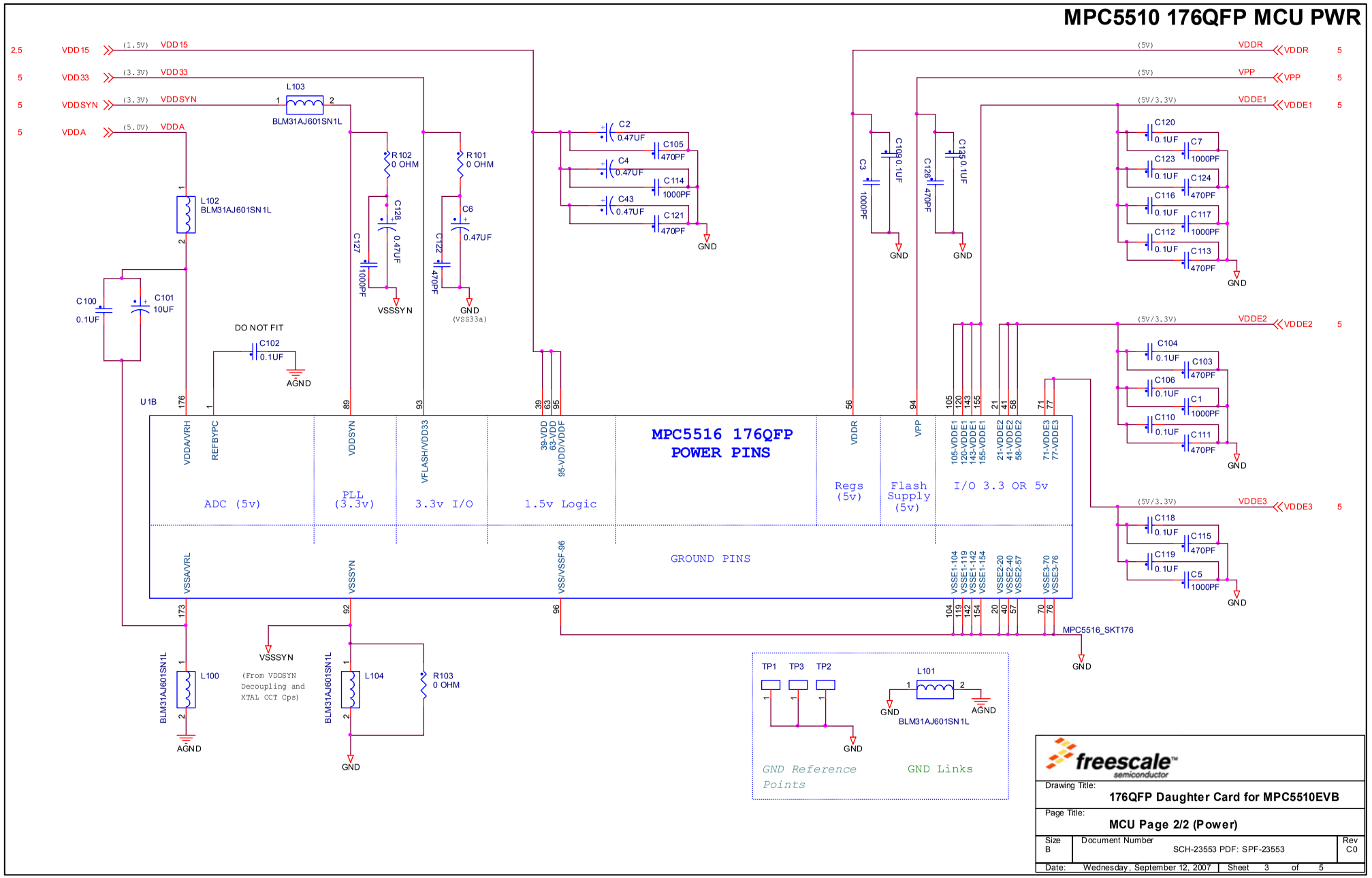
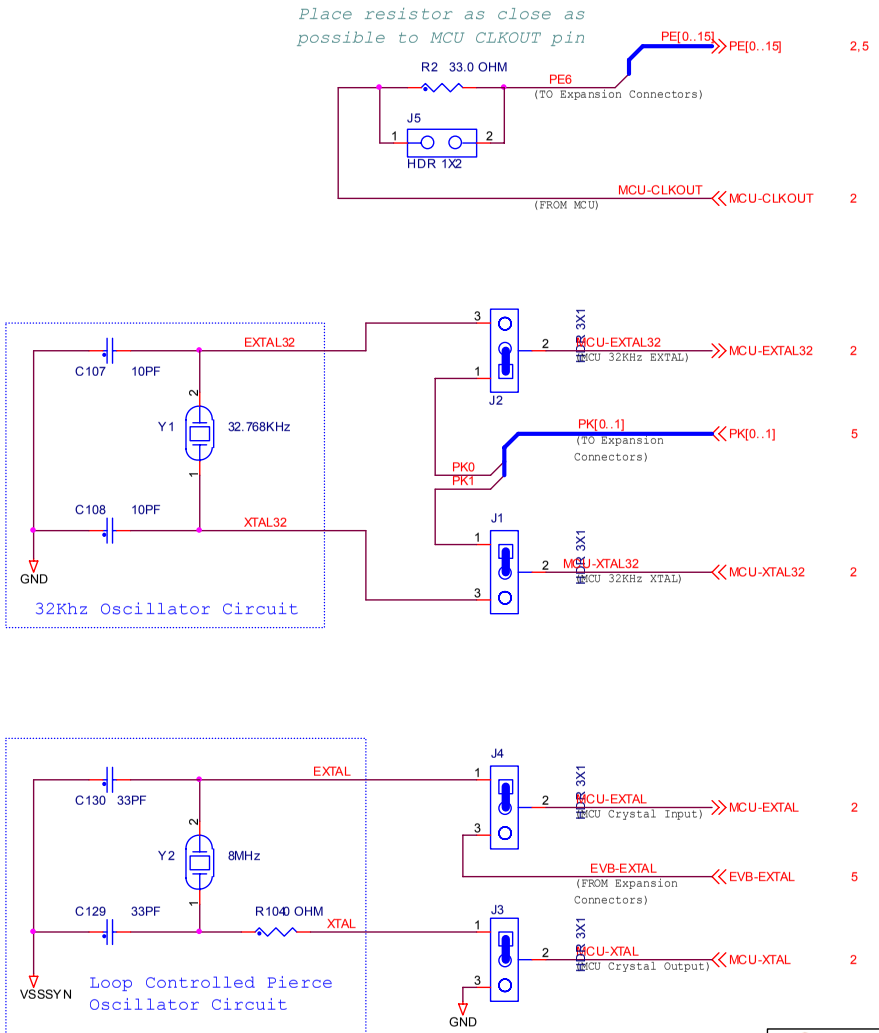
Drawing Title:
176QFP Daughter Card for MPC5510EVB
Page Title:
MCU Page 1/2 (I/O)
Size B
Document Number
SCH-23553 PDF: SPF-23553
Rev C0
Date: Wednesday, September 12, 2007
Sheet 2 of 5


MPC5510 176QFP MCU PWR
MPC5516 176QFP
POWER PINS
ADC (5v)
PLL (3.3v)
3.3v I/O
1.5v Logic
Regs (5v)
Flash Supply (5v)
I/O 3.3 OR 5v
GROUND PINS
VDD15
VDD33
VDDSYN
VDDA
VDDR
VPP
VDDE1
VDDE2
VDDE3
VSSSYN
AGND
GND
DO NOT FIT
GND Reference Points
GND Links
MPC5516_SKT176
freescale semiconductor
Drawing Title: 176QFP Daughter Card for MPC5510EVB
Page Title: MCU Page 2/2 (Power)
Size B
Document Number SCH-23553 PDF: SPF-23553
Rev C0
Date: Wednesday, September 12, 2007
Sheet 3 of 5

CLOCK CIRCUITRY



Layout Notes (Important):

Route EXTAL / XTAL in isolated plane (analogue signals between VSSSYN and VDDSYN layer)
Keep MCU-CLKOUT AWAY from analoguesignals (EXTAL, XTAL etc)

REMOVE XTAL jumper when driving EXTAL from Oscilaltor Module or External Source (PLL Enabled)
Connect XTAL jumper to GND when driving EXTAL from Oscilaltor Module or External Source (PLL Bypass Mode)

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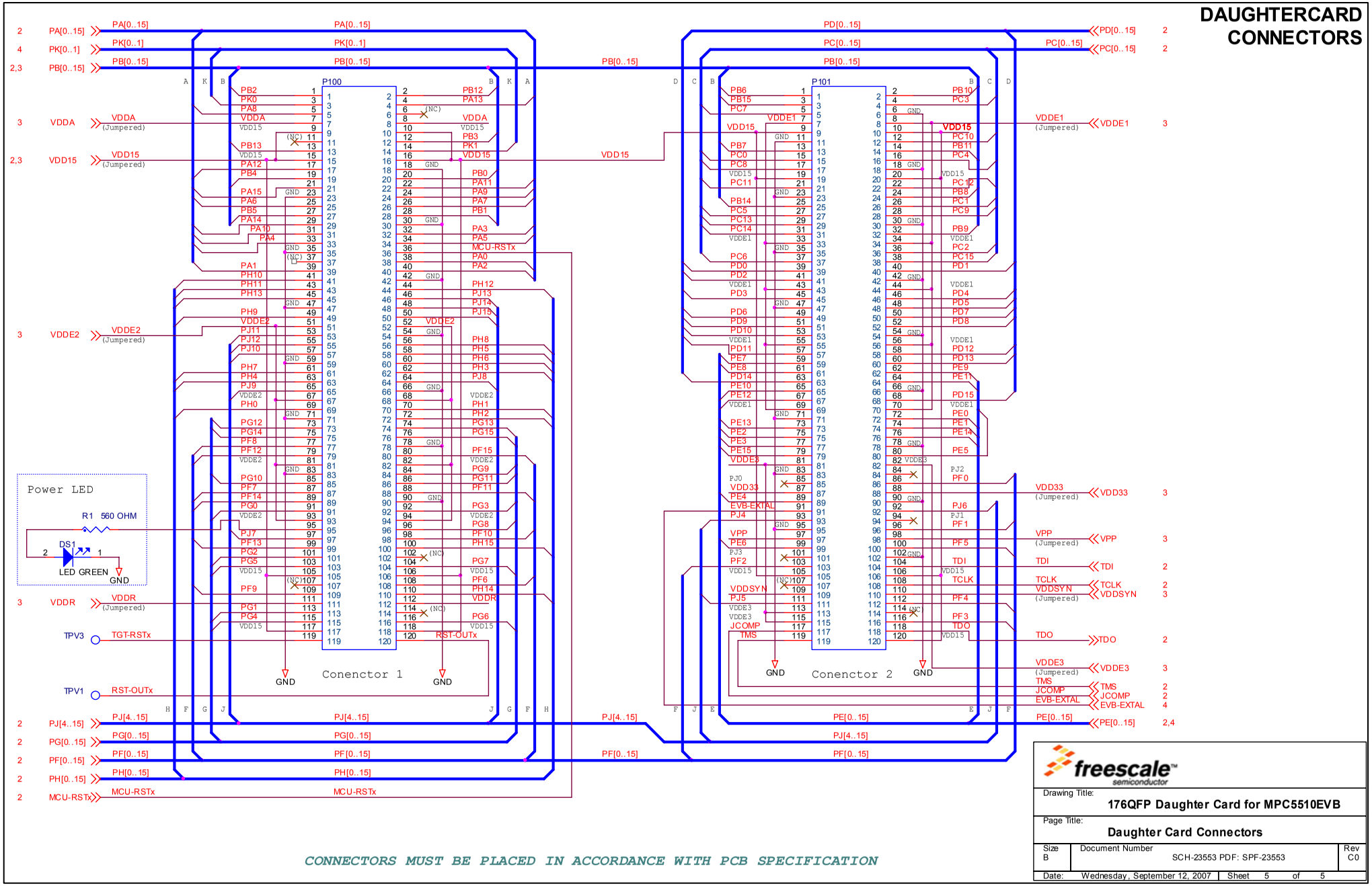
Drawing Title:	176QFP Daughter Card for MPC5510EVB
Page Title:	Clock Circuitry
Size: B	Document Number: SCH-23553 PDF: SPF-23553 — Rev: C0
Date: Wednesday, September 12, 2007	Sheet 4 of 5


DAUGHTERCARD CONNECTORS
P100
Conenctor 1
P101
Conenctor 2
Power LED
R1 560 OHM
DS1
LED GREEN
GND
VDDA (Jumpered)
VDD15 (Jumpered)
VDDE2 (Jumpered)
VDDR (Jumpered)
VDDE1 (Jumpered)
VDD33 (Jumpered)
VPP (Jumpered)
VDDSYN (Jumpered)
VDDE3 (Jumpered)
TPV3
TGT-RSTx
TPV1
RST-OUTx
MCU-RSTx
TCLK
TDI
TDO
TMS
JCOMP
EVB-EXTAL
CONNECTORS MUST BE PLACED IN ACCORDANCE WITH PCB SPECIFICATION
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Drawing Title: 176QFP Daughter Card for MPC5510EVB
Page Title: Daughter Card Connectors
Size B
Document Number SCH-23553 PDF: SPF-23553
Rev C0
Date: Wednesday, September 12, 2007
Sheet 5 of 5

Appendix F - 176QFP Daughtercard Bill Of Materials

Qty	Refdes	Value	Manufacturer	Part Number
7	C1,C3,C5,C7,C114,C117,C127	1000PF	VENKEL COMPANY	C0805COG500-102JNE
5	C2,C4,C6,C43,C128	0.47UF	AVX	TAJA474M025R
13	C100,C102,C104,C106,C109,C110,C112,C116,C118,C119,C120,C123,C125	0.1UF	MURATA	GRM188R71H104KA93D
1	C101	10UF	VISHAY INTERTECHNOLOGY	293D106X9010A2TE3
9	C103,C105,C111,C113,C115,C121,C122,C124,C126	470PF	PANASONIC	ECJ1VC1H471J
2	C107,C108	10PF	KEMET	C0603C100F5GAC
2	C129,C130	33PF	VENKEL COMPANY	C0603C0G500-330JNE
1	DS1	LED GREEN	KINGBRIGHT	K/APT-3216SGD
4	J1,J2,J3,J4	HDR 3X1	SAMTEC	TMM-103-02-G-S
1	J5	HDR 1X2	SAMTEC	TMM-102-02-G-S
5	L100,L101,L102,L103,L104	BLM31AJ601SN1L	MURATA	BLM31AJ601SN1L
2	P100,P101	CON 2X60	TYCO ELECTRONICS	5-5179009-5
1	R1	560 OHM	KOA SPEER	RK73H1JTTD5600F
1	R2	33.0 OHM	KOA SPEER	RK73H1JTTD33R0F
5	R100,R101,R102,R103,R104	0 OHM	THYE MING TECH CO LTD	CR-03JL7-0R
8	TPV1,TPV2,TPV3,TPV4,TPV5,TPV6,TPV7,TP100	TEST POINT	NA	NA
3	TP1,TP2,TP3	TP_2MMX1.3MM	N/A	N/A
1	U1	MPC5516_SKT176	Subassembly	210-77332, 344-00384
1	Y1	32.768KHz	VISHAY INTERTECHNOLOGY	XT26TTA32K768
1	Y2	8MHz	C-MAC MICROTECHNOLOGY	LF A140K

Appendix G - 208BGA Daughtercard Schematics

MPC5510 208BGA MCU Daughter Card

Table Of Contents:

MPC5510 208 PIN MCU (1of2) - I/O	SHEET 2
MPC5510 208 PIN MCU (2of2) - Power	SHEET 3
CLOCK AND PLL CIRCUITRY	SHEET 4
EXPANSION CONNECTORS (DAUGHTERCARD)	SHEET 5

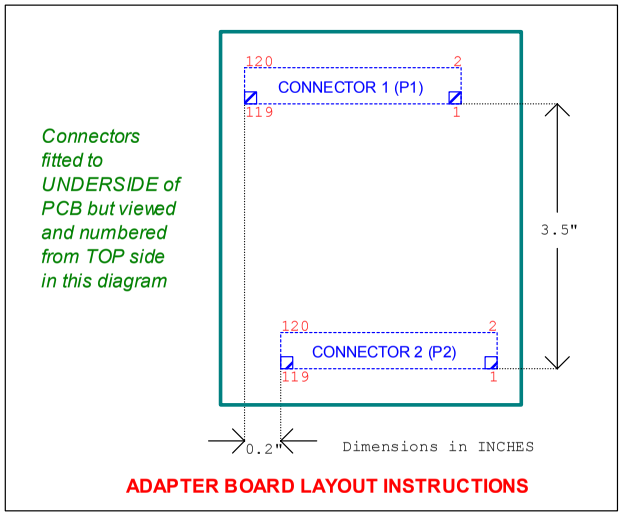
Revision Information

Rev	Date	Designer	Comments
0.1	03 Jan 07	M. Stewart	Provisional release
0.2	09 Jan 07	M. Stewart	Provisional release (Post Layout)
0.3	29 Jan 07	M. Stewart	Prototype Release - PCB RevA
B0	12 Sept 07	A. Robertson	Cosmetic changes optimised for A4 - PCB RevB

Notes:

- Resistor networks are donated RNx. All resistor networks are SMD 1206 style package.
- All decoupling caps less than 0.1uF are COG unless otherwise stated
- All decoupling caps greater than 0.1uF are X7R unless otherwise stated
- All connectors are denoted Px. All connectors and headers are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2
- All Switches are denoted SWx
- All test points are denoted TPx
- All unpopulated test points (vias) are denoted as TPVx

User notes are given throughtout the schematics.
Specific PCB LAYOUT notes are detailed in ITALICS



ADAPTER BOARD LAYOUT INSTRUCTIONS

Important Note:

These schematics are provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale MPC5510 family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

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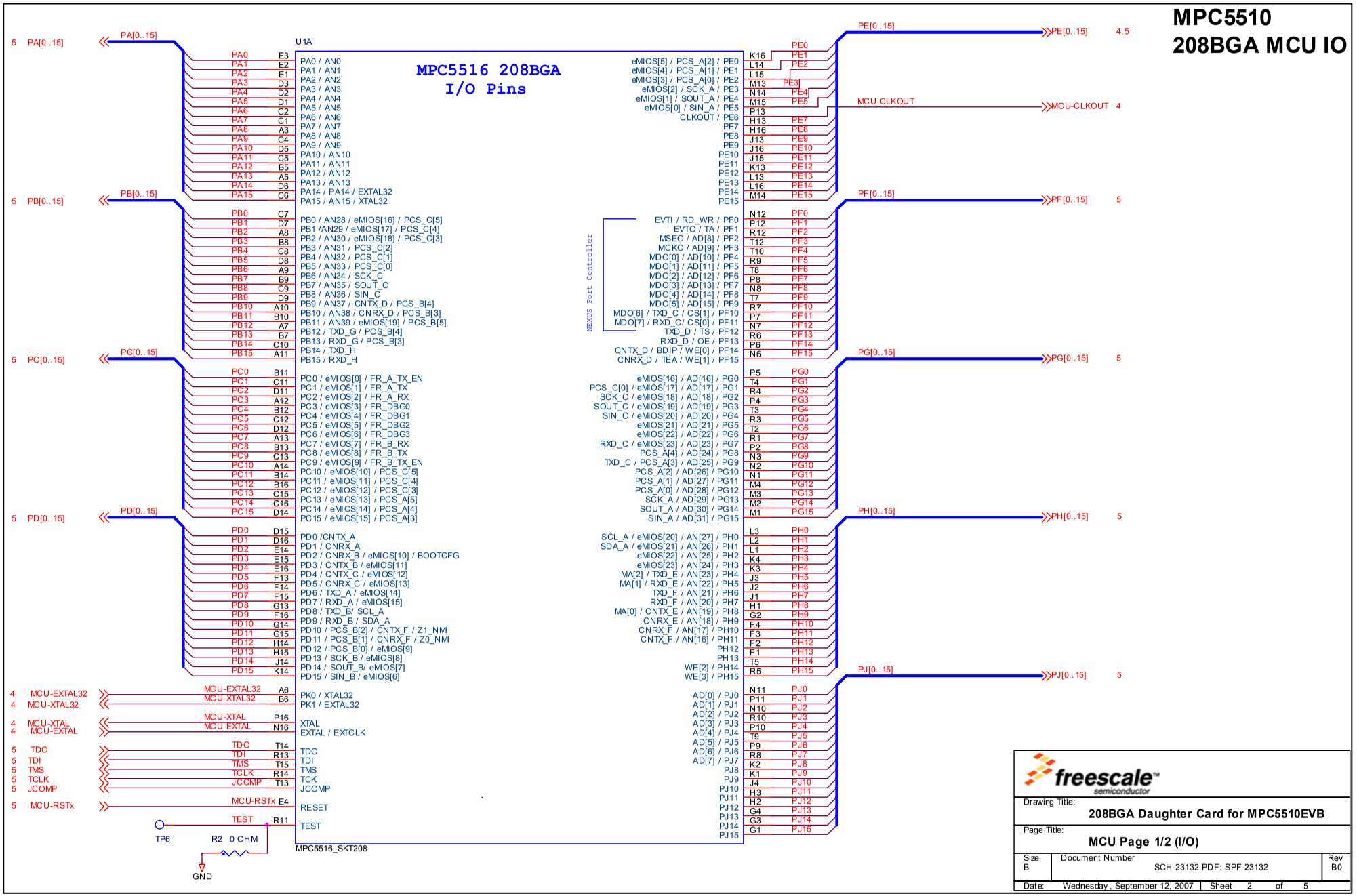
Transportation & Standard Products Group
MCD Applications East Kilbride
Colvilles Road, Kelvin Industrial Estate, East Kilbride G75 0TG

Designer: M. Stewart	Drawing Title: 208BGA Daughter Card for MPC5510EVB		
Drawn by : M. Stewart	Page Title: Front Page Contents and Notes		
Approved: M.Stewart	Size B	Document Number SCH-23132 PDF: SPF-23132	Rev B0
	Date: Wednesday, September 12, 2007	Sheet 1 of 5	


MPC5510
208BGA MCU IO
MPC5516 208BGA
I/O Pins
U1A
MPC5516_SKT208
NEXUS Port Controller
PA[0..15]
PB[0..15]
PC[0..15]
PD[0..15]
PE[0..15]
PF[0..15]
PG[0..15]
PH[0..15]
PJ[0..15]
MCU-CLKOUT
MCU-EXTAL32
MCU-XTAL32
MCU-XTAL
MCU-EXTAL
TDO
TDI
TMS
TCLK
JCOMP
MCU-RSTx
TEST
TP6
R2 0 OHM
GND
freescale semiconductor
Drawing Title:
208BGA Daughter Card for MPC5510EVB
Page Title:
MCU Page 1/2 (I/O)
Size B
Document Number
SCH-23132 PDF: SPF-23132
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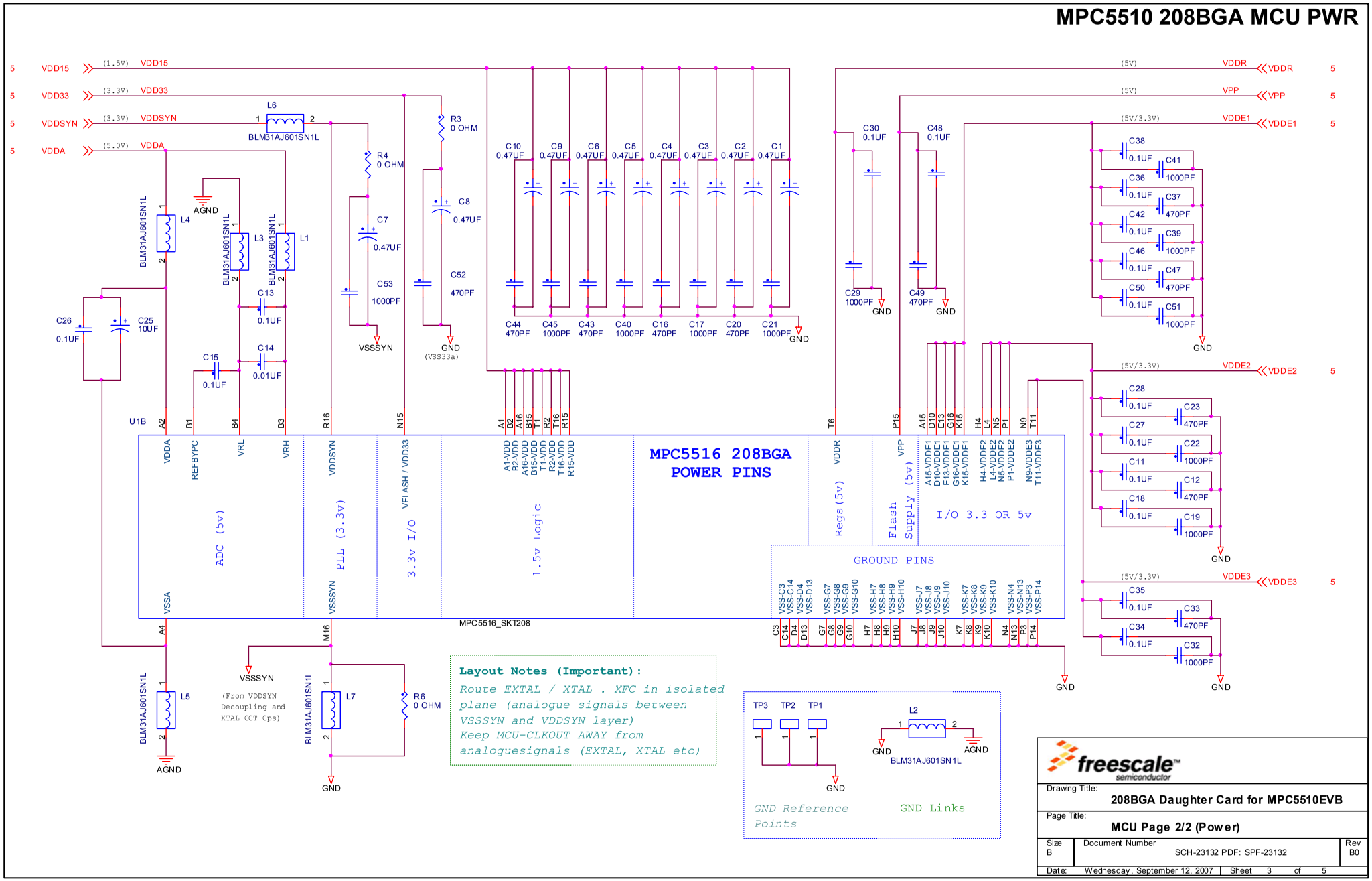
Date: Wednesday, September 12, 2007
Sheet 2 of 5


MPC5510 208BGA MCU PWR
MPC5516 208BGA
POWER PINS
ADC (5v)
PLL (3.3v)
3.3v I/O
1.5v Logic
Regs(5v)
Flash Supply (5v)
I/O 3.3 OR 5v
GROUND PINS
MPC5516_SKT208
Layout Notes (Important):
Route EXTAL / XTAL . XFC in isolated plane (analogue signals between VSSSYN and VDDSYN layer)
Keep MCU-CLKOUT AWAY from analoguesignals (EXTAL, XTAL etc)
GND Reference Points
GND Links
freescale semiconductor
Drawing Title:
208BGA Daughter Card for MPC5510EVB
Page Title:
MCU Page 2/2 (Power)
Size B
Document Number SCH-23132 PDF: SPF-23132
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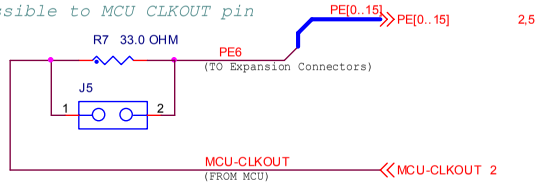
CLOCK CIRCUITRY

FID1 FID2 FID3 FID4

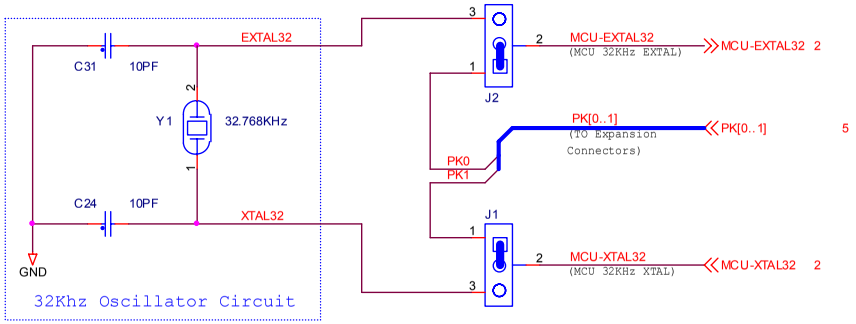
FID5 FID6 FID7 FID8

Place resistor as close as possible to MCU CLKOUT pin

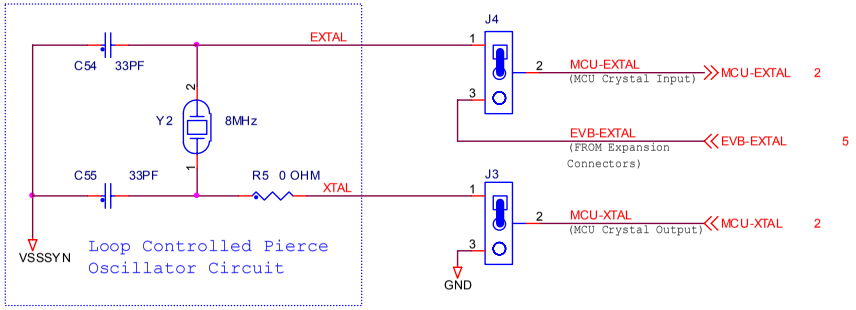


Layout Notes (Important):

Route EXTAL / XTAL in isolated plane (analogue signals between VSSSYN and VDDSYN layer)
Keep MCU-CLKOUT AWAY from analoguesignals (EXTAL, XTAL etc)



REMOVE XTAL jumper when driving EXTAL from Oscilaltor Module or External Source (PLL Enabled)
Connect XTAL jumper to GND when driving EXTAL from Oscilaltor Module or External Source (PLL Bypass Mode)



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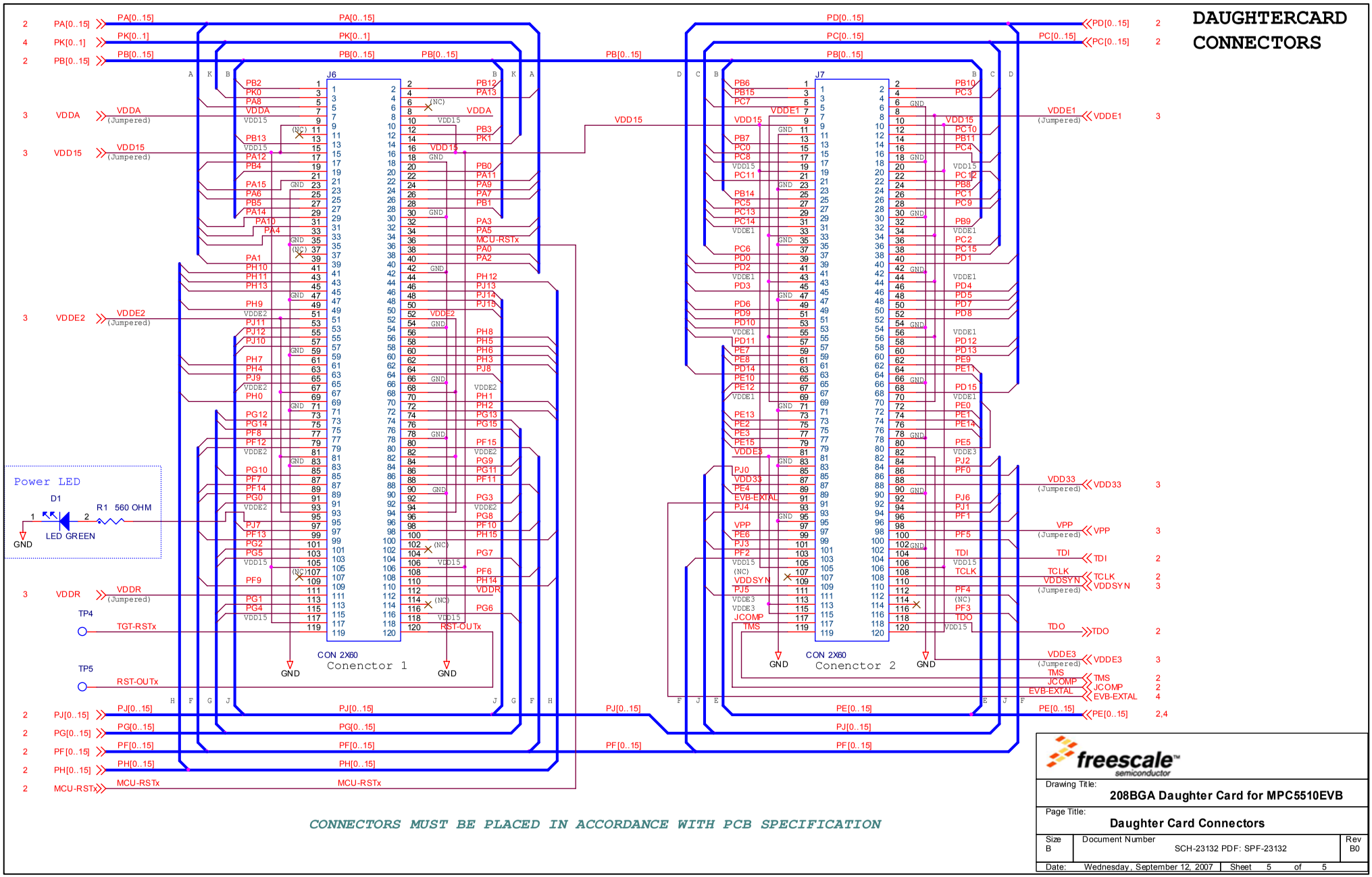
Drawing Title:	208BGA Daughter Card for MPC5510EVB
Page Title:	Clock Circuitry
Size: B	Document Number: SCH-23132 PDF: SPF-23132 Rev: B0
Date: Wednesday, September 12, 2007	Sheet 4 of 5


DAUGHTERCARD CONNECTORS
J6
J7
CON 2X60
Conenctor 1
Conenctor 2
Power LED
D1
LED GREEN
R1 560 OHM
TP4
TP5
TGT-RSTx
RST-OUTx
VDDA (Jumpered)
VDD15 (Jumpered)
VDDE2 (Jumpered)
VDDR (Jumpered)
VDDE1 (Jumpered)
VDD33 (Jumpered)
VPP (Jumpered)
VDDSYN (Jumpered)
VDDE3 (Jumpered)
CONNECTORS MUST BE PLACED IN ACCORDANCE WITH PCB SPECIFICATION
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Drawing Title: 208BGA Daughter Card for MPC5510EVB
Page Title: Daughter Card Connectors
Size B
Document Number SCH-23132 PDF: SPF-23132
Rev B0
Date: Wednesday, September 12, 2007
Sheet 5 of 5

Appendix H - 208BGA Daughtercard Bill Of Materials

Qty	Refdes	Value	Manufacturer	Part Number
10	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10	0.47UF	AVX	TAJA474M025R
16	C11,C13,C15,C18,C26,C27,C28,C30,C34,C35,C36, C38,C42,C46,C48,C50	0.1UF	MURATA	GRM188R71H104KA93D
11	C12,C16,C20,C23,C33,C37,C43,C44,C47,C49,C52	470PF	PANASONIC	ECJ1VC1H471J
1	C14	0.01UF	VENKEL COMPANY	C0603X7R500-103KNE
12	C17,C19,C21,C22,C29,C32,C39,C40,C41,C45,C51, C53	1000PF	VENKEL COMPANY	C0805COG500-102JNE
2	C24,C31	10PF	KEMET	C0603C100F5GAC
1	C25	10UF	VISHAY INTERTECHNOLOGY	293D106X9010A2TE3
2	C54,C55	33PF	VENKEL COMPANY	C0603C0G500-330JNE
1	D1	LED GREEN	KINGBRIGHT	K/APT-3216SGD
8	FID1,FID2,FID3,FID4,FID5,FID6,FID7,FID8	FID-040	GENERIC	FID-040
4	J1,J2,J3,J4	HDR 3X1	SAMTEC	TMM-103-02-G-S
1	J5	HDR 1X2	SAMTEC	TMM-102-02-G-S
2	J6,J7	CON 2X60	TYCO ELECTRONICS	5-5179009-5
7	L1,L2,L3,L4,L5,L6,L7	BLM31AJ601SN1L	MURATA	BLM31AJ601SN1L
1	R1	560 OHM	KOA SPEER	RK73H1JTTD5600F
5	R2,R3,R4,R5,R6	0 OHM	THYE MING TECH CO LTD	CR-03JL7-0R
1	R7	33.0 OHM	KOA SPEER	RK73H1JTTD33R0F
3	TP1,TP2,TP3	TEST POINT	NICOMATIC	C12000B
3	TP4,TP5,TP6	TEST POINT	NA	NA
1	U1	MPC5516_SKT208	Subassembly	344-00364, 210-77299
1	Y1	32.768KHz	VISHAY INTERTECHNOLOGY	XT26TTA32K768
1	Y2	8MHz	C-MAC MICROTECHNOLOGY	LF A140K