M52277EVBUM
Rev. 0.8, 03/2010

# M52277 Evaluation Board

## For MCF52277 Evaluation/Validation

by: Microcontroller Division

## 1 Introduction

The M52277 Evaluation Board (EVB) is based on the V2 ColdeFire Core with EMAC. This board is shipped with the MCF52277 populated to allow for the evaluation of all of the functionality of this part.

This board was designed as a validation platform with maximum flexibility. Where possible we've also designed for power and speed but the primary goal of this system was flexibility.

## 2 Applicable Documents

- MCF52277 Reference Manual
- Universal Serial Bus Specification, Revision 2.0

**Contents**





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# 3 Evaluation Board Overview

## 3.1 Features

The following is a list of evaluation board features.

M52277 External Interfaces:

- On Board Sharp 240 x 320 color touch screen LCD panel
- 60 pin external LCD connector
- Synchronous Serial Interface (SSI) connected to audio CODEC
- USB Support
  - MCF52277 on-chip OTG transceiver with device, host, and OTG support (Mini-AB receptacle)
- Crystal/Clock
- BDM/JTAG
- Two UARTs
- FlexBus
- Timers
- External Interrupts
- CAN Support
  - External CAN transceiver (DB9 connector)
- University Breakout Connector for serial interfaces (I2C, QSPI, GPIO, etc.)

Memory Subsystems:

- 32M x 16 Mobile DDR
- 8M x 16 NOR Flash
- 16Mbit Serial Boot Flash

Power:

- Inputs:
  - 5 V Input to the voltage regulator circuitry
- Regulated On-board voltages:
  - 3.3 V - I/O Voltage
  - 1.8 V - Mobile DDR and Flash Voltage
  - 1.5 V - MCF52277 Core Voltage

## 3.2 Board Diagram

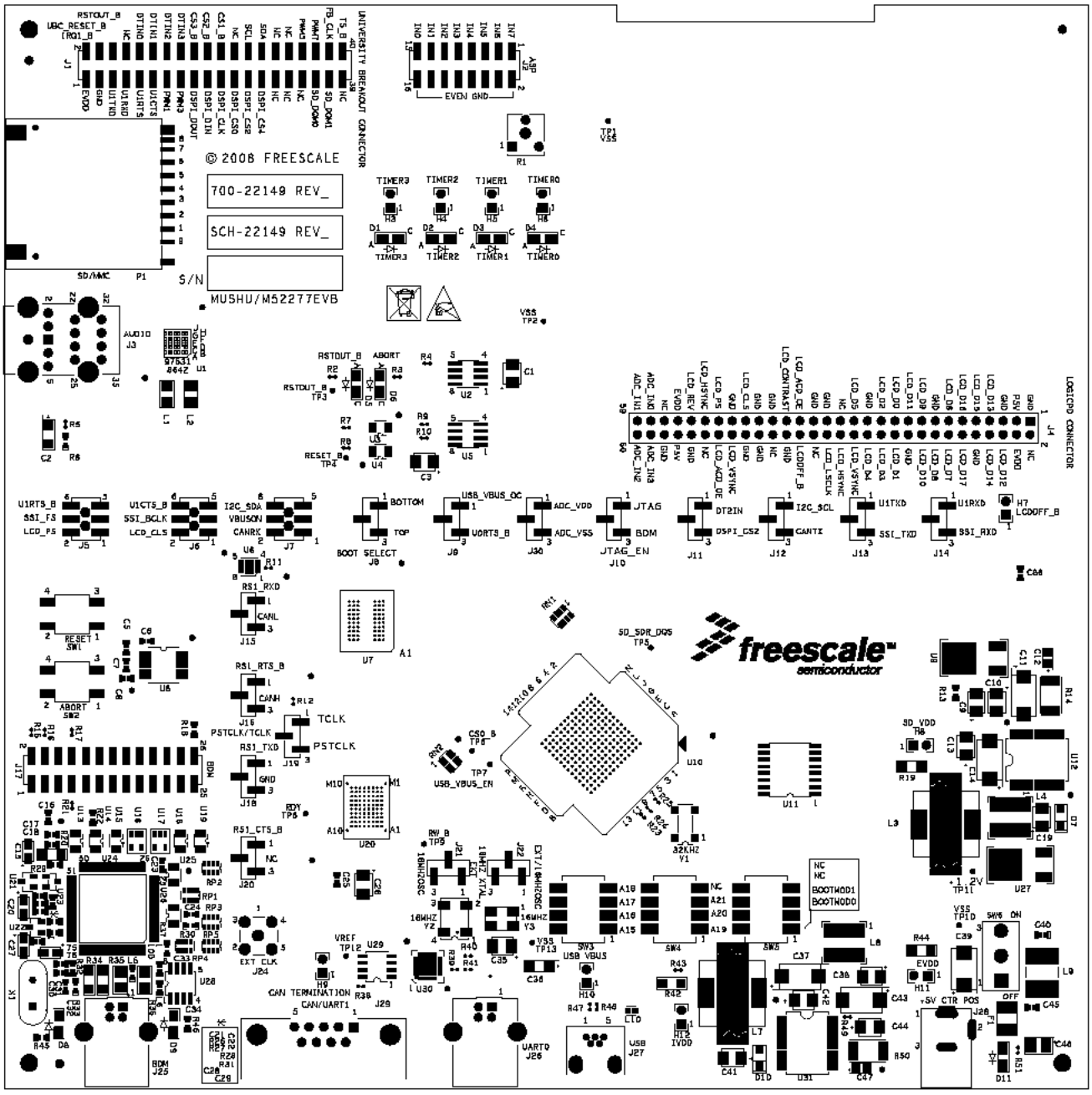


**Figure 1. Board Diagram**

**M52277 Evaluation Board, Rev. 0.8**

# 4 Memory Map

The M52277EVB contains two FlexBus memory sections. These two nonconsecutive sections were arranged so that you can easily configure one to support glueless external memories like Flash or SRAM and configure the other to use as space for unique chip-selects for non-cacheable, non-memory devices like GPIO, control structures or other I/Os.

In Table 1, you'll find the details on how we've set up the first FlexBus region on the M52277EVB. We don't set up the second FlexBus memory region.

**Table 1. FlexBus Memory Map - Region 1**

| Component | Start Address | End Address | Size |
|---|---|---|---|
| **Flash Memory** | | | |
| Spansion S29WS128J0PBFW010 | 0x0000_0000 | 0x0100_0000 | 16 MB |
| **SDRAM** | | | |
| Micron MT46H32M16LFCK-75 | 0x4000_0000 | 0x4400_0000 | 64 MB |
| **Internal SRAM** | | | |
| Internal | 0x8000_0000 | 0x8FFF_FFFF | 256MB[1] |
| **Peripheral Space** | | | |
| Internal | 0xF000_0000 | 0xFFFF_FFFF | 256MB |

[1]The actual size of the SRAM is 128KByte. However, it may be placed anywhere within the 256MB space using the RAMBAR register.

# 5 Hardware Submodules

This section describes the major sections of the M52277EVB.

## 5.1 Processor

The MCF52277 processor is the fundamental control chip on the M52277EVB. This is a Version 2 ColdFire processor running at a maximum core speed of 160MHz. The M52277EVB allows you to fully evaluate the feature set of the MCF52277 silicon. Refer to section 3.1 to review the list of board features.

## 5.2 Reset

Reset can be asserted through a push button switch, SW1. The push button switch is connected to the reset line on the chip through a Dallas DS1834 Reset chip. Reset of the chip can also be caused by the on-board BDM circuit, the University Breakout Connector, or the on board voltage regulator.

## 5.3 System Clocks

Two on-board clock sources are provided on the M52277EVB -- a 16MHz oscillator and a 16MHz crystal. Alternatively, an input clock signal can be provided via an SMA connector for test purposes. The different

clock signals and configurations are described below. Please refer to the MCF52277 Reference Manual for further information on the clocking requirements for the MCF52277.

**Table 2. M52277EVB Clock Definitions**

| Clock | Description | Frequency |
|---|---|---|
| 16MHz Input Oscillator | Jumpers J21 and J22 are used to select between clock options. Setting J21 to 2-3 and J22 to 1-2 selects the 16MHz Oscillator option. | 16MHz |
| 16MHz Input Crystal | Setting J22 to 2-3 selects the 16MHz Crystal option (In this mode, the setting of J21 is a don't care). | 16MHz |
| External Clock Input | Setting J21 to1-2 and J22 to 1-2 selects the External Clock Input option. The external clock can be input on the SMA connector J24. | Variable |

**NOTE**

If the clock selection is changed, the SW3 and SW4 switch settings need to be changed to reflect the appropriate clock input.

## 5.4 Boot and Program Flash Memory

The M52277EVB includes a serial boot flash and a program flash memory.

### 5.4.1 Program Flash

The program flash memory resides on the first block of FlexBus memory. The 128Mbit Spansion flash can be used for RTOS development. Your software must configure the memory access parameters consistent with the hardware configuration.

Jumper J8 controls the boot mode of the flash. The default position is 1-2 which selects bottom boot mode. Setting the jumper to position 2-3, selects top boot mode. This flash device is connected to CS0 and is the device from which the MCF52277 executes following reset.

### 5.4.2 Serial Boot Flash

The serial boot flash stores configuration parameters and boot code. All of this is loaded into on-chip SRAM during the processor reset sequence (i.e. when the BOOTMOD signals = 11). The serial boot flash has a dedicated interface to the MCF52277 processor. When the BOOTMOD = 11, the serial boot facility sets the configurable power-up options for the processor. As an additional option it can also load code into the processor memory space at that time.

Through interaction with the MCF52277 processor's reset controller, the serial boot facility accomplishes all of this before the MCF52277 processor reset negates, ensuring the chip is properly configured when exiting the reset state.

## 5.5 SDRAM Interface

The M52277EVB provides 64 Mbytes of on-board Mobile SDRAM (16bit x 32M Micron Mobile SDRAM). On-board terminations are provided.

## 5.6 BDM and JTAG Interfaces — Processor

The M52277EVB provides a BDM (Background Debug Mode) and JTAG Connector (26-pin header), J17, to give the end-user the ability to utilize the BDM/JTAG features of the MCF52277 processor. In addition, the M52277EVB provides an on board USB to BDM interface, J25.

## 5.7 USB 2.0 Host and Device

The MCF52277 Processor contains a USB OTG module. This module is USB 2.0 compliant. It supports host and device modes, and provides an on-chip full-speed/low-speed transceiver. One mini-AB receptacle (USB 2.0 OTG) is provided on the M52277EVB.

## 5.8 Interrupts

Three are three external interrupt pins provided on the MCF52277. IRQ7_B is connected to push button switch SW2 to provide a user driven ABORT signal. This signal is also connected to the LED D6 to denote when this signal is asserted.

IRQ1_B and IRQ4_B are available on the University Breakout Connector, J1. IRQ1_B is also used as the DAT1 line for the SD/MMC interface. IRQ4_B is also used as the DSPI chip select, DSPI_CS4 for the Audio CODEC.

## 5.9 Timers

The MCF52277 provides four 32-bit timers with DMA support. DT0 - DT3 are connected to LEDs D4 - D1. They can be disconnected from the LEDs by removing jumpers H6 - H3.

## 5.10 DSPI

The DSPI Module on the MCF52277 interfaces with a 16Mbit Serial Flash memory and a TI stereo audio CODEC. Both use the DSPI in SPI bus interface mode.

## 5.11 RS232

The MCF52277 includes 3 UART modules. The M52277EVB provides one standard RS232 line driver necessary to interface with RS232 connectors. The board also supplies a USB-to-UART bridge to interface with the MCF52277's UART0. If using this option, a USB type B connector can be used to interface with an external device, instead of the standard RS232 connector.

## 5.12 Power Regulation

The M52277EVB provides two Freescale QuiccSupply MC34702 power regulators. These power regulators provide 3.3V, 1.8V, and 1.5V to devices on the board. The regulators generate these voltages from a 5V external supply. The 5V supply is provided through a barrel jack connector. A power switch is provided to turn power to the board off.

Jumpers are provided that allow for the 3.3V, 1.8V, and 1.5V supplies to be separated from the MCF52277. The intention of these jumpers is to connect a current meter to measure the power consumed by the MCF52277 processor.

## 5.13 Boot Options

The MCF52277 has three boot options:

- Boot from FlexBus, RCON defaults
- Boot from FlexBus and override RCON (Parallel RCON)
- Boot from serial boot flash

The boot mode is determined by the BOOTMOD[1:0] inputs into the MCF52277. The mode switches (SW5[2:1]) control the BOOTMOD[1:0] inputs to the MCF52277.

When booting from FlexBus with overrides from the data bus, the SW3 and SW4 settings control the state of FB_AD[7:0] during reset (while /RSTOUT is asserted). The following table describes the override settings.

**Table 3. SW3, SW4, and SW5 Settings**

| Pins Affected | Switch Settings[1] | Function |
|---|---|---|
| (none) | **SW5-1/SW5-2** | **Boot Mode** |
| | OFF/OFF | Boot from SPI Flash and override RCON (Serial RCON) |
| | **OFF/ON** | Boot from FlexBus with RCON defaults, split bus (16-Bit/16-Bit) |
| | ON/OFF | Boot from FlexBus override RCON (Parallel RCON) |
| | ON/ON | Boot from FlexBus with RCON defaults, unified bus (32-Bits) |
| (none) | **SW4-1** | **PLL Mode** |
| | ON | Limp Mode |
| | **OFF** | PLL Mode |
| A[23:22] | **SW4-2** | **Chip Select Mode** |
| | ON | A[23:22] = FB_CS[5:4] |
| | **OFF** | A[23:22] = A[23:22] |
| (none) | **SW4-3** | **Memory Mode** |
| | ON | SDR Mode |
| | **OFF** | DDR Mode |
| (none) | **SW3-1** | **Master Mode** |
| | **ON** | Master Mode |
| | OFF | Reserved |

**Table 3. SW3, SW4, and SW5 Settings (continued)**

| Pins Affected | Switch Settings[1] | Function |
|---|---|---|
| (none) | **SW3-2** | **Clock Mode** |
| | **ON** | Oscillator Bypass Mode |
| | OFF | Crystal Oscillator Mode |
| FB_D[31..0] | **SW3-3** | **Port Size** |
| | **ON** | 16-Bit Boot Port (Split and Unified Bus) |
| | OFF | 8-Bit Boot Port (Split Bus) or 32-Bit Boot (Unified) |
| (none) | **SW3-4** | **Drive Strength** |
| | **ON** | High Drive Strength |
| | OFF | Low Drive Strength |

[1] Bold indicates the default setting, SW5-3, SW5-4, and SW4-4 are not connected and their position does not affect configuration.

## 5.14 Jumpers, Headers, and Switches

There are several jumpers on the M52277EVB that allow for user control of the hardware configuration. The following table provides descriptions for all the jumper settings.

**Table 4. Jumper Settings**

| Reference Designator | Setting[1,2] | Function |
|---|---|---|
| H3 | **ON** | Connects DT3IN to LED D1 |
| | OFF | Leaves DT3IN disconnected |
| H4 | **ON** | Connects DT2IN to LED D2 |
| | OFF | Leaves DT2IN disconnected |
| H5 | **ON** | Connects DT1IN to LED D3 |
| | OFF | Leaves DT1IN disconnected |
| H6 | **ON** | Connects DT0IN to LED D4 |
| | OFF | Leaves DT0IN disconnected |
| H7 | **ON** | Connects PI2C1 to the LCD SHDN_B pin to be used as LCDOFF_B |
| | OFF | Leaves PI2C1 disconnected |
| H8 | **ON** | 1.8V Current Measurement Header |
| H9 | **ON** | Adds 120 OHM termination between CANH and CANL lines |
| | OFF | Removes 120 OHM termination between CANH and CANL lines |
| H10 | **ON** | Connects the on board generated VBUS to the VBUS signal on the mini USB connector J27 |
| | OFF | Leaves the VBUS signal on the mini USB connector J27 disconnected |

**Table 4. Jumper Settings (continued)**

| Reference Designator | Setting[1,2] | Function |
|---|---|---|
| H11 | **ON** | 3.3V Current Measurement Header |
| H12 | **ON** | 1.5V Current Measurement Header |
| J5 | **1-2** | Sets the U1RTS_B/LCD_PS signal up as LCD_PS for LCD operation |
| | 3-4 | Sets the U1RTS_B/LCD_PS signal up as SSI_FS or SSI operation |
| | 5-6 | Sets the U1RTS_B/LCD_PS signal up as U1RTS_B for UART operation |
| J6 | **1-2** | Sets the U1CTS_B/LCD_CLS signal up as LCD_CLS for LCD operation |
| | 3-4 | Sets the U1CTS_B/LCD_CLS signal up as SSI_BCLK or SSI operation |
| | 5-6 | Sets the U1CTS_B/LCD_CLS signal up as U1CTS_B for UART operation |
| J7 | 1-2 | Sets the I2C_SDA/CANRX signal up as CANRX for CAN operation |
| | **3-4** | Sets the I2C_SDA/CANRX signal up as VBUSON for USB operation |
| | 5-6 | Sets the I2C_SDA/CANRX signal up as I2C_SDA for I2C operation |
| J8 | **1-2** | Selects Bottom Boot Mode for the flash |
| | 2-3 | Selects Top Boot Mode for the flash |
| J9 | **1-2** | Sets the U0RTS_B/USB_VBUS_OC signal up as USB_VBUS_OC for USB operation |
| | 2-3 | Sets the U0RTS_B/USB_VBUS_OC signal up as U0RTS_B for UART operation |
| J10 | 1-2 | Enables JTAG on the MCF52277 |
| | **2-3** | Enables BDM on the MCF52277 |
| J11 | **1-2** | Sets the DT2IN/DSPI_CS2 signal up as DT2IN for Timer operation |
| | 2-3 | Sets the DT2IN/DSPI_CS2 signal up as DSPI_CS2 for Serial Boot Flash operation |
| J12 | **1-2** | Sets the I2C_SCL/CANTX signal up as I2C_SCL for I2C operation |
| | 2-3 | Sets the I2C_SCL/CANTX signal up as CANTX for CAN operation |
| J13 | 1-2 | Sets the U1TXD/SSI_TXD signal up as U1TXD for UART operation |
| | **2-3** | Sets the U1TXD/SSI_TXD signal up as SSI_TXD for SSI operation |
| J14 | 1-2 | Sets the U1RXD/SSI_RXD signal up as U1RXD for UART operation |
| | **2-3** | Sets the U1RXD/SSI_RXD signal up as SSI_RXD for SSI operation |
| J15 | **1-2** | Connects pin 2 of the DB-9 connector J29 to RS1_TXD for UART operation |
| | 2-3 | Connects pin 2 of the DB-9 connector J29 to CANL for CAN operation |
| J16 | **1-2** | Connects pin 7 of the DB-9 connector J29 to RS1_CTS_B for UART operation |
| | 2-3 | Connects pin 7 of the DB-9 connector J29 to CANH for CAN operation |
| J18 | **1-2** | Connects pin 3 of the DB-9 connector J29 to RS1_RXD for UART operation |
| | 2-3 | Connects pin 3 of the DB-9 connector J29 to GND for CAN operation |
| J19 | 1-2 | Sets the PSTCLK/TCLK signal up as TCLK |
| | 2-3 | Sets the PSTCLK/TCLK signal up as PSTCLK for BDM Debug (Default for this jumper is “not installed”) |

**Table 4. Jumper Settings (continued)**

| Reference Designator | Setting[1,2] | Function |
|---|---|---|
| J20 | **1-2** | Connects pin 8 of the DB-9 connector J29 to RS1_RTS_B for UART operation |
| | 2-3 | Connects pin 8 of the DB-9 connector J29 to NC for CAN operation |
| J21 | 1-2 | Sets the clock input to be from an external source input on the SMA connector J24 |
| | **2-3** | Sets the clock input to be from an on board 16MHz Oscillator |
| J22 | 1-2 | Sets the clock input to be either from an external source or an on board 16MHz Oscillator, depending on the setting of J21 |
| | **2-3** | Sets the clock input to be from an on board 16MHz crystal |
| J30 | **1-2** | Connects the ADC_REF signal to ADC_VDD |
| | 2-3 | Connects the ADC_REF signal to ADC_VSS |

1 Bold indicates the default setting

2 ON indicates that a shunt should be fitted on the jumper; OFF indicates that no shunt should be applied.

The following table provides a description for the interface connectors.

**Table 5. Interface Connectors**

| Reference Designator | Function |
|---|---|
| J1 | University Breakout Connector |
| J2 | ASP Connector |
| J3 | 3 Port Audio Connector |
| J4 | LogicPD LCD Connector |
| J17 | BDM Connector |
| J24 | SMA Connector for external clock source |
| J25 | USB B Connector - Used to communicate with the M52277EVB's on board USB to BDM Debug Port |
| J26 | USB B Connector - Used to communicate with on board serial to USB converter connected to UART0 |
| J27 | Mini USB A/B Connector - Connected to the MCF52277's on chip USB interface |
| J28 | 5V Center Positive 1.94mm maximum pin diameter power jack |
| J29 | DB9 Socket used for CAN or UART operation depending on the Setting of Jumpers J15, J16, J18, and J20 |
| J500 | Sharp LCD Connector - 1X50 FPC ZIF |
| J501 | Sharp LCD Touchscreen Connector - 1X4 FPC ZIF |

The following table provides a description of the various switches on the board.

**Table 6. Switches**

| Reference Designator | Function |
|---|---|
| SW1 | Board Reset push button |
| SW2 | Abort Reset push button - Connected to IRQ7_B |
| SW3 | Board Configuration switch. See Boot Options section for more information. |
| SW4 | Board Configuration switch. See Boot Options section for more information. |
| SW5 | Board Configuration switch. See Boot Options section for more information. |
| SW6 | Power Switch |

The following table provides a description of the various test points on the board.

**Table 7. Test Points**

| Reference Designator | Signal |
|---|---|
| TP1 | VSS |
| TP2 | VSS |
| TP3 | RSTOUT_B |
| TP4 | RESET_B |
| TP5 | SD_SDR_DQS |
| TP6 | CS0_B |
| TP7 | USB_VBUS_EN |
| TP8 | FLASH RDY |
| TP9 | RW_B |
| TP10 | VSS |
| TP11 | V1.2 |
| TP12 | CAN VREF |
| TP13 | VSS |