MG2475

(No.ADS1101)

Revision 1.0

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DataSheet

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Revision History

Revision No.	Date	Description
V1.0	2015-07-30	• First version is released.

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1 INTRODUCTION

MG2475AZZ-F340C (hereinafter called "MG2475") is a true 2.4 GHz system-on-chip (SOC) designed for low-power and low-cost applications based on industry standards, IEEE802.15.4 and RF4CE. Some special features and peripherals such as peripherals DMA, memory and I/O retention under the power down modes, etc are added to achieve both enhanced performance and low-power. MG2475 uses an ISM band of 2.4 ~ 2.48 GHz. In addition to the standard 250Kbps data-rate specified in IEEE802.15.4, enhanced high data-rate mode (1Mbps) with channel coding is supported.

MG2475 combines an advanced RF transceiver with an industry-standard enhanced 8051 MCU, a baseband PHY, a MAC with AES-128 HW engine, an in-system programmable 64KB flash memory, a 7-KB RAM, and many other application-specific peripherals. For voice applications, the voice encoder/decoder of ADPCM and µ/a-law are embedded.

MG2475 fits best for low-cost and low-power RF4CE remote control applications.

APPLICATIONS

- -2.4 GHz IEEE 802.15.4 Applications

- - RF4CE Remote Control Systems

- - Lighting Systems

- - Voice Applications

- - Home/Building Automation

- - Industrial Control and Monitoring

- - Energy Management

- - Low Power Wireless Sensor Networks

- - Consumer Electronics

- - Health-care equipment

- - Toys

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2 KEY FEATURES

RF Transceiver

- Integrated 2.4GHz RF Transceiver
- Low Power Consumption
- High Sensitivity of −98.5 dBm at 250kbps
- No External T/R Switch or Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9.0dBm
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- High Data Rate including 250Kbps specified in IEEE802.15.4: 1Mbps
- RSSI Measurement
- Compliant to IEEE802.15.4

Hardwired MAC

- Two 128-byte FIFOs for Modem Tx and Rx
- CRC-16 Computation and Check
- Address filtering enhanced
- Voice MAC header H/W generation

8051-Compatible MCU

- 8051 Compatible (single cycle execution)
- 64KB Embedded Flash Memory
- 7KB Data Memory (support the retention in all power down modes, power-off is possible)
- 128-byte CPU dedicated Memory(support the retention in all power down modes, power-off is possible)
- 1KB Boot ROM
- Dual DPTR Support
- 4-channels peripheral DMA(channel 0 is only for MAC RX)
- AES-128 Encryption/Decription Engine
- ECC(Error Checking and Correction) logic for the Flash or RAM data integrity
- I2S/PCM Interface with two 128-byte FIFOs
- μ-law/a-law/ADPCM Voice Encoder/Decoder
- Two High-Speed UARTs with Two 16-byte FIFOs(up to 1Mbps)
- Four Timer/Counters
- 5 PWM channels
- Watchdog Timer

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- Sleep Timer using the 32kHz internal RC-OSC
- Quadrature Signal Decoder
- 22 General Purpose I/Os (support the retention in deep sleep mode)
- 16 MHz RC oscillator for the fast start-up from reset & power-down mode
- On-chip Power-on-Reset and Brown-out detector
- SPI Master/Slave Interface with two 16-byte FIFOs
- I2C Master/Slave with 16-byte FIFO
- Programmable IR(Infra-Red) Modulator
- ISP (In System Programming)
- External clock output function(500KHz, 1/2/4/8/16/32 MHz selectable)

Clock Inputs

- 32MHz Crystal for System Clock

Power

- 1.2V(Core)/2.0~3.6V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Power Supply Range for Internal Regulator(2.0V(Min) ~ 3.6V(Max))

Package

- Lead-Free 40-pin QFN Package (6mm x 6mm)

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3 BLOCK DIAGRAM

[Figure 1] shows the block diagram of MG2475. MG2475 consists of a 2.4GHz RF, a baseband PHY, a MAC hardware engine, an industry-standard enhanced 8051 MCU, an in-system programmable flash memory 64KB, a 7KB data RAM, and rich peripherals such as a voice encoder/decoder block, I2C, 5-channel PWM.

Figure 1. Functional Block Diagram of MG2475

MG2475 integrates an RF transceiver compliant to IEEE802.15.4 RF. The RF transceiver operates on an ISM band of 2.4 ~ 2.48GHz with excellent receiver sensitivity and programmable output power up to +9dBm.

The MAC block supports IEEE802.15.4 compliant functions and it is located between the microprocessor and the baseband modem. MAC block includes FIFOs for transmitting/receiving packets, a CRC generation and the enhanced address filtering and its control circuit. In addition, it supports automatic CRC check and address decoding. And AES engine for security is accessed like the general 8051 peripheral and operated through direct data memory access without 8051 intervention.   Also, MG2475 supports the ECC (Error Checking and Correction logic) code generation per 512-bytes for guaranteeing the reliable memory data integrity.

The 4-channels DMA block enables efficient, high-speed operation of the peripherals such as UARTs, SPI, etc by reducing the load on the CPU. The DMAC of MG2475 only supports the data transfer between peripheral FIFOs and the DMA buffers in data memory. The channel-0 of DMAC is only for the baseband modem RX FIFO.

MG2475 integrates a high performance embedded microcontroller, compatible to industry standard 8051 microcontroller in an instruction level. This embedded microcontroller has 8-bit operation architecture sufficient for controller applications. The embedded microcontroller has 4-stage pipeline architecture to improve the performance over previous compatible chips making it capable of executing simple instructions during a single

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cycle.

The memory part of the embedded microcontroller consists of program memory and data memory. The data memory has 2 memory areas. For more detailed explanations, refer to Section 7.1.2 Data Memory.

MG2475 includes 22 GPIOs and rich peripherals to aid in the development of the application circuit with the various external peripherals interface. All I/O pins are retained in deep sleep mode such as PM2 and PM3. MG2475 uses 32MHz crystal oscillator for RF PLL and 8MHz clock generated from 32MHz in clock generator is used as the default clock of 8051 MCU subsystem. The clocks for MAC, a baseband modem are separately controlled by the internal clock controller block.

MG2475 supports a voice function as follows. The data generated by an external ADC is inputted to the voice block via I2S interface. After the data is received via I2S, it is compressed by the voice encoder and stored in the Voice TXFIFO. Then the data in the Voice TXFIFO is transferred to the MAC TXFIFO and transmitted via PHY. On the other hand, the received data in the MAC RXFIFO is transferred to voice RXFIFO through the internal direct path. Then the data in the Voice RXFIFO is decompressed in the internal voice decoder. After that, the decompressed data is transferred to the external DAC via I2S interface.

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4 PIN DESCRIPTION

The pin-out diagram of MG2475 is shown in [Figure 2]. The description for that is summarized in [Table 1].
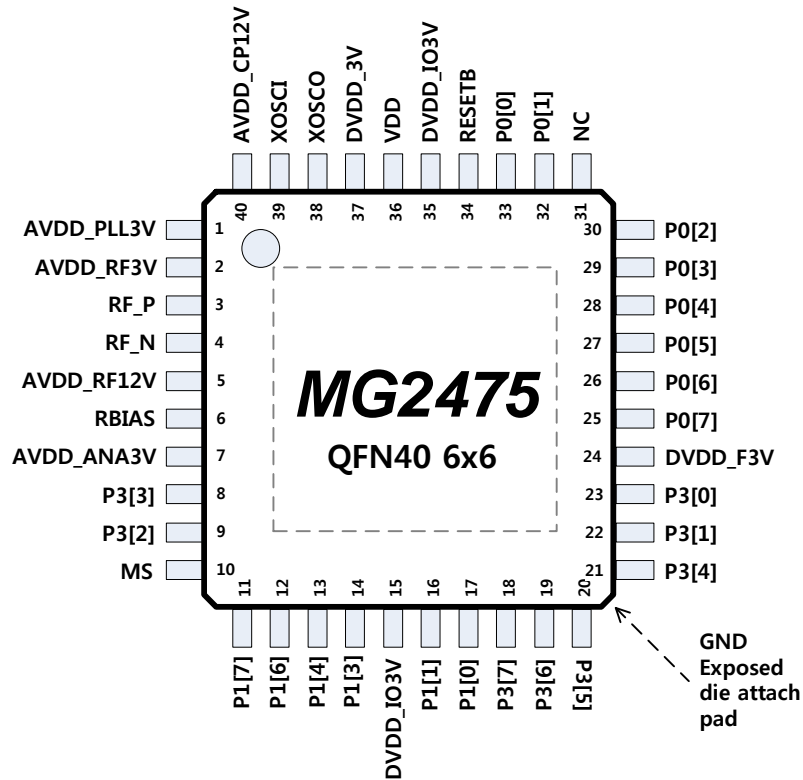
Figure 2. Pinout Top View of MG2475

NOTE: The exposed ground pad is located at the bottom of the chip and electrically connected to the die ground inside the package. It must be connected to a solid ground plane.

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Table 1. Pin Description

Radio, Synthesizer, and Oscillator			
Name	Pin	Type	Description
AVDD_PLL3V	1	Power	2.0V to 3.6V RF/Analog power supply connection
AVDD_RF3V	2	Power	2.0V to 3.6V RF/Analog power supply connection
AVDD_ANA3V	7	Power	2.0V to 3.6V RF/Analog power supply connection
AVDD_RF12V	5	Power	Regulated Output of AVDD_RF3V for PA bias
AVDD_CP12V	40	Power	Regulated Output of AVDD_PLL3V for decoupling
RF_P	3	RF I/O	Positive RF input signal to LNA in RX mode Positive RF output signal from PA in TX mode
RF_N	4	RF I/O	Negative RF input signal to LNA in RX mode Negative RF output signal from PA in TX mode
RBIAS	6	Analog I/O	External precision bias resistor(510kohm) to generate the reference current
Digital and Oscillator			
Name	Pin	Type	Description
DVDD_IO3V	15, 35	Power	2.0V to 3.6V Digital power supply connection(I/O supply)
DVDD_F3V	24	Power	2.0V to 3.6V Digital power supply connection(Flash supply)
DVDD_3V	37	Power	2.0V to 3.6V Digital power supply connection to digital regulator input
VDD	36	Power	1.2V Regulated Output of DVDD_3V for decoupling *Note: Do not use for supplying external circuits.
RESETB	34	Digital input	External Reset pin, active low
MS	10	Digital input	Mode slection 0 = Normal Mode, 1= ISP Mode
P0[0]	33	Digital I/O	Port P0.0/I2SRX_DI/PWM0
P0[1]	32	Digital I/O	Port P0.1/I2SRX_LRCLK/PWM1
P0[2]	30	Digital I/O	Port P0.2/I2SRX_BCLK/PWM2
P0[3]	29	Digital I/O	Port P0.3/I2SRX_MCLK/PWM3
P0[4]	28	Digital I/O	Port P0.4/I2STX_DO/PWM4/TRSWB

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P0[5]	27	Digital I/O	Port P0.5/I2STX_LRCLK/PTC_GATE0/TRSW
P0[6]	26	Digital I/O	Port P0.6/I2STX_BCLK/PTC_GATE1
P0[7]	25	Digital I/O	Port P0.7/I2STX_MCLK/PTC_GATE2
P1[0]	17	Digital I/O	Port P1.0/RXD1
P1[1]	16	Digital I/O	Port P1.1/TXD1
P1[3]	14	Digital I/O	Port P1.3/QUADZA/PTC_GATE3/IR_TX/CLK_OUT
P1[4]	13	Digital I/O	Port P1.4/QUADZB/EXT_RTC_CLK/PTC_GATE4
P1[6]	12	Digital I/O	Port P1.6/I2C_SCL
P1[7]	11	Digital I/O	Port P1.7/I2C_SDA
P3[0]	23	Digital I/O	Port P3.0/RXD0/QUADXA
P3[1]	22	Digital I/O	Port P3.1/TXD0/QUADXB
P3[2]	9	Digital I/O	Port P3.2/nINT0
P3[3]	8	Digital I/O	Port P3.3/nINT1/ATEST0
P3[4]	21	Digital I/O	Port P3.4/RTS0/QUADYA/SPIDI/T0
P3[5]	20	Digital I/O	Port P3.5/CTS0/QUADYB/SPIDO/T1
P3[6]	19	Digital I/O	Port P3.6/RTS1/SPICLK
P3[7]	18	Digital I/O	Port P3.7/CTS1/SPICSN
XOSCI	39	Analog I/O	32MHz crystal oscillator pin
XOSCO	38	Analog I/O	32MHz crystal oscillator pin or external clock input
Ground			
Exposed bottom		Ground	Ground for RF, Analog, digital core, and I/O
NC			
NC	31	NC	-

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Table 2. I/O Pins Equivalent Circuit Summary

Equivalent Circuit Schematic	Reset Status	Note
GPIOs(P0[7:0], P1[1:0], P1[7:6], P3[7:0])		
	Input with pull-up	I/O with the programmable pull-up/pull-down function
RESETB		
	input with pull-up	External Reset Input, Low Active
MS		
	input with pull-down	Mode Selection Pin (0: Normal, 1: ISP)

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ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter		Min.	Max	Unit	
Supply Voltage (AVDD_PLL3V, AVDD_RF3V,AVDD_ANA3V, DVDD_3V,DVDD_F3V, DVDD_IO3V)		-0.3	3.6	V	All supply pins must have the same voltage.
Core voltage(AVDD_RF12V, AVDD_ANA12V, VDD, XOSCI, XOSCO)		-0.3	1.32	V	
Storage Temperature		-40	150	°C	
ESD	HBM		2000	V	According to human-body model(JEDEC STD 22)
	MM		200	V	According to machine model(JEDEC STD 22)
	CDM		1000	V	According to charged-device model(JEDEC STD 22)

Exceeding one or more of these ratings may cause permanent damage to the device.

These are stress ratings only, and the functional operation of the device at these or any other conditions beyond those indicated under "ELECTRICAL SPECIFICATIONS" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: These values were obtained under worst-case test conditions specially prepared for the MG2475 and these conditions are not sustained in normal operation environment.

Caution: ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.

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5.2 Recommended Operating Conditions

Parameter	MIN	MAX	UNIT
Operating ambient temperature range, TOP	-40	125	℃
Operating supply voltage, VDD (AVDD_PLL3V, AVDD_RF3V,AVDD_ANA3V, DVDD_3V,DVDD_F3V, DVDD_IO3V)	2	3.6	V
Voltage on any digital pin	-0.3	VDD	V

5.3 Digital IO DC Characteristics

All voltage values are based on AGND.

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DDIO}	I/O supply voltage(DVDD_IO3V)	2.0	3.0	3.6	V
AGND	Chip ground		0		V
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{OH}	Output high voltage	2.4			V
V_{OL}	Output low voltage			0.4	V
R_{PU}	Pull-up Resistance		66		kΩ
R_{PD}	Pull-down Resistance		66		kΩ
R_{SPU}	Strong Pull-up Resistance (@ DVDD_IO3V=3.3V)	1.42	1.62	1.92	kΩ

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5.4 Current Consumption and Timing Characteristics

TOP = 25°C, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
MCU active. No radio and peripherals (UART1&RNG) active. @ MCU clock = 8MHz @ MCU clock = 16MHz		2.13 3.28		mA
RX mode. MCU active @ MCU clock = 8MHz		16.3		mA
TX mode. MCU active @ MCU clock = 8MHz @ +9 dBm Output Power @ +8 dBm Output Power @ +7 dBm Output Power @ +6 dBm Output Power @ +5 dBm Output Power @ +4 dBm Output Power @ +3 dBm Output Power @ +2 dBm Output Power @ +1 dBm Output Power @ 0dBm Output Power		36.5 30.8 27.0 24.1 22.4 21.3 19.9 19.7 18.7 16.9		mA
Power mode1. Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off, 32kHz RCOSC, POR, BOD, and sleep timer active.		7.6		µA
Power mode2. Digital regulator off, retention mode 1(7KB SRAM retained), GPIO retention, 16MHz RCOSC and 32MHz crystal oscillator off, 32kHz RCOSC, POR, BOD, and sleep timer active.		4.6		µA
Power mode3. Digital regulator off, retention mode 3(all digital off), GPIO retention, 16MHz RCOSC, 32MHz crystal oscillator, 32kHz RCOSC, BOD and sleep timer off.		1.7		µA
Wake-up and timing				
Power mode1 → MCU Active Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of 16MHz RCOSC		200		µs
Power mode2 → MCU Active Digital regulator off, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of regulator and 16MHz RCOSC		380		µs
MCU Active → TX or RX (Power mode1) Initially running on 16MHz RCOSC, Added start-up time of 32MHz crystal oscillator.		1.16		ms
MCU Active → TX or RX (Power mode2) Initially running on 16MHz RCOSC, Added start-up time of 32MHz crystal oscillator.		1.054		ms
TX/RX and RX/TX turnaround			192	µs

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5.5 RF Receive Section

Measured on 2-layer reference design with TOP=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range[1](center frequency)	2405		2480	MHz
Maximum input level (PER≤1%) @ 1000kbps @ 250kbps		10 10		dBm
Spurious radiation @ 30MHz – 1000MHz @ 1GHz – 12.75GHz		-70 -70		dBm
Received RF bandwidth		2		MHz
Channel spacing[2]		5		MHz
Receiver sensitivity (PER≤1%, PSDU length of 20-byte) @ 1000kbps @ 250kbps		-95 -98.5		dBm

Adjacent channel rejection @ 250 kbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps)
        +5MHz
        -5MHz
		36.2
		34.7
				dB

Adjacent channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps)
        +5MHz
        -5MHz
		31.2
		31.4
				dB

Adjacent channel rejection @ 250 kbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps, filtered)
        +5MHz
        -5MHz
		48.4
		48.8
				dB

Adjacent channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±5MHz, PER=1%, 250kbps, filtered)
        +5MHz
        -5MHz
		46.9
		46.2
				dB

Alternate channel rejection @ 250 kbps (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps)
        +10MHz
        -10MHz
		47.7
		48.1
				dB

Alternate channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps)				

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[1] Extended range: 2394~2507MHz

[2] Specified in IEEE Standard 802.15.4[TM]

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+10MHz -10MHz		43.7 43.6	

Alternate channel rejection (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps, filtered)
    +10MHz
    -10MHz
		
		56.2
		57.0	

Alternate channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at ±10MHz, PER=1%, 250kbps, filtered)
    +10MHz
    -10MHz
		
		54.8
		56.2
			dB

Others channel rejection (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps)
    ≥+15MHz
    ≥-15MHz
		
		58.4
		58.5
			dB

Others channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps)
    ≥+15MHz
    ≥-15MHz
		
		56
		55.3
			dB

Others channel rejection (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps, filtered)
    ≥+15MHz
    ≥-15MHz
		
		63.3
		64.1	

Others channel rejection @ 1 Mbps (-82 dBm, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps, filtered)
    ≥+15MHz
    ≥-15MHz
		
		61.6
		62.5
			dB

Co-channel rejection (-82 dBm. Undesired IEEE 802.15.4 modulated signal at the same frequency. Signal level for PER=1%, 250kbps)		-4	dB
Co-channel rejection @ 1 Mbps (-82 dBm. Undesired IEEE 802.15.4 modulated signal at the same frequency. Signal level for PER=1%, 250kbps)		-8	dB
Wifi Rejection @ 250 kbps (-82 dBm, 802.11n (BW40MHz), @ ±27 MHz offset)		45.5	
Wifi Rejection @ 1 Mbps (-82 dBm, 802.11n (BW40MHz), @ ±27 MHz offset)		44	dB

Blocking/desensitization
    -250MHz
    -100MHz
    -50MHz
    +50MHz
    +100MHz
    +250MHz
		
		-28
		-30
		-26.7
		-28
		-26.3
		-23.2
			dBm

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Blocking/desensitization @ 1 Mbps (wanted signal is with power 3 dB larger than sensitivity, -92 dBm)				
-250MHz		-25.8		
-100MHz		-26.9		
-50MHz		-25.6		dBm
+50MHz		-27.0		
+100MHz		-25.8		
+250MHz		-23.9		
RSSI dynamic range		95		dB
RSSI accuracy		±3		dB

5.6 RF Transmit Section

Measured on 2-layer reference design with TOP=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range[3](center frequency)	2405		2480	MHz
TX output power (using the recommended matching circuit)		9		dBm
Transmit chip rate		2		Mcps
Error vector magnitude (EVM)		6		%
Harmonics				
2nd harmonic		-45		dBm
3rd harmonic		-50		
Spurious emission (complies with EN 300-440, FCC and ARIB STD-T66)				
30Hz ~ 1GHz		-60		
1GHz ~ 12.75GHz		-70		dBm
1.8 ~ 1.9GHz		-70		
5.15 ~ 5.3GHz		-70		

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[3] Extended range: 2394~2507MHz

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5.7 Frequency Synthesizer

TOP=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier @ ±100kHz offset @ ±1MHz offset @ ±2MHz offset @ ±3MHz offset @ ±5MHz offset @ ±10MHz offset @ ±50MHz offset		 -82.3 -108.8 -116.6 -120 -125.2 -134.9 -151.7		dBc/Hz
Lock time			80	µs

5.8 32MHz Crystal Oscillator

T_{OP}=25℃, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Crystal frequency		32		MHz
Crystal frequency accuracy requirement	-40		40	ppm
Equivalent series resistance(ESR)		30[4]		Ω
Crystal shunt capacitance(CO)		5[4]		pF
Crystal load capacitance(CL)		13[4]		pF
Start-up time			0.8	ms

5.9 32kHz RC Oscillator

T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Calibrated frequency		32.787		kHz
frequency accuracy after calibration	-0.3		0.3	%
Initial calibration time		5.6		ms
Start-up time			100	µs

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[4] Equivalent series resistance, Crystal shunt capacitance (CO) and Load capacitance (CL) can vary with the selection of Crystal Oscillator.

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5.10 Flash Memory

5.10.1 Flash memory characteristics

Characteristic	Symbol	Conditions	MIN	TYP	MAX	UNIT
Endurance	Nendu	20 ms erase and 20 us program time	10,000			cycles
Data retention	Tret	85 °C	10			years

5.10.2 Flash memory and page size

Name	Size	Unit
Flash main memory block	65,536	bytes
Flash information block	4,096	bytes
Flash page size	2048	bytes

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6 REFERENCE APPLICATION CIRCUITS

A typical application diagram of the MG2475 is shown in [Figure 3]. Only a few external components are required for the operation of the MG2475. [Table 3] describes the external components including decoupling capacitors.

The inductor, L_1 is used as a matching component for the LNA and as an output load for the PA. The components near the RF_P/RF_N pins, L_2, L_3, C_2, and C_3 form a balun which converts the differential RF signals to a single-ended RF signal. And, L_4, C_4, and C_5 form a LC harmonic filter to suppress the TX output harmonics. In addition, C_4 is needed for DC blocking. All together with adequate values, they also transform the impedance to match a 50-Ohm antenna. As shown in [Figure 3], to provide supply current for TX output stage, RF_P and RF_N should be biased by AVDDRF_12V through L_1 and L_3.

The 32MHz crystal provides the reference frequency source for MG2475. C_6 and C_7 are loading capacitors of it. C_{D1}, C_{D2}, C_{D3}, C_{D4}, C_{D5}, and C_8 are supply decoupling capacitors, whose values depend on PCB artwork and stack-up information.

The components' values listed in [Table 3] are selected for 2-layer reference PCB design.
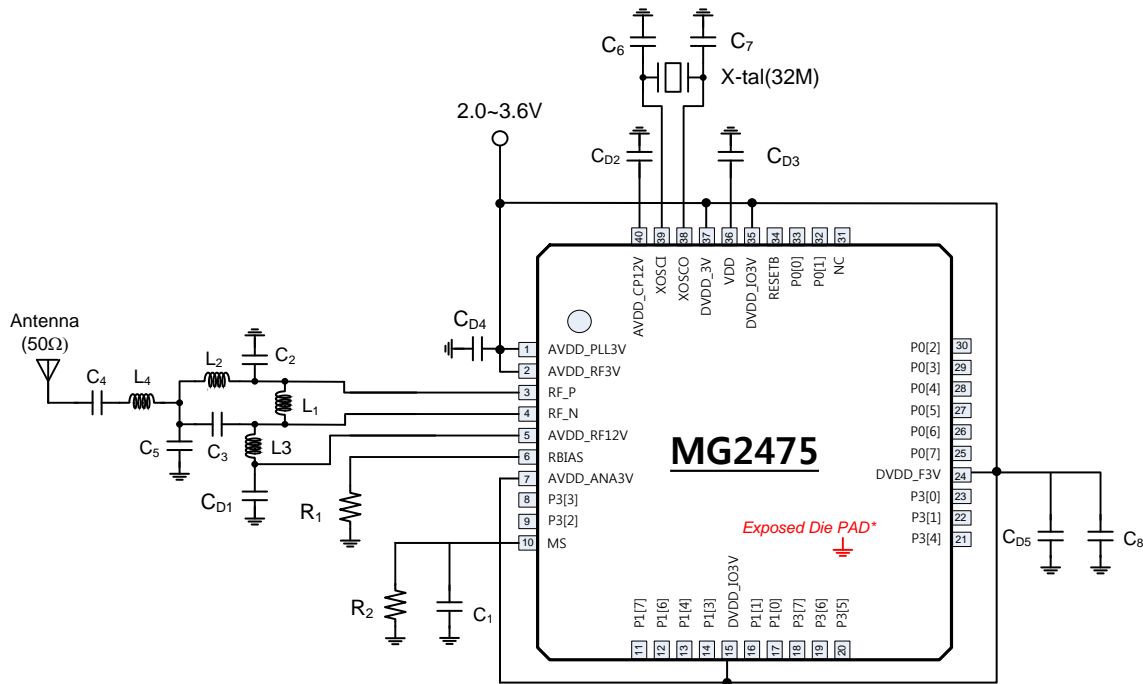
Figure 3. MG2475 Typical Application Circuit

* GND is bottom pad (down-bonding pad) in the above schematic

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In applications, some GPIO pins (among P0, P1 and P3) may be unused. Then, the unused GPIO pins are recommended to be set as inputs with pull-up enabled: the input pull-up is the default state of the GPIO pins. For the detailed register configuration on the GPIOs, please refer to the Section 8.2.

Table 3. Bill of Materials for Figure 3

No	Component	Description	Value
1	C_1	MS control signal filter capacitor	1uF
2	L_1	RF matching inductor	5.1nH
3	L_2, L_3	RF balun inductors	2.4nH
4	C_2, C_3	RF balun capacitors	1.2pF
5	L_4	RF LC filter/matching inductor	3.9nH
6	C_4	RF matching/DC blocking capacitor	1.0pF
7	C_5	RF LC filter/matching capacitor	1.8pF
8	R_1	Resistor for internal bias current reference	510kohm
9	R_2	MS control signal filter resistor	10kohm
10	X-tal 32M	32MHz crystal unit	32MHz
11	C_6, C_7	Crystal loading capacitors	30pF
12	C_{D1}	Decoupling capacitor for ACDD_RF12V	1nF
13	C_{D2}	Decoupling capacitor for ACDD_CP12V	1uF
14	C_{D3}	Decoupling capacitor for VDD	1uF
15	C_{D4}	Decoupling capacitor for 3V supply	1uF
16	C_{D5}	Decoupling capacitor for 3V supply	1uF
17	C_8	Decoupling capacitor for 3V supply	100nF

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7

MCU SUBSYSTEM

7.1 Memory Organization

7.1.1 Program Memory

The address space of program memory is 64KB (0x0000~0xFFFF). Basically, the lower 63KB of program memory is implemented by non-volatile memory. The upper 1KB from 0xFC00 to 0xFFFF is implemented by both non-volatile memory and ROM. As shown in [Figure 4] below, there are two types of memory in the same address space. The address space, which is implemented by non-volatile memory, is used as general program memory and the address space, which is implemented by ROM, is used for ISP (In-System Programming).

As shown in (a) of [Figure 4] below, when Power is turned on, the upper 1KB of program memory is mapped to ROM under the ISP mode. As shown in (b) of [Figure 4], this program area (1KB) is used as non-volatile program memory under the normal mode. The ROM area can't be accessed under the normal mode.

ISP MODE(ROM is always active)   NORMAL MODE
                                                   (ROM is always inactive)

(a)   (b)
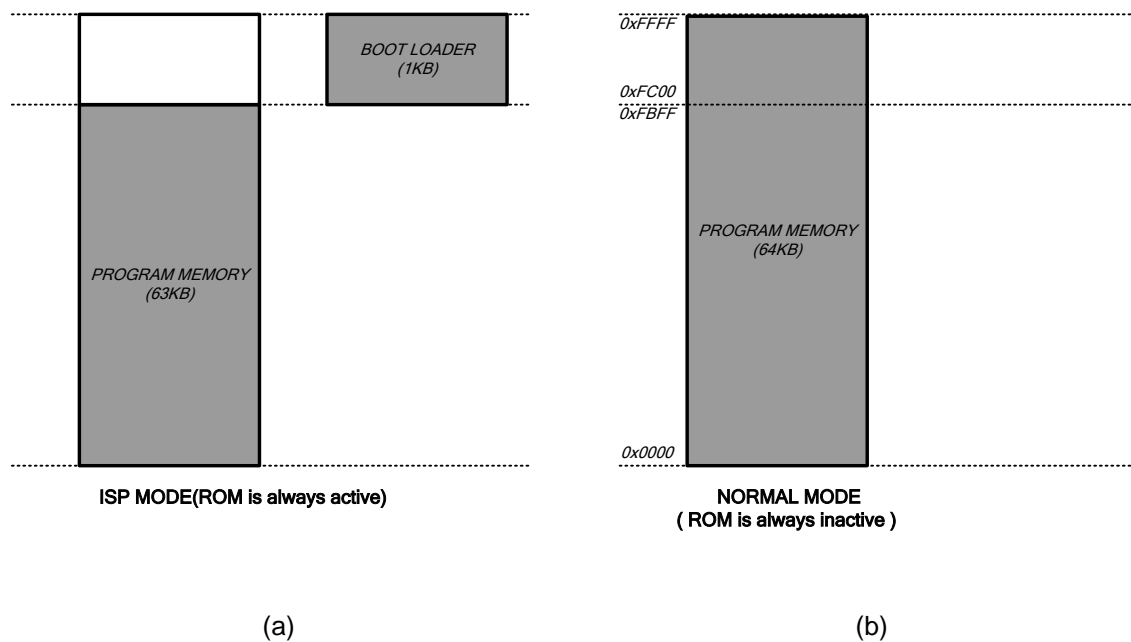
Figure 4. Address Map of Program Memory

7.1.2 Data Memory

MG2475 reserves 64 KB data memory address space. This address space can be accessed by 8051 MOVX instruction. [Figure 5] shows the address map of MG2475 data memory.
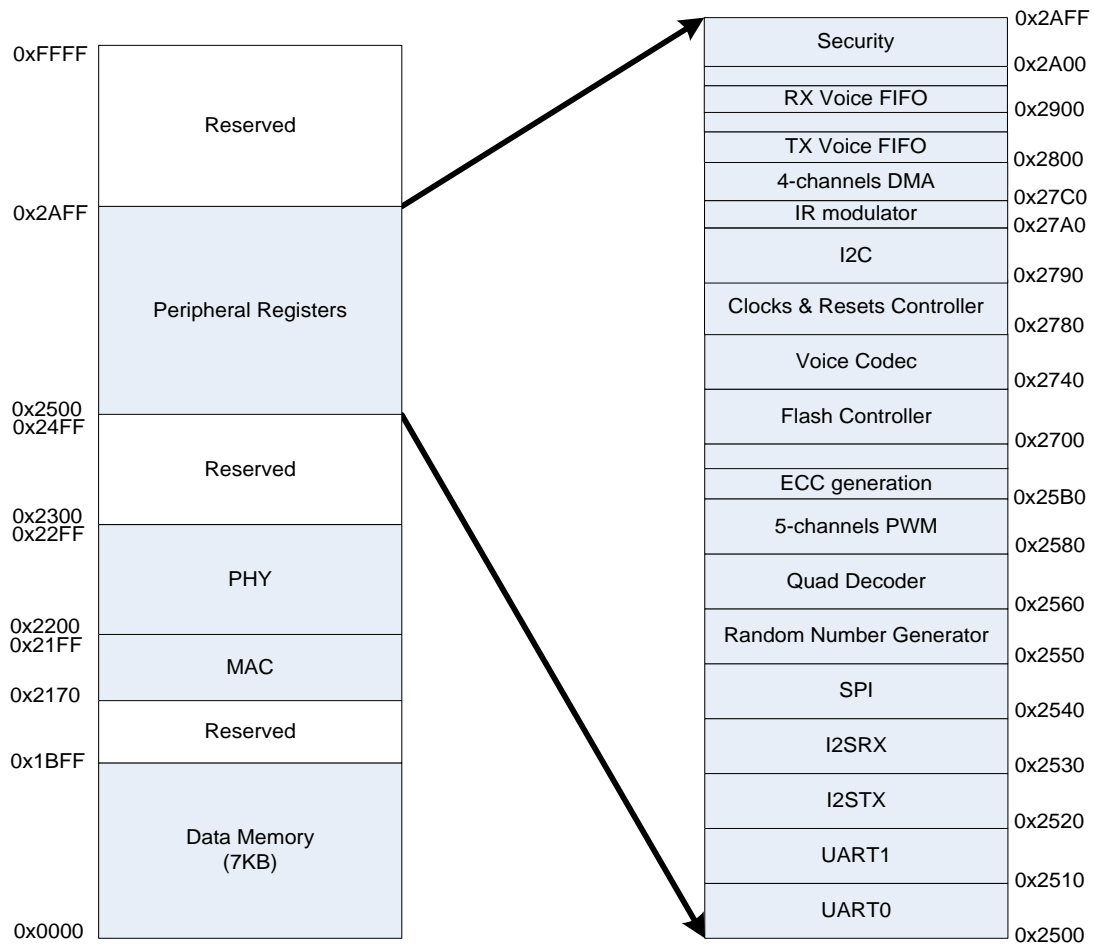
Figure 5. Address Map of Data Memory

The data memory used in the application programs resides in the address range 0x0000-0x1BFF. The registers and memory used in the MAC block reside in the address range 0x2170-0x21FF. The registers to control or report the status of PHY block reside in the address range 0x2200-0x22FF.

Registers related to the numerous peripheral functions of the MG2475 reside in the address range of 0x2500-0x2AFF.

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7.1.3 General Purpose Registers

[Figure 6] describes the address map of the General Purpose Registers (GPRs). GPRs can be addressed either directly or indirectly. As shown in the lower address space of [Figure 6], a bank consists of 8 registers.

The address space above the bank area is the bit addressable area, which is used as a flag by software or by a bit operation. The address space above the bit addressable area includes registers used as a general purpose of a byte unit. For more detailed information, refer to the paragraphs following [Figure 6] below.

0xFF		
	SFRs Area	
0x80		
0x7F		
	Data RAM Area	
0x30		
0x2F		
	Bit Addressable Area	GPRs
0x20		
0x18	Bank3	
0x10	Bank2	
0x08	Bank1	
0x00	Bank0	
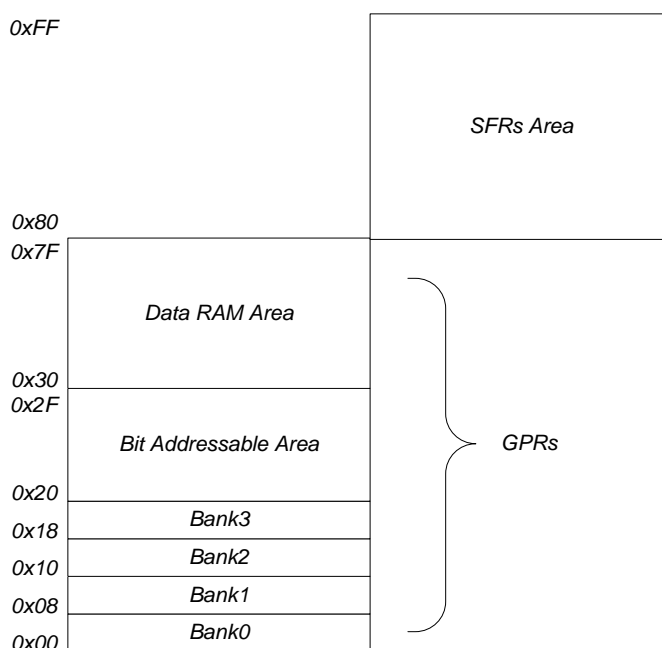
Figure 6. GPRs Address Map

Register Bank 0-3: It is located from 0x00 to 0x1F (32 bytes). One bank consists of each 8 registers out of 32 registers. Therefore, there are total 4 banks. Each bank should be selected by software as referring the RS field in PSW(Program Status Word) register. The bank (8 registers) selected by RS value can be accessed by a name (R0-R7) by software. After reset, the default value is set to bank0.

Bit Addressable Area: The address is assigned to each bit of 16 bytes (0x20~0x2F) and registers, which is the multiple of 8, in SFR. Each bit can be accessed by the address which is assigned to these bits. 128 bits (16 bytes, 0x20~0x2F) can be accessed by direct addressing for each bit (0x00~0x7F address is assigned) and by a byte unit as using the address from 0x20~0x2F.

Data RAM Area: A user can use the data memory area (0x30~0x7F) as a general purpose.

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7.1.4 Special Function Registers (SFR)

The special function registers (SFRs) reside in their associated peripherals or in the 8051 core.

The SFR include the status or control register of the I/O ports, the timer registers, the stack pointers and so on. [Table 4] shows the address to all SFRs in MG2475. Unoccupied locations in the SFR space (the blank locations in Table 4) are unimplemented, i.e., no register exists.

If an instruction attempts to write to an unimplemented SFR location, the instruction executes, but nothing is actually written. If an unimplemented SFR location is read, it returns a zero value.

 All SFRs are accessed by a byte unit. However, when SFR address is multiple of 8, it can be accessed by a bit unit.   Note that all SFR registers in MG2475 is retained in deep sleep mode, such as PM3.

Table 4. SFR (Special Function Register) Memory Map

SFR Address	8 bytes							SFR Address
80	P0	SP	DPL	DPH			PCON	87
88	TCON	TMOD	TL0	TL1	TH0	TH1		8F
90	P1	EXIF1	PERI_CLK_STP3					97
98	PERI_CLK_STP0	PERI_CLK_STP1	PERI_CLK_STP2					9F
A0	P2		AUXR1					A7
A8	IE	T23CON	TH2	TH3	TL2	TL3		AF
B0	P3	P0OEN	P1OEN		P3OEN			B7
B8	IP	P0_IE	P1_IE		P3_IE			BF
C0	WCON	P0_DS0	P1_DS0		P3_DS0			C7
C8								CF
D0	PSW		WDTCON					D7
D8	EXIF2	P0_DS1	P1_DS1		P3_DS1			DF
E0	ACC	P0_DS2	P1_DS2		P3_DS2			E7
E8	EIE1	EIE2	P0_POL	P0_EDGE	P0_IRQ_EN	P0_IRQ_STS		EF
F0	B		P1_POL	P1_EDGE	P1_IRQ_EN	P1_IRQ_STS		F7
F8	EIP1	EIP2	P3_POL	P3_EDGE	P3_IRQ_EN	P3_IRQ_STS		FF

The following section describes each SFR included in the MG2475.

> **NOTE:** This table shows register bit symbol conventions.
>
> | Symbol | Access Mode |
> |---|---|
> | R/W | Read/Write |
> | RO | Read Only |
> | WO | Write Only |

- WCON (WRITE CONTROL REGISTER, 0xC0)

This register can control the upper 1KB of program memory and miscellaneous setting.

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved	RO	0
6	ISPMODE	ISP Mode Indication. When MS pin is '1', this field is set to 1 by hardware. It notifies the MCU whether or not ISP MODE is.	RO	Unknown
5:3		Reserved	RO	0
2	FlashLowPower	If this bit is set to 1, the low-power mode is enabled at flash memory access by CPU	R/W	0
1		Reserved	RO	1
0		Reserved	RO	0

- ACCUMULATOR (A or ACC, 0xE0)

This register is marked as A or ACC and it is related to all the operations.

Bit	Name	Descriptions	R/W	Reset Value
7:0	A	Accumulator	R/W	0x00

- B REGISTER (B, 0xF0)

This register is used for a special purpose when multiplication and division are processed. For other instructions, it can be used as a general-purpose register. After multiplication is processed, this register contains the MSB data and 'A register' contains LSB data for the multiplication result. In division operation, this register stores the value before division (dividend) and the remainder after division. At this time, before division, the divisor should be stored in 'A register' and result value (quotient) is stored in it after division.

Bit	Name	Descriptions	R/W	Reset Value
7:0	B	B register. Used in MUL/DIV instructions.	R/W	0x00

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- PROGRAM STATUS WORD (PSW, 0xD0)

This register stores the status of the program. The explanation of each bit is as follows.

Bit	Name	Descriptions	RW	Reset Value
7	CY	Carry flag	R/W	0
6	AC	Auxiliary carry flag for BCD operations	R/W	0
5	F0	Flag0. User-defined	R/W	0
4:3	RS	Register bank select. 0: Bank0 1: Bank1 2: Bank2 3: Bank3	R/W	0
2	OV	Overflow flag	R/W	0
1	F1	Flag1. User-defined	R/W	0
0	P	Parity flag. Set to 1 when the value in accumulator has odd number of '1' bits.	R/W	0

- STACK POINTER (SP, 0x81)

When PUSH and CALL instructions are executed, some data (like the parameters by function call) are stored in stack to inform the values. In 8051 MCU, the data memory area which can be used for a general purpose (0x08~0x7F) is used as a stack area.

This register value is increased before the data is stored and decreased after the data is read when the POP and RET instructions are executed. The default value is 0x07.

Bit	Name	Descriptions	RW	Reset Value
7:0	SP	Stack Pointer	R/W	0x07

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- DATA POINTER (DPH : 0x83, DPL : 0x82)

Data pointer consists of a high byte (DPH) and a low byte (DPL) to support 16-bit address. It can be accessed by 16-bit register or by two 8-bit registers respectively.

Bit	Name	Descriptions	RW	Reset Value
7:0	DPH	Data pointer, high byte	R/W	0x00

Bit	Name	Descriptions	RW	Reset Value
7:0	DPL	Data pointer, low byte	R/W	0x00

- AUXILIARY CONTROL REGISTER (AUXR1, 0xA2)

This register is used to implement the Dual DPTR functions. Physically, The DPTR consists of DPTR0 and DPTR1. However, DPTR0 and DPTR1 can be accessed depending on the DPS value of AUXR1 respectively. In other words, they cannot be accessed at the same time.

Bit	Name	Descriptions	RW	Reset Value
7:1		Reserved	RO	0
0	DPS	Dual DPTR Select: Used to select either DPTR0 or DPTR1. When DPS is '0', DPTR0 is selected. When DPS is '1', DPTR1 is selected.	R/W	0

- GPIO SFRs

Please refer to Sec 8.2. GPIO for more details.

Register	Address	Description
P0	0x80	PORT-0 data register
P1	0x90	PORT-1 data register
P2	0xA0	PORT-2 data register for PDATA area access in 8051 architecture.
P3	0xB0	PORT-3 data register
P0OEN	0xB1	PORT-0 direction register
P1OEN	0xB2	PORT-1 direction register
P3OEN	0xB4	PORT-3 direction register
P0_IE	0xB9	PORT-0 input enable register
P1_IE	0xBA	PORT-1 input enable register
P3_IE	0xBC	PORT-3 input enable register
P0_DS0	0xC1	PORT-0 drive strength selection register-0

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P1_DS0	0xC2	PORT-1drive strength selection register-0
P3_DS0	0xC4	PORT-3 drive strength selection register-0
P0_DS1	0xD9	PORT-0 drive strength selection register-1
P1_DS1	0xDA	PORT-1drive strength selection register-1
P3_DS1	0xDC	PORT-3 drive strength selection register-1
P0_DS2	0xE1	PORT-0 drive strength selection register-2
P1_DS2	0xE2	PORT-1drive strength selection register-2
P3_DS2	0xE4	PORT-3 drive strength selection register-2
P0_POL	0xEA	P0[7:0] interrupt polarity selection register
P0_EDGE	0xEB	P0[7:0] interrupt edge selection register
P0_IRQ_EN	0xEC	P0[7:0] interrupt enable register
P0_IRQ_STS	0xED	P0[7:0] interrupt flags register
P1_POL	0xF2	P1[7:0] interrupt polarity selection register
P1_EDGE	0xF3	P1[7:0] interrupt edge selection register
P1_IRQ_EN	0xF4	P1[7:0] interrupt enable register
P1_IRQ_STS	0xF5	P1[7:0] interrupt flags register
P3_POL	0xFA	P3[7:0] interrupt polarity selection register
P3_EDGE	0xFB	P3[7:0] interrupt edge selection register
P3_IRQ_EN	0xFC	P3[7:0] interrupt enable register
P3_IRQ_STS	0xFD	P3[7:0] interrupt flags register

- WDT (WATCHDOG TIMER) SFR

Please refer to Sec 8.6. WDT for the more details.

Register	Address	Description
WDTCON	0xD2	Watchdog timer control register

- Timer 0/1 SFRs

Please refer to Sec 8.3. timer 0/1 for the more details.

Register	Address	Description
TCON	0x88	Timer/Counter 0 & 1 control
TMOD	0x89	Timer/Counter 0 & 1 mode control
TL0	0x8A	Timer/Counter 0 low byte
TH0	0x8C	Timer/Counter 0 high byte
TL1	0x8B	Timer/Counter 1 low byte
TH1	0x8D	Timer/Counter 1 high byte

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- Timer 2/3 SFRs

Please refer to Sec 8.4 timer 2/3 for the more details.

Register	Address	Description
T23CON	0xA9	Timer 2 & 3 control
TL2	0xAC	Timer2 low byte
TH2	0xAA	Timer2 high byte
TL3	0xAD	Timer3 low byte
TH3	0xAB	Timer3 high byte

- 8051 MCU Clock Control SFRs

Please refer to Sec 7.2. clock for the more details.

Register	Address	Description
PERI_CLK_STP0	0x98	MCU peripherals clock on/off control 0
PERI_CLK_STP1	0x99	MCU peripherals clock on/off control 1
PERI_CLK_STP2	0x9A	MCU peripherals clock on/off control 2
PERI_CLK_STP3	0x92	MCU peripherals clock on/off control 3

- Power Control SFR

Please refer to Sec 8.15. power management for the more details.

Register	Address	Description
PCON	0x87	Power control register

Bit	Name	Descriptions	RW	Reset Value
7:2		Reserved	RO	0
1	PD	Power-down mode bit 1: start power-down mode 0: clear by hardware when an enabled external interrupt or a reset occurs.	R/W	0
0	IDLE	8051 Idle mode bit 1: Start the 8051 idle mode (The clock to 8051 is only off-state) 0: Cleared by hardware when an enabled peripherals interrupt or a reset occurs.	R/W	0

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- 8051 MCU Interrupt SFRs

Please refer to Sec 7.4. interrupts for the more details.

Register	Address	Description
IE	0xA8	Interrupt Enable
EIE1	0xE8	Extended Interrupt Enable 1
EIE2	0xE9	Extended Interrupt Enable 2
IP	0xB8	Interrupt Priority
EIP1	0xF8	Extended Interrupt Priority 1
EIP2	0xF9	Extended Interrupt Priority 2
EXIF2	0xD8	Extended Interrupt Flag 2
EXIF1	0x91	Extended Interrupt Flag 1

7.2 Clock

The MG2475 supports an advanced and flexible clock selection function to reduce the power consumption depending on the target applications. The clock system overview of MG2475 is shown in the [Figure 7].
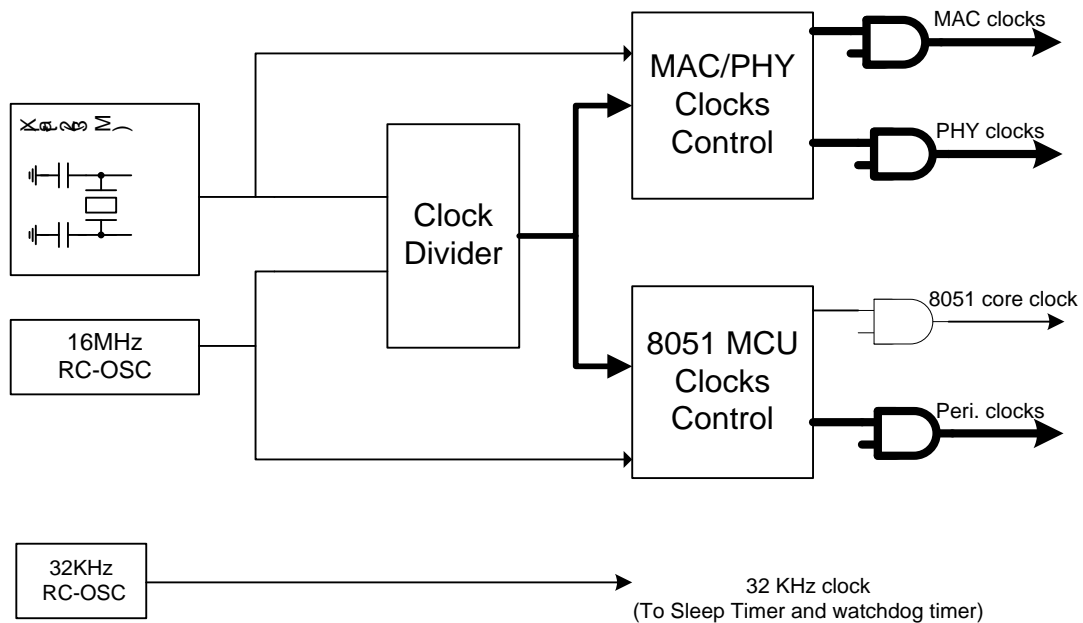
Figure 7. Clock System Overview

Two high speed oscillators are included in the MG2475. One is 32 MHz crystal oscillator and the other is 16MHz RC oscillator (HSRCOSC). The high speed 32MHz crystal oscillator startup-time may be too long for the power critical applications. For example, the wake-up time from the power down mode is longer than the RC oscillator. So, the MG2475 can run on the 16MHz RC oscillator until the 32MHz crystal oscillator is stable.

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7.2.1 8051 MCU Reference Clock Control

The 8 MHz clock source from 32MHz crystal and a high-speed RC oscillator can be used to drive the internal 8051 MCU subsystem clock in MG2475. The default clock frequency of MG2475 is 8 MHz. When selecting 8051 MCU subsystem clock, the SELCLK register (0x2784) should be set as follows.

• Clock Selection Register (SELCLK, 0x2784**[RETENTION]**)

Bit	Name	Descriptions		RW	Reset Value
7		Reserved			
6	SEL_MCU_CLK[2]			R/W	001
5	SEL_MCU_CLK[1]	Value	MCU subsystem clock frequency		
4	SEL_MCU_CLK[0]	000	16 MHz operation		
		001	8 MHz operation		
		010	4 MHz operation		
		011	2 MHz operation		
		100	1 MHz operation		
		101	32kHz operation		
		Others	Clock Off		
3		Reserved			
2		Reserved			
1	SEL_DCC_MODE	16MHz clock selection bit 1: Manual clock mode, DCC clock is selected by SEK_CLK_DCC bit. 0: Auto mode, DCC clock is seleted by SEL_CPS bit.		R/W	0
0	SEL_CLK_DCC	DCC clock selection only when SEL_DCC_MODE bit is 0. 1: 16MHz 0: 32MHz		R/W	0

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7.2.2 MCU Peripherals Clock Control

The operating clock of 8051 MCU peripherals can be enabled or disabled by some SFR registers write operation. For details, please refer to the SFRs description below.

- Peripheral Clock Stop 0(PERI_CLK_STP0, 0x98)

Bit	Name	Descriptions	R/W	Reset Value
7	SPI_ON	This bit is for enabling or disabling the operating clock of SPI. 0 : clock is off 1 : clock is on	R/W	0
6	UART1_ON	This bit is for enabling or disabling the operating clock of UART1. 0 : clock is off 1 : clock is on	R/W	1
5	UART0_ON	This bit is for enabling or disabling the operating clock of UART0. 0 : clock is off 1 : clock is on	R/W	1
4	GPIO_ON	This bit is for enabling or disabling the operating clock of GPIO. 0 : clock is off 1 : clock is on	R/W	1
3	TIMER3_ON	This bit is for enabling or disabling the operating clock of TIMER 3 0 : clock is off 1 : clock is on	R/W	0
2	TIMER2_ON	This bit is for enabling or disabling the operating clock of TIMER 2. 0 : clock is off 1 : clock is on	R/W	0
1	TIMER1_ON	This bit is for enabling or disabling the operating clock of TIMER 1. 0 : clock is off 1 : clock is on	R/W	0
0	TIMER0_ON	This bit is for enabling or disabling the operating clock of TIMER 0. 0 : clock is off 1 : clock is on	R/W	0

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- Peripheral Clock Stop 1(PERI_CLK_STP1, 0x99)

Bit	Name	Descriptions	R/W	Reset Value
7	I2C_ON	This bit is for enabling or disabling the operating clock of I2C controller. 0 : clock is off 1 : clock is on	R/W	0
6	IRTX_ON	This bit is for enabling or disabling the operating clock of IR TX modulator. 0 : clock is off 1 : clock is on	R/W	0
5	FLASHC_ON	This bit is for enabling or disabling the operating clock of flash controller. 0 : clock is off 1 : clock is on	R/W	0
4	VOICE_ON	This bit is for enabling or disabling the operating clock of voice block. 0 : clock is off 1 : clock is on	R/W	0
3	I2SRX_ON	This bit is for enabling or disabling the operating clock of I2S RX. 0 : clock is off 1 : clock is on	R/W	0
2	I2STX_ON	This bit is for enabling or disabling the operating clock of I2S TX. 0 : clock is off 1 : clock is on	R/W	0
1	QUAD_ON	This bit is for enabling or disabling the operating clock of quadrature signal decoder. 0 : clock is off 1 : clock is on	R/W	0
0	RNG_ON	This bit is for enabling or disabling the operating clock of random number generator. 0 : clock is off 1 : clock is on	R/W	0

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- Peripheral Clock Stop 2(PERI_CLK_STP2, 0x9A)

Bit	Name	Descriptions	R/W	Reset Value
7	PWM_CH4_ON	This bit is for enabling or disabling the operating clock of PWM channel 4. 0 : clock is off 1 : clock is on	R/W	0
6	PWM_CH3_ON	This bit is for enabling or disabling the operating clock of PWM channel 3. 0 : clock is off 1 : clock is on	R/W	0
5	PWM_CH2_ON	This bit is for enabling or disabling the operating clock of PWM channel 2. 0 : clock is off 1 : clock is on	R/W	0
4	PWM_CH1_ON	This bit is for enabling or disabling the operating clock of PWM channel 1. 0 : clock is off 1 : clock is on	R/W	0
3	PWM_CH0_ON	This bit is for enabling or disabling the operating clock of PWM channel 0. 0 : clock is off 1 : clock is on	R/W	0
2:0		Reserved	RO	0x7

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- Peripheral Clock Stop 3(PERI_CLK_STP3, 0x92)

Bit	Name	Descriptions	R/W	Reset Value
7:6		Reserved	RO	0
5	SEC_ON	This bit is for enabling or disabling the operating clock of security engine for IEEE.802.15.4. 0 : clock is off 1 : clock is on		
4	DMAC_ON	This bit is for enabling or disabling the operating clock of DMA controller. 0 : clock is off 1 : clock is on	R/W	0
3	P3_INTCTL_ON	This bit is for enabling or disabling the operating clock of the interrupt controller for the external P3[1:0]/P3[7:4] pins. 0 : clock is off 1 : clock is on	R/W	0
2	P1_INTCTL_ON	This bit is for enabling or disabling the operating clock of the interrupt controller for the external P1[1:0]/P1[4:3]/P1[7:6] pins . 0 : clock is off 1 : clock is on	R/W	0
1	P0_INTCTL_ON	This bit is for enabling or disabling the operating clock of the interrupt controller for the external P0[7:0] pins . 0 : clock is off 1 : clock is on	R/W	0
0	WDT_ON	This bit is for enabling or disabling the operating clock of Watchdog timer block. 0 : clock is off 1 : clock is on	R/W	1

7.2.3 MAC/PHY Clocks Control

Please refer to the clock & reset in Sec 8.1 peripherals chapter for details.

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7.3 Resets

The MG2475 has four types of reset sources.

- The external pin RESETB is inputted to low during more than 62.5 us

- Internal POR (Power-On-Reset) condition

- Internal BOD (Brown Out Detector) reset condition

- Watchdog timer reset condition

The initial conditions after a reset are as follows;

- I/O pins are configured as inputs with pull-up
- CPU program counter is loaded with 0x0000 and program execution starts at this address
- All peripheral registers are initialized to their reset values.
- Watchdog timer is enabled

The resets of MAC/PHY blocks are controlled by the separate reset controller block in the MG2475. They can be reset by S/W control besides four sources for system reset. For more detailed information, please refer to the register description in the clock & reset controller (Sec 8.1).

7.3.1 POR (Power-On-Reset)

There are two digital powers in the MG2475. One is Always-On power and the other is On-Off power. There are two detection circuits for power-on-reset as follows:

- POR LP monitors the always-on digital supply voltage.

- POR NML monitors the on-off digital supply voltage whenever MG2475 wake up from PM2/PM3 power down mode to normal mode

The POR reset signal is released after a certain delay time if the supply voltage rises above a stable threshold level. Please refer to [Table 5] and [Table 6] for POR delay time.

Table 5. POR LP delay Time

Parameter	MIN	TYP	MAX	unit
	515.8	537.9	928.7	us

Table 6. POR NML delay time

Parameter	MIN	TYP	MAX	unit
POR_NML_DLY = H	124	142	157	us
POR_NML_DLY = L	61	69	78	us

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7.3.2 BOD (Brown-Out Detector)

The BOD of MG2475 monitors the 3V power supply voltage and drive a reset signal whenever the 3V voltage falls below the threshold level (V_{thd}). When 3V power supply voltage is higher than the threshold level (V_{thu}), the reset signal will be released.

Table 7. BOD characteristics

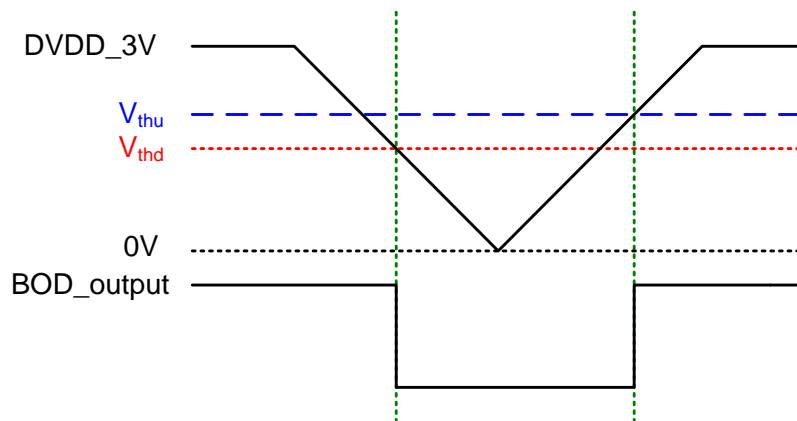|	MIN	TYP	MAX	unit
Operating Voltage	1.5		3.6	V
Operating Temperature	-40		85	℃
Detection Voltage Level (V_{thd})	1.62	1.83	2.00	V
Detection Voltage Level (V_{thu})	1.88	2.12	2.32	V
Operating Current		1.20		uA

Figure 8. BOD operating diagram

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7.4 Interrupts

The 8051 CPU of MG2475 employs a program interrupt method similar to the one of other CPU. When the interrupt event occurs, the 8051 CPU core jumps to the location which is called as an interrupt vector address and the interrupt service routine at the corresponding vector address is executed. When the interrupt subroutine completes, execution resumes at the point where the interrupt occurred. Interrupts can occur as a result of internal activity (e.g. timer0 overflow) or at the initiation of an external device (external interrupt pin). All the interrupts of MG2475 can be enabled or disabled dynamically by a user.
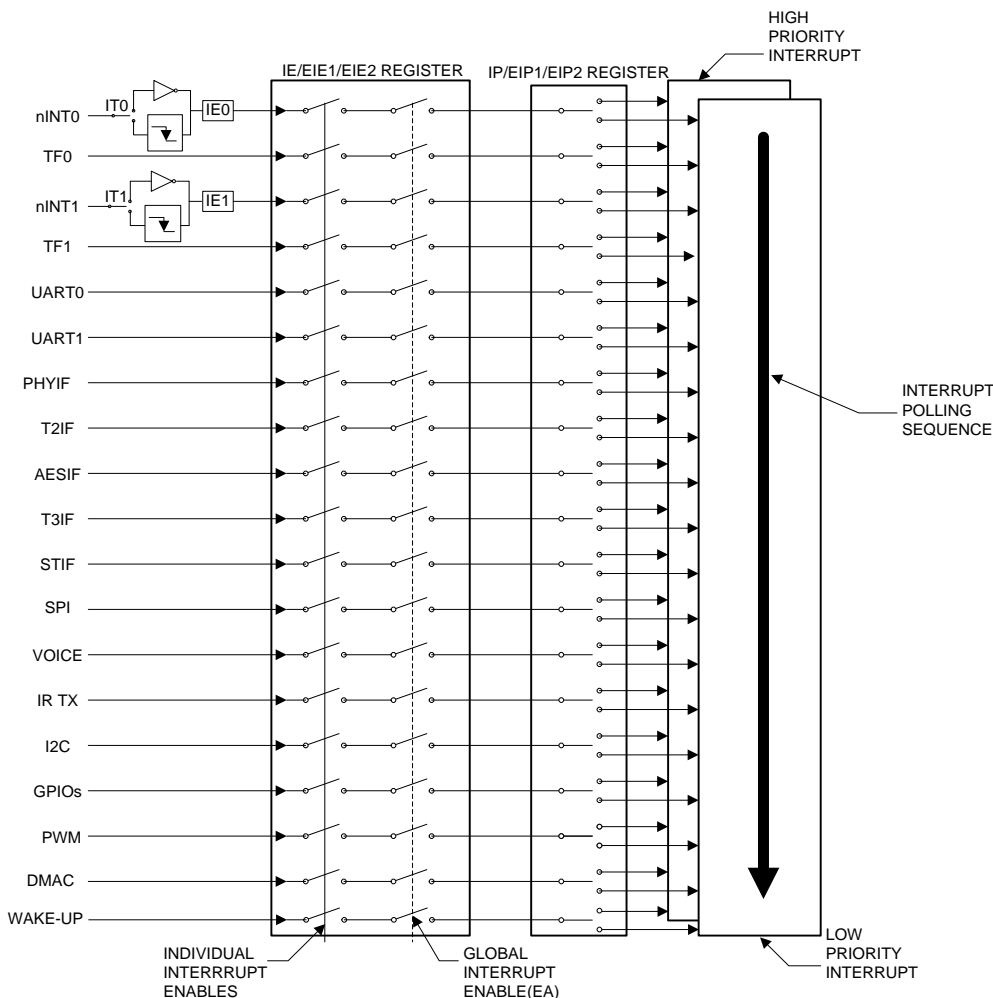
Figure 9. Interrupts Overview of MG2475

MG2475 has 19 interrupt sources. [Table 8] describes the detailed information for each of the interrupt sources. The 'Interrupt Address' indicates the address where the interrupt service routine is located. The 'Interrupt Flag' is the bit that notifies the MCU that the corresponding interrupt has occurred. 'Interrupt Enable' is the bit which decides whether each interrupt has been enabled. 'Interrupt Priority' is the bit which decides the priority of the interrupt. 'Interrupt Number' is the interrupt priority fixed by the hardware. That is, when two or more interrupts having the same 'Interrupt Priority' value, occur simultaneously, the lower 'Interrupt Number' is processed first.

Table 8. Interrupt Descriptions

Interrupt Number	Interrupt Type	Interrupt Address	Interrupt Flag	Interrupt Enable	Interrupt Priority
0	External Interrupt0	0x0003	TCON.IE0 (TCON[1])	IE.EX0 (IE[0])	IP[0]
1	Timer0 Interrupt	0x000B	TCON.TF0 (TCON[5])	IE.ET0 (IE[1])	IP[1]
2	External Interrupt1	0x0013	TCON.IE1 (TCON[3])	IE.EX1 (IE[2])	IP[2]
3	Timer1 Interrupt	0x001B	TCON.TF1 (TCON[7])	IE.ET1 (IE[3])	IP[3]
4	UART0 Interrupt	0x0023	Refer to Note1	IE.ES0 (IE[4])	IP[4]
5	IR TX Interrupt	0x002B	Refer to Note2	EIE2[0]	EIP2[0]
6	I2C Interrupt	0x0033	Refer to Note3	EIE2[1]	EIP2[1]
7	UART1 Interrupt	0x003B	Refer to Note1	IE.ES1(IE[6])	IP[6]
8	PHY Interrupt	0x0043	Refer to Note4	EIE1.PHYIE(EIE1[0])	EIP1[0]
9	Timer2 Interrupt	0x004B	EXIF1.T2IF(EXIF1[5])	EIE1.T2IE(EIE1[1])	EIP1[1]
10	AES Done Interrupt	0x0053	EXIF1.AESIF(EXIF1[6])	EIE1.AESIE(EIE1[2])	EIP1[2]
11	Timer3 Interrupt	0x005B	EXIF1.T3IF(EXIF1[7])	EIE1.T3IE(EIE1[3])	EIP1[3]
12	Sleep-Timer time-out Interrupt	0x0063	EXIF2.STIF(EXIF2[1])	EIE1.STIE(EIE1[4])	EIP1[4]
13	SPI Interrupt	0x006B	Refer to Note5	EIE1.SPIIE(EIE1[5])	EIP1[5]
14	Voice Interrupt	0x0073	Refer to Note6	EIE1.VOICEIE (EIE1[6])	EIP1[6]
15	Wake-up Interrupt	0x007B	EXIF2.WUIF(EXIF2[0])	EIE1.WUIE(EIE1[7])	EIP1[7]
16	GPIO Interrupt	0x0083	Refer to Note7	EIE2[2]	EIP2[2]
17	PWM Interrupt	0x008B	Refer to Note8	EIE2[3]	EIP2[3]
18	General DMA Interrupt	0x0093	Refer to Note9	EIE2[4]	EIP2[4]

NOTE: 1.In case of a UART Interrupt, bit[0] of the IIR register(0x2502,0x2512) in the UART block is used as a flag. Also, the Tx, Rx, Timeout, Line Status and Modem Status interrupts can be distinguished by bit[3:1] value. For more detailed information, refer to the UART0/1 description in Sec 8.7.

NOTE: 2.In case of an IR TX interrupt, please refer to the IR Modulator section (*8.10*)

NOTE: 3.In case of an I2C interrupt, please refer to the *I2C section (8.9)*

NOTE: 4.In case of an PHY interrupt, please refer to the section *(9.2.1)* of PHY chapter.

NOTE: 5.In case of an SPI interrupt, there is another interrupt enable bit in the SPI register besides EIE.SPIIE. In order to enable SPI interrupt, both SPIE in SPCR (0x2540) register and EIE.SPIIE should be set to '1'. And, SPIF in SPSR (0x2541) register acts as an interrupt flag.

NOTE: 6.In case of a Voice interrupt, there are interrupt enable register and interrupt flag register in voice block. The interrupt enable register are VTFINTENA (0x2770), VRFINTENA (0x2771) and VDMINTENA (0x2772). There are 24 interrupt sources. When both an interrupt enable signal and an interrupt flag signal are set to '1,' Voice interrupt is enabled.

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NOTE: 7. In case of a GPIO interrupt, please refer to the GPIO section (*8.2*).

NOTE: 8. In case of a PWM interrupt, please refer to the PWM section (*8.5*).

NOTE: 9. In case of a DMA interrupt, please refer to the DMA section (8.15).

7.4.1 Interrupt Sources

The MG2475 has the 19 hardware interrupt sources. They include two external interrupts (nINT0/P3[2] & nINT1/P3[3]), four timers interrupt timers 0/1/2/3, two UART interrupts and eleven additional interrupt. Each interrupt has an interrupt request flag and for some interrupts, hardware clears the request flag when it grants an interrupt. The followings are interrupt sources in the MG2475.

- Two external interrupts(IE0 and IE1 in TCON register)
- (Theses can be used as wakeup sources under the power down mode.)

- PHY interrupt
- AES done interrupt
- Sleep timer time-out interrupt
- MCU peripherals interrupt
- Timer 0&1 (TF0 and TF1 in TCON register)
- Timer 2&3 (T2IF and T3IF in EXIF1 register)
- UART0 & UART1
- SPI
- Voice
- 5-channels PWM
- General DMA done interrupt
- IR modulator
- I2C
- All GPIO pins except P3[3:2] pins under normal mode
- Wake-up interrupt from the power-down mode

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- EXTENDED INTERRUPT FLAG REGISTER 1 (EXIF1, 0x91)

This register stores the interrupt state corresponding to each bit. When the interrupt corresponding to a bit is triggered, the flag is set to '1'.

Bit	Name	Descriptions	R/W	Reset Value
7	T3IF	Timer3 Interrupt Flag. 0: No interrupt 1: Interrupt pending *Note: To clear the interrupt flag, The 1 must be written into this bit.	R/W	0
6	AESIF	AES Interrupt Flag. 0: No interrupt 1: Interrupt pending *Note: To clear the interrupt flag, The 1 must be written into this bit	R/W	0
5	T2IF	Timer2 Interrupt Flag. 0: No interrupt 1: Interrupt pending *Note: To clear the interrupt flag, The 1 must be written into this bit.	R/W	0
4:0		Reserved bits	RO	0

- EXTENDED INTERRUPT FLAG REGISTER 2 (EXIF2, 0xD8)

Bit	Name	Descriptions	R/W	Reset Value
7:2		Reserved	RO	0
1	STIF	Sleep timer time-out interrupt flag in normal mode. 0: No interrupt 1: Interrupt pending *Note: To clear the interrupt flag, 1 must be written into this bit.	R/W	0
0	WUIF	Power-down wake-up interrupt flag 0: No interrupt 1: Interrupt pending *Note: To clear the interrupt flag, 1 must be written into this bit.	R/W	0

7.4.2 Interrupt Enable

The EA bit in the IE register is the global interrupt enable signal for all interrupts. In addition, each interrupt is masked by each interrupt enable bit. Therefore, in order to use an interrupt, both EA and the specific interrupt enable bit should be set to '1'. When the bit for each interrupt is '0', that interrupt is disabled. When the bit for each interrupt is '1', that interrupt is enabled.

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- Interrupt Enable Register (IE, 0xA8)

Bit	Name	Descriptions	R/W	Reset Value
7	EA	Global interrupt enable 0: No interrupt will be acknowledged. 1: Each interrupt source is individually enabled or disabled by setting its corresponding enable bit.	R/W	0
6	ES1	UART1 interrupt enable 0: interrupt disabled 1: interrupt enabled (EA bit should be set to '1')	R/W	0
5		Reserved		0
4	ES0	UART0 interrupt enable 0: interrupt disabled 1: interrupt enabled (EA bit should be set to '1')	R/W	0
3	ET1	Timer1 interrupt enable 0: interrupt disabled 1: interrupt enabled (EA bit should be set to '1')	R/W	0
2	EX1	External interrupt1 enable 0: interrupt disabled 1: interrupt enabled (EA bit should be set to '1')	R/W	0
1	ET0	Timer0 interrupt enable 0: interrupt disabled 1: interrupt enabled (EA bit should be set to '1')	R/W	0
0	EX0	External interrupt0 enable 0: interrupt disabled 1: interrupt enabled (EA bit should be set to '1')	R/W	0

- Extended Interrupt Enable Register 1(EIE1, 0xE8)

Bit	Name	Descriptions	R/W	Reset Value
7	WUIE	Wake-up from the power-down mode interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
6	VOICEIE	Voice interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0

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5	SPIIE	SPI interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
4	STIE	Sleep Timer Time-out interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
3	T3IE	Timer3 interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
2	AESIE	AES Done interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
1	T2IE	Timer2 interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
0	PHYIE	PHY interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0

- Extended Interrupt Enable Register 2(EIE2, 0xE9)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved bits	RO	0
4	DMAIE	DMA interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
3	PWMIE	PWM interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
2	GPIOIE	GPIO interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
1	I2CIE	I2C interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0
0	IRTXIE	IR TX interrupt enable 0: interrupt disabled 1: interrupt enabled	R/W	0

7.4.3 Interrupt Priority

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in SFRs IP/EIP1/EIP2. A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

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- INTERRUPT PRIORITY REGISTER (IP, 0xB8)

If a bit corresponding to each interrupt is '0', the corresponding interrupt has lower priority and if a bit is '1', the corresponding interrupt has higher priority.

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved	RO	0
6	PS1	UART1 interrupt priority bit 0: assign low priority 1: assign high priority	R/W	0
5		Reserved		0
4	PS0	UART 0 interrupt priority bit 0: assign low priority 1: assign high priority	R/W	0
3	PT1	Timer1 interrupt priority bit 0: assign low priority 1: assign high priority	R/W	0
2	PX1	External interrupt1 interrupt priority bit 0: assign low priority 1: assign high priority	R/W	0
1	PT0	Timer0 interrupt priority bit 0: assign low priority 1: assign high priority	R/W	0
0	PX0	External interrupt0 interrupt priority bit 0: assign low priority 1: assign high priority	R/W	0

- EXTENDED INTERRUPT PRIORITY REGISTER 1 (EIP1, 0xF8)

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved		0
6	VOICEIP	Voice interrupt priority bit 1: Voice interrupt has higher priority. 0: Voice interrupt has lower priority.	R/W	0
5	SPIIP	SPI interrupt priority bit 1: PI interrupt has higher priority. 0: PI interrupt has lower priority.	R/W	0
4	RTCIP	Sleep Timer time-out interrupt priority bit 1: Sleep Timer interrupt has higher priority. 0: Sleep Timer interrupt has lower priority.	R/W	0
3	T3IP	Timer3 interrupt priority bit 1: Timer3 interrupt has higher priority. 0: Timer3 interrupt has lower priority.	R/W	0

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2	AESIP	AES interrupt priority bit 1: AES interrupt has higher priority. 0: AES interrupt has lower priority.	R/W	0
1	T2IP	Timer2 interrupt priority bit 1: Timer2 interrupt has higher priority. 0: Timer2 interrupt has lower priority.	R/W	0
0	PHYIP	PHY interrupt priority bit 1: PHY interrupt has higher priority. 0: PHY interrupt has lower priority.	R/W	0

- EXTENDED INTERRUPT PRIORITY REGISTER 2 (EIP2, 0xF9)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved bits		
4	DMAIP	DMA interrupt priority bit 1: DMA interrupt has higher priority. 0: DMA interrupt has lower priority.	R/W	0
3	PWMIP	PWM interrupt priority bit 1: PWM interrupt has higher priority. 0: PWM interrupt has lower priority.	R/W	0
2	GPIOIP	GPIO interrupt priority bit 1: GPIO interrupt has higher priority. 0: GPIO interrupt has lower priority.	R/W	0
1	I2CIP	I2C interrupt priority bit 1: I2C interrupt has higher priority. 0: I2C interrupt has lower priority.	R/W	0
0	IRTXIP	IR TX interrupt priority 1: IR TX interrupt has higher priority. 0: IR TX interrupt has lower priority.	R/W	0

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8 PERIPHERALS

8.1 Clock and Reset Controller

This block controls the clock on/off for the individual blocks in the MAC/PHY or RF/Analog. Also, it controls the clock output function for supplying the clock to external devices.
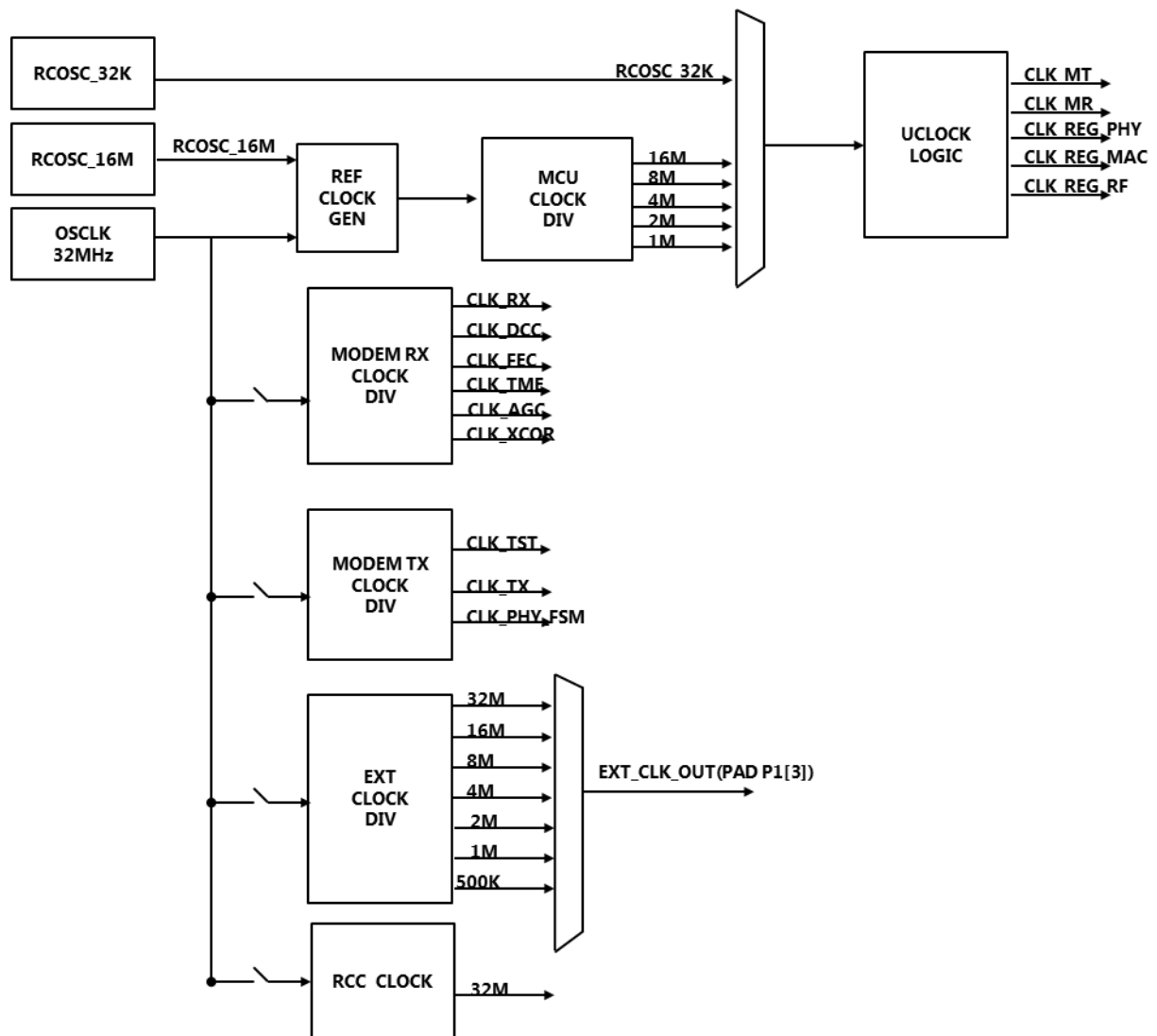

Figure 10. Clocks Structure of the MAC/PHY block

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- PHY_CLK_ON0 (PHY Clock ON Register 0, 0x2780)

This register is used to enable or disable clocks of the MAC/PHY block.

Bit	Name	Descriptions	R/W	Reset Value
7	CLKON_PHY_FSM	Modem State Machine clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
6	CLKON_TX	TX block clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
5	CLKON_RX	RX block clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
4	CLKON_DCC	DC Cancelation clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
3	CLKON_TST	CLK_TST clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
2	CLKON_MR	CLK_MR clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
1	CLKON_MT	CLK_MT clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
0	CLKAC_MT	CLK_MT clock on/off control bit at DMA transfer 0: CLK_MT is controlled by CLKON_MT bit. 1: CLK_MT is automatically off by done event at DMA transfer between data memory and Mac Tx FIFO.	R/W	0

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- PHY_CLK_ON1 (PHY Clock ON Register 1, 0x2781)

This register is used to enable or disable clocks of the MAC/PHY or RF/Analog block.

Bit	Name	Descriptions	R/W	Reset Value
7	Ext_CLKEn	Enable the external clock output function (0 : disabled, 1: enabled)	R/W	0
6	Ext_clk_sel[2]		R/W	0
5	Ext_clk_sel[1]	<table><tr><td>Value</td><td>External Clock Output Frequency</td></tr><tr><td>0</td><td>500 kHz</td></tr><tr><td>1</td><td>1MHz</td></tr><tr><td>2</td><td>2MHz</td></tr><tr><td>3</td><td>4MHz</td></tr><tr><td>4</td><td>8MHz</td></tr><tr><td>5</td><td>16MHz</td></tr><tr><td>6</td><td>32MHz</td></tr><tr><td>7</td><td>Clock Off</td></tr></table>		0
4	Ext_clk_sel[0]			0
3	CLKON_REG_PHY	CLK_REG_PHY clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
2	CLKON_REG_RF	CLK_REG_RF clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
1	CLKON_REG_MAC	CLK_REG_MAC clock on/off control bit 0: clock disabled 1: clock enabled	R/W	1
0		Reserved		

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- PHY_CLK_FE0 (PHY Clock Force Enable Register 0, 0x2782)

This register is always used to enable the clock regardless of clock enable registers setting.

Bit	Name	Descriptions	R/W	Reset Value
7	CLKFE_FEC	Rx Viterbi Decoder clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
6	CLKFE_TX	Tx clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
5	CLKFE_RX	Rx clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
4	CLKFE_DCC	DCC clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
3	CLKFE_TME	Timing Offset Estimator clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
2	CLKFE_AGC	AGC clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
1	CLKFE_XCOR	Cross Correlation Average Block clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
0		Reserved		

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- PHY_CLK_FE1 (PHY Clock Force Enable Register 1, 0x2783**[RETENTION]**)

This register is always used to enable the clock regardless of clock enable registers setting.

Bit	Name	Descriptions	R/W	Reset Value
7:6		Reserved		
5	CLKFE_PHY_FSM	Modem State Machine clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
4	CLKFE_MR	MAC Rx FIFO clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
3	CLKFE_MT	MAC Tx FIFO clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
2	CLKFE_REG_PHY	PHY registers clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
1	CLKFE_REG_RF	RF registers clock force enable bit 0: Force disabled 1: Force enabled	R/W	0
0	CLKFE_REG_MAC	MAC registers clock force enable bit 0: Force disabled 1: Force enabled	R/W	0

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8.2 General Purpose Input/Output Ports (GPIO)

The MG2475 has 22 general purpose pins which have the following key features;

- General I/O pins with selectable direction for each bit
- Programmable pull-up/down control for each bit
- Driving strength control for each bit
- External input disabling function for each bit
- Interrupt generation from all GPIO pins except P3[3:2]
  (This function is valid only under normal mode and assigned to the separate interrupt vector.)

- External interrupt capability of P3[3:2] pins
  (These pins can be used to wake up the MG2475 from power down modes.)

- Wakeup sources in power down modes
  (For more detailed description, please see to Sec 8.15. Power management)

The GPIO functions are listed in [Table 9]. [Figure 11] shows the block diagram of the GPIO.

The GPIO pins after a reset are configured as inputs with pull-up.

Table 9. PORT-0/1/3 Operation Truth Table

INPUTs					OUTPUT
OEN	I	PE	PS	SPU	PAD
0	0	x	x	x	0
0	1	x	x	x	1
1	x	0	x	x	Hi-Z
1	x	1	0	x	Pull-down
1	x	1	1	0	Pull-up
1	x	1	1	1	Strong Pull-up

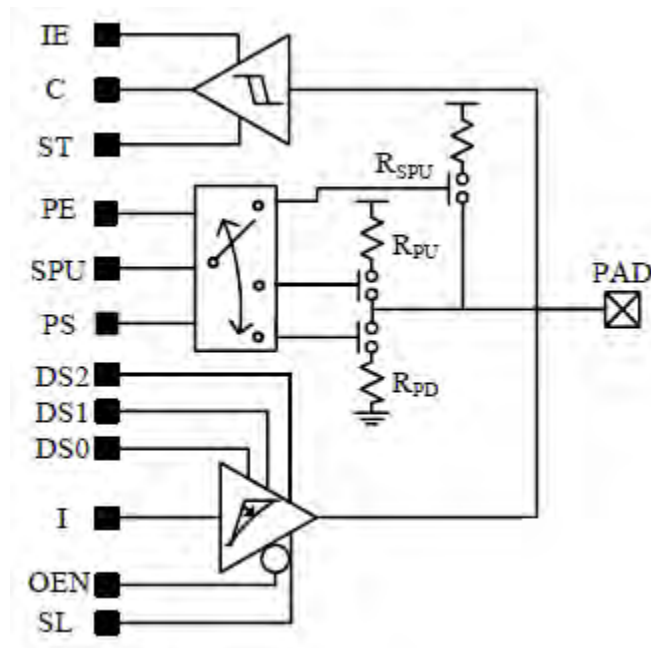| DS2	DS1	DS0	Current Spec.
0	0	0	4 mA
0	0	1	8 mA
0	1	0	12 mA
0	1	1	16 mA
1	0	0	20 mA
1	0	1	24 mA
1	1	0	32 mA
1	1	1	40 mA

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Figure 11. PORT-0/1/3 PAD Block Diagram

8.2.1 Port Data Registers (SFR area)

- PORT-3 DATA REGISTER (P3, 0xB0)

Bit	Name	Descriptions	R/W	Reset Value
7:0	P3[7:0]	This port register is used as a general purpose I/O ports. When reading the each bit of PORT-3, the current status value of the corresponding bit is returned. When writing the each bit of PORT-3, the corresponding PORT-3 bit is changed to the new value. By default, the direction of P3[7:0] is the input mode and the pull-up enable bit is the active-state. For details of pull-up/pull-down controls of P3[7:0], Please see to the Power Management section(8.15).	R/W	Unknown

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- PORT-1 DATA REGISTER (P1, 0x90)

Bit	Name	Descriptions	R/W	Reset Value
7:0	P1[7:0]	This port register is used as a general purpose I/O ports. When reading the each bit of PORT-1, the current status value of the corresponding bit is returned. When writing the each bit of PORT-1, the corresponding PORT-1 bit is changed to the new value. By default, the direction of P1[7:0] is the input mode and the pull-up enable bit is the active-state. For details of pull-up/pull-down controls of P1[7:0], Please see to the Power Management section(8.15). *Note: The P1[2] and P1[5] are reserved bits.	R/W	Unknown

- PORT-0 DATA REGISTER (P0, 0x80)

Bit	Name	Descriptions	R/W	Reset Value
7:0	P0[7:0]	This port register is used as a general purpose I/O ports. When reading the each bit of PORT-0, the current status value of the corresponding bit is returned. When writing the each bit of PORT-0, the corresponding PORT-0 bit is changed to the new value. By default, the direction of P0[7:0] is the input mode and the pull-up enable bit is the active-state. For details of pull-up/pull-down controls of P0[7:0], Please see to the Power Management section(8.15).	R/W	Unknown

8.2.2 Port Direction Registers (SFR area)

- PORT-0 OUTPUT ENABLE REGISTER (P0OEN, 0xB1)

This register is SFR for setting the PORT-0 directions.

Bit	Name	Descriptions	R/W	Reset Value
7:0	P0OEN[7:0]	When writing a '1' to the port direction SFR bit, sets the corresponding bit to be an input. Writing a '0' causes the port bit to be an output.	R/W	0xFF

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- PORT-1 OUTPUT ENABLE REGISTER (P1OEN, 0xB2)

This register is SFR for setting the PORT-1 directions.

Bit	Name	Descriptions	R/W	Reset Value
7:0	P1OEN[7:0]	When writing a '1' to the port direction SFR bit, sets the corresponding bit to be an input. Writing a '0' causes the port bit to be an output. **NOTE:** The P1OEN[2] and P1OEN[5] are reserved bits.	R/W	0xFF

- PORT-3 OUTPUT DATA REGISTER (P3OEN, 0xB4)

This register is SFR for setting the PORT-3 directions.

Bit	Name	Descriptions	R/W	Reset Value
7:0	P3OEN[7:0]	When writing a '1' to the port direction SFR bit, sets the corresponding bit to be an input. Writing a '0' causes the port bit to be an output.	R/W	0xFF

8.2.3 Port Input Enable Registers (SFR area)

- PORT-0 INPUT ENABLE REGISTER (P0_IE, 0xB9)

This register is SFR for enabling or disabling the inputs from the external PORT-0 PADs.

Please refer to [Figure 11] and [Table 9] above for PAD IN/OUT pins and operation modes.

Bit	Name	Descriptions	R/W	Reset Value
7:0	P0_IE[7:0]	When writing a '1' to the PORT-0 PAD input enable SFR bit, enabled the input from the corresponding PORT-0 PAD. Writing a '0' causes the input from PAD to be disabled.	R/W	0xFF

- PORT-1 INPUT ENABLE REGISTER (P1_IE, 0xBA)

This register is SFR for enabling or disabling the inputs from the external PORT-1 PADs.

Bit	Name	Descriptions	R/W	Reset Value
7:0	P1_IE[7:0]	When writing a '1' to the PORT-1 PAD input enable SFR bit, enabled the input from the corresponding PORT-1 PAD. Writing a '0' causes the input from PAD to be disabled.	R/W	0xFF

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		NOTE: The P1_IE[2] and P1_IE[5] are reserved bits.		

- PORT-3 INPUT ENABLE REGISTER (P3_IE, 0xBC)

This register is SFR for enabling or disabling the inputs from the external PORT-3 PADs.

Bit	Name	Descriptions	R/W	Reset Value
7:0	P3_IE[7:0]	When writing a '1' to the PORT-3 PAD input enable SFR bit, enabled the input from the corresponding PORT-3 PAD. Writing a '0' causes the input from PAD to be disabled.	R/W	0xFF

8.2.4 Port Drive Strength Selection Registers (SFR area)

- PORT-0 DRIVE STRENGTH SELECTION REGISTER-0 (P0_DS0, 0xC1)

This register is SFR for selecting the drive strength capability of PORT-0, DS0.

Bit	Name	Descriptions	R/W	Reset Value
7	P0_DS0[7]	Configure the DS0 value of P0[7]-pin	R/W	0
6	P0_DS0[6]	Configure the DS0 value of P0[6]-pin	R/W	0
5	P0_DS0[5]	Configure the DS0 value of P0[5]-pin	R/W	0
4	P0_DS0[4]	Configure the DS0 value of P0[4]-pin	R/W	0
3	P0_DS0[3]	Configure the DS0 value of P0[3]-pin	R/W	0
2	P0_DS0[2]	Configure the DS0 value of P0[2]-pin	R/W	0
1	P0_DS0[1]	Configure the DS0 value of P0[1]-pin	R/W	0
0	P0_DS0[0]	Configure the DS0 value of P0[0]-pin	R/W	0

- PORT-0 DRIVE STRENGTH SELECTION REGISTER-1 (P0_DS1, 0xD9)

This register is SFR for selecting the drive strength capability of PORT-0, DS1.

Bit	Name	Descriptions	R/W	Reset Value
7	P0_DS1[7]	Configure the DS1 value of P0[7]-pin	R/W	0
6	P0_DS1[6]	Configure the DS1 value of P0[6]-pin	R/W	0
5	P0_DS1[5]	Configure the DS1 value of P0[5]-pin	R/W	0
4	P0_DS1[4]	Configure the DS1 value of P0[4]-pin	R/W	0
3	P0_DS1[3]	Configure the DS1 value of P0[3]-pin	R/W	0
2	P0_DS1[2]	Configure the DS1 value of P0[2]-pin	R/W	0
1	P0_DS1[1]	Configure the DS1 value of P0[1]-pin	R/W	0
0	P0_DS1[0]	Configure the DS1 value of P0[0]-pin	R/W	0

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- PORT-0 DRIVE STRENGTH SELECTION REGISTER-2 (P0_DS2, 0xE1)

This register is SFR for selecting the drive strength capability of PORT-0, DS2.

Bit	Name	Descriptions	R/W	Reset Value
7	P0_DS2[7]	Configure the DS2 value of P0[7]-pin	R/W	0
6	P0_DS2[6]	Configure the DS2 value of P0[6]-pin	R/W	0
5	P0_DS2[5]	Configure the DS2 value of P0[5]-pin	R/W	0
4	P0_DS2[4]	Configure the DS2 value of P0[4]-pin	R/W	0
3	P0_DS2[3]	Configure the DS2 value of P0[3]-pin	R/W	0
2	P0_DS2[2]	Configure the DS2 value of P0[2]-pin	R/W	0
1	P0_DS2[1]	Configure the DS2 value of P0[1]-pin	R/W	0
0	P0_DS2[0]	Configure the DS2 value of P0[0]-pin	R/W	0

- PORT-1 DRIVE STRENGTH SELECTION REGISTER (P1_DS0, 0xC2)

This register is SFR for selecting the drive strength capability of PORT-1, DS0.

Bit	Name	Descriptions	R/W	Reset Value
7	P1_DS0[7]	Configure the DS0 value of P1[7]-pin	R/W	0
6	P1_DS0[6]	Configure the DS0 value of P1[6]-pin	R/W	0
5		Reserved	RO	0
4	P1_DS0[4]	Configure the DS0 value of P1[4]-pin	R/W	0
3	P1_DS0[3]	Configure the DS0 value of P1[3]-pin	R/W	0
2		Reserved	RO	0
1	P1_DS0[1]	Configure the DS0 value of P1[1]-pin	R/W	0
0	P1_DS0[0]	Configure the DS0 value of P1[0]-pin	R/W	0

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- PORT-1 DRIVE STRENGTH SELECTION REGISTER (P1_DS1, 0xDA)

This register is SFR for selecting the drive strength capability of PORT-1, DS1.

Bit	Name	Descriptions	R/W	Reset Value
7	P1_DS1[7]	Configure the DS1 value of P1[7]-pin	R/W	0
6	P1_DS1[6]	Configure the DS1 value of P1[6]-pin	R/W	0
5		Reserved	RO	0
4	P1_DS1[4]	Configure the DS1 value of P1[4]-pin	R/W	0
3	P1_DS1[3]	Configure the DS1 value of P1[3]-pin	R/W	0
2		Reserved	RO	0
1	P1_DS1[1]	Configure the DS1 value of P1[1]-pin	R/W	0
0	P1_DS1[0]	Configure the DS1 value of P1[0]-pin	R/W	0

- PORT-1 DRIVE STRENGTH SELECTION REGISTER (P1_DS2, 0xE2)

This register is SFR for selecting the drive strength capability of PORT-1, DS2.

Bit	Name	Descriptions	R/W	Reset Value
7	P1_DS2[7]	Configure the DS2 value of P1[7]-pin	R/W	0
6	P1_DS2[6]	Configure the DS2 value of P1[6]-pin	R/W	0
5		Reserved	RO	0
4	P1_DS2[4]	Configure the DS2 value of P1[4]-pin	R/W	0
3	P1_DS2[3]	Configure the DS2 value of P1[3]-pin	R/W	0
2		Reserved	RO	0
1	P1_DS2[1]	Configure the DS2 value of P1[1]-pin	R/W	0
0	P1_DS2[0]	Configure the DS2 value of P1[0]-pin	R/W	0

- PORT-3 DRIVE STRENGTH SELECTION REGISTER (P3_DS, 0xC4)

This register is SFR for selecting the drive strength capability of PORT-3, DS0.

Bit	Name	Descriptions	R/W	Reset Value
7	P3_DS0[7]	Configure the DS0 value of P3[7]-pin	R/W	0
6	P3_DS0[6]	Configure the DS0 value of P3[6]-pin	R/W	0
5	P3_DS0[5]	Configure the DS0 value of P3[5]-pin	R/W	0
4	P3_DS0[4]	Configure the DS0 value of P3[4]-pin	R/W	0
3	P3_DS0[3]	Configure the DS0 value of P3[3]-pin	R/W	0
2	P3_DS0[2]	Configure the DS0 value of P3[2]-pin	R/W	0
1	P3_DS0[1]	Configure the DS0 value of P3[1]-pin	R/W	0
0	P3_DS0[0]	Configure the DS0 value of P3[0]-pin	R/W	0

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- PORT-3 DRIVE STRENGTH SELECTION REGISTER (P3_DS, 0xDC)

This register is SFR for selecting the drive strength capability of PORT-3, DS1.

Bit	Name	Descriptions	R/W	Reset Value
7	P3_DS1[7]	Configure the DS1 value of P3[7]-pin	R/W	0
6	P3_DS1[6]	Configure the DS1 value of P3[6]-pin	R/W	0
5	P3_DS1[5]	Configure the DS1 value of P3[5]-pin	R/W	0
4	P3_DS1[4]	Configure the DS1 value of P3[4]-pin	R/W	0
3	P3_DS1[3]	Configure the DS1 value of P3[3]-pin	R/W	0
2	P3_DS1[2]	Configure the DS1 value of P3[2]-pin	R/W	0
1	P3_DS1[1]	Configure the DS1 value of P3[1]-pin	R/W	0
0	P3_DS1[0]	Configure the DS1 value of P3[0]-pin	R/W	0

- PORT-3 DRIVE STRENGTH SELECTION REGISTER (P3_DS, 0xE4)

This register is SFR for selecting the drive strength capability of PORT-3, DS2.

Bit	Name	Descriptions	R/W	Reset Value
7	P3_DS2[7]	Configure the DS2 value of P3[7]-pin	R/W	0
6	P3_DS2[6]	Configure the DS2 value of P3[6]-pin	R/W	0
5	P3_DS2[5]	Configure the DS2 value of P3[5]-pin	R/W	0
4	P3_DS2[4]	Configure the DS2 value of P3[4]-pin	R/W	0
3	P3_DS2[3]	Configure the DS2 value of P3[3]-pin	R/W	0
2	P3_DS2[2]	Configure the DS2 value of P3[2]-pin	R/W	0
1	P3_DS2[1]	Configure the DS2 value of P3[1]-pin	R/W	0
0	P3_DS2[0]	Configure the DS2 value of P3[0]-pin	R/W	0

8.2.5 Port Pull-up/down Control Registers

These registers are mapped to the DATA memory area and can be accessed by MOVX instruction of 8051 core. These registers value are retained in the power down mode.

Please refer to the GPIOPS0/GPIOPE0/GPIOSPU0, GPIOPS1/GPIOPE1/GPIOSPU1, GPIOPS3/GPIOPE3/GPIOSPU3 registers in the section 8.24 for details on the register setting.

8.2.6 Port Interrupt Control Registers (SFR area)

The interrupt generation from GPIO pins is valid only under the normal mode. In the power down mode, all GPIO pins can be only used as the wakeup sources depending on the always-on register setting. (Please refer to the Sec 8.21.) The interrupt vector address is also different in case of normal mode and power down mode. (normal: 0x83, power down:0x7B)

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- PORT-0 INTERRUPT POLARITY SELECTION REGISTER (P0_POL, 0xEA)

This register is SFR for selecting the active interrupt polarity of PORT-0.

Bit	Name	Descriptions	R/W	Reset Value
7	P0_POL[7]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
6	P0_POL[6]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
5	P0_POL[5]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
4	P0_POL[4]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
3	P0_POL[3]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
2	P0_POL[2]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
1	P0_POL[1]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
0	P0_POL[0]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0

- PORT-0 INTERRUPT EDGE SELECTION REGISTER (P0_EDGE, 0xEB)

This register is SFR for selecting the interrupt mode of PORT-0.

Bit	Name	Descriptions	R/W	Reset Value
7	P0_EDGE[7]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
6	P0_EDGE[6]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
5	P0_EDGE[5]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
4	P0_EDGE[4]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
3	P0_EDGE[3]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
2	P0_EDGE[2]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
1	P0_EDGE[1]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
0	P0_EDGE[0]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0

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- PORT-0 INTERRUPT ENABLE REGISTER (P0_IRQ_EN, 0xEC)

This register is SFR for selecting the interrupt enabled/disabled function of PORT-0.

Bit	Name	Descriptions	R/W	Reset Value
7	P0_IRQ_EN[7]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
6	P0_IRQ_EN[6]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
5	P0_IRQ_EN[5]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
4	P0_IRQ_EN[4]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
3	P0_IRQ_EN[3]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
2	P0_IRQ_EN[2]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
1	P0_IRQ_EN[1]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
0	P0_IRQ_EN[0]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0

- PORT-0 INTERRUPT FLAG REGISTER (P0_IRQ_STS, 0xED)

This register is SFR for reflecting the interrupt status flags of PORT-0.

Bit	Name	Descriptions	R/W	Reset Value
7	P0_IRQ_STS[7]	0 : No interrupt generation for P0[7] 1 : the pending interrupt generation for P0[7] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0
6	P0_IRQ_STS[6]	0 : No interrupt generation for P0[6] 1 : the pending interrupt generation for P0[6] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0
5	P0_IRQ_STS[5]	0 : No interrupt generation for P0[5] 1 : the pending interrupt generation for P0[5] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0
4	P0_IRQ_STS[4]	0 : No interrupt generation for P0[4] 1 : the pending interrupt generation for P0[4] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0

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3	P0_IRQ_STS[3]	0 : No interrupt generation for P0[3] 1 : the pending interrupt generation for P0[3] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0
2	P0_IRQ_STS[2]	0 : No interrupt generation for P0[2] 1 : the pending interrupt generation for P0[2] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0
1	P0_IRQ_STS[1]	0 : No interrupt generation for P0[1] 1 : the pending interrupt generation for P0[1] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0
0	P0_IRQ_STS[0]	0 : No interrupt generation for P0[0] 1 : the pending interrupt generation for P0[0] **NOTE:** For the interrupt clear, the 1 must be written to this bit.	R/W	0

- PORT-1 INTERRUPT POLARITY SELECTION REGISTER (P1_POL, 0xF2)

This register is SFR for selecting the active interrupt polarity of PORT-1.

Bit	Name	Descriptions	R/W	Reset Value
7	P1_POL[7]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
6	P1_POL[6]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
5		Reserved bit		
4	P1_POL[4]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
3	P1_POL[3]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
2		Reserved bit		
1	P1_POL[1]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
0	P1_POL[0]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0

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- PORT-1 INTERRUPT EDGE SELECTION REGISTER (P1_EDGE, 0xF3)

This register is SFR for selecting the interrupt mode of PORT-1.

Bit	Name	Descriptions	R/W	Reset Value
7	P1_EDGE[7]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
6	P1_EDGE[6]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
5		Reserved bit		
4	P1_EDGE[4]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
3	P1_EDGE[3]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
2		Reserved bit		
1	P1_EDGE[1]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
0	P1_EDGE[0]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0

- PORT-1 INTERRUPT ENABLE REGISTER (P1_IRQ_EN, 0xF4)

This register is SFR for selecting the interrupt enabled/disabled function of PORT-1.

Bit	Name	Descriptions	R/W	Reset Value
7	P1_IRQ_EN[7]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
6	P1_IRQ_EN[6]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
5		Reserved bit	RO	0
4	P1_IRQ_EN[4]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
3	P1_IRQ_EN[3]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
2		Reserved bit	RO	0
1	P1_IRQ_EN[1]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
0	P1_IRQ_EN[0]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0

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- PORT-1 INTERRUPT FLAG REGISTER (P1_IRQ_STS, 0xF5)

This register is SFR for reflecting the interrupt status flags of PORT-1.

Bit	Name	Descriptions	R/W	Reset Value
7	P1_IRQ_STS[7]	0 : No interrupt generation for P1[7] 1 : the pending interrupt generation for P1[7] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
6	P1_IRQ_STS[6]	0 : No interrupt generation for P1[6] 1 : the pending interrupt generation for P1[6] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
5		Reserved bit		
4	P1_IRQ_STS[4]	0 : No interrupt generation for P1[4] 1 : the pending interrupt generation for P1[4] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
3	P1_IRQ_STS[3]	0 : No interrupt generation for P1[3] 1 : the pending interrupt generation for P1[3] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
2		Reserved bit		
1	P1_IRQ_STS[1]	0 : No interrupt generation for P1[1] 1 : the pending interrupt generation for P1[1] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
0	P1_IRQ_STS[0]	0 : No interrupt generation for P1[0] 1 : the pending interrupt generation for P1[0] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0

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- PORT-3 INTERRUPT POLARITY SELECTION REGISTER (P3_POL, 0xFA)

This register is SFR for selecting the active interrupt polarity of PORT-3.

Bit	Name	Descriptions	R/W	Reset Value
7	P3_POL[7]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
6	P3_POL[6]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
5	P3_POL[5]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
4	P3_POL[4]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
3		Reserved bit	RO	0
2		Reserved bit	RO	0
1	P3_POL[1]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0
0	P3_POL[0]	0 : low level/falling edge interrupt selection 1 : high level/rising edge interrupt selection	R/W	0

- PORT-3 INTERRUPT EDGE SELECTION REGISTER (P3_EDGE, 0xFB)

This register is SFR for selecting the interrupt mode of PORT-3.

Bit	Name	Descriptions	R/W	Reset Value
7	P3_EDGE[7]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
6	P3_EDGE[6]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
5	P3_EDGE[5]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
4	P3_EDGE[4]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
3		Reserved bit	RO	0
2		Reserved bit	RO	0
1	P3_EDGE[1]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0
0	P3_EDGE[0]	0 : level interrupt mode 1 : edge interrupt mode	R/W	0

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- PORT-3 INTERRUPT ENABLE REGISTER (P3_IRQ_EN, 0xFC)

This register is SFR for selecting the interrupt enabled/disabled function of PORT-3.

Bit	Name	Descriptions	R/W	Reset Value
7	P3_IRQ_EN[7]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
6	P3_IRQ_EN[6]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
5	P3_IRQ_EN[5]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
4	P3_IRQ_EN[4]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
3		Reserved bit	RO	0
2		Reserved bit	RO	0
1	P3_IRQ_EN[1]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0
0	P3_IRQ_EN[0]	0: interrupt generation disabled 1: interrupt generation enabled	R/W	0

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- PORT-3 INTERRUPT FLAG REGISTER (P3_IRQ_STS, 0xFD)

This register is SFR for reflecting the interrupt status flags of PORT-3.

Bit	Name	Descriptions	R/W	Reset Value
7	P3_IRQ_STS[7]	0 : No interrupt generation for P3[7] 1 : the pending interrupt generation for P3[7] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
6	P3_IRQ_STS[6]	0 : No interrupt generation for P3[6] 1 : the pending interrupt generation for P3[6] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
5	P3_IRQ_STS[5]	0 : No interrupt generation for P3[5] 1 : the pending interrupt generation for P3[5] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
4	P3_IRQ_STS[4]	0 : No interrupt generation for P3[4] 1 : the pending interrupt generation for P3[4] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
3		Reserved bit	RO	0
2		Reserved bit	RO	0
1	P3_IRQ_STS[1]	0 : No interrupt generation for P3[1] 1 : the pending interrupt generation for P3[1] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0
0	P3_IRQ_STS[0]	0 : No interrupt generation for P3[0] 1 : the pending interrupt generation for P3[0] *Note: For the interrupt clear, the 1 must be written to this bit.	R/W	0

- PORTs INTERRUPT PENDING REGISTER (GPIO_IRQ_PEND, 0xF1)

This register is SFR for reflecting the pending interrupt flags of PORT-0/1/3.

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved bits	RO	0
2	P3_IRQ_PEND	0 : No interrupt generation 1 : The pending interrupt flag for Port-3	RO	0
1	P1_IRQ_PEND	0 : No interrupt generation 1 : The pending interrupt flag for Port-1	RO	0
0	P0_IRQ_PEND	0 : No interrupt generation 1 : The pending interrupt flag for Port-0	RO	0

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8.3 TIMER 0/1

The MG2475 has two 16-bit timers which are compatible with Intel 8051 MCU (Timer0, Timer1). These timers have 2 modes; one is operated as a timer and the other is operated as a counter. When it is operated as a timer, there are 4 operating modes.

Each timer is 16-bit timer and consists of two 8-bit register. Therefore, the counter can be either 8-bit or 16-bit set by the operating mode.

In counter mode, the input signal T0 (P3 [4]) and T1 (P3 [5]) are sampled once every 12 cycles of the system clock. If the sampled value is changed from '1' to '0', the internal counter is incremented. In this time, the duty cycle of T0 and T1 doesn't affect the increment. Timer0 and Timer1 are accessed by using 6 SFR's.

The following table describes timer registers and modes.

- TCON (TIMER/COUNTER CONTROL REGISTER, 0x88)

This register is used to control a timer function and monitor a timer status.

Bit	Name	Descriptions	R/W	Reset Value
7	TF1	Timer1 Overflow Flag. When this field is '1', a Timer1 interrupt occurs. After the Timer1 interrupt service routine is executed, this field value is cleared by hardware.	R/W	0
6	TR1	Timer1 Run Control. When this bit is set to '1', Timer1 is enabled.	R/W	0
5	TF0	Timer0 Interrupt Flag. 1: Interrupt is pending After Timer0 interrupt service routine is executed, this field is cleared by hardware.	R/W	0
4	TR0	Timer0 Run When this bit is set to '1', Timer0 is enabled.	R/W	0
3	IE1	External Interrupt1 Edge Flag. When this field is '1', External interrupt1 is pending. After the interrupt service routine is executed, this field is cleared by hardware.	R/W	0
2	IT1	External Interrupt1 Type Control. This field specifies the type of External interrupt1. 1=Edge type. When the falling edge of INT1 is detected, the interrupt occurs. 0=Level type. When INT1 is low level, the interrupt occurs.	R/W	0
1	IE0	External Interrupt0 Edge Flag. When this field is '1', External interrupt0 is pending. After the interrupt service routine is executed, this field is cleared by hardware.	R/W	0
0	IT0	External Interrupt0 Type Control.	R/W	0

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		This field specifies the type of External interrupt0. 1=Edge type. When the falling edge of INT0 is detected, the interrupt occurs. 0=Level type. When INT0 is low level, the interrupt occurs.		

- TMOD (TIMER/COUNTER MODE CONTROL REGISTER, 0x89)

Bit	Name	Descriptions	R/W	Reset Value
7	GATE 1	Timer Gate Control When TR1 is set to '1' and GATE1 is '1', Timer1 is enabled only while INT1 pin is high. When GATE1 is set to '0', Timer1 is enabled whenever TR1 control is set to '1'.	R/W	0
6	CT1	Timer1 Counter Mode Select When this field is set to '1', Timer1 is enabled as counter mode.	R/W	0
5:4	M1	Timer1 mode select. 0: Mode0, 12-bit Timer 1: Mode1, 16-bit Timer 2: Mode2, 8-bit Timer with auto-load 3: Mode3, two 8-bit Timer	R/W	0
3	GATE 0	Timer0 Gate Control. When TR0 is set to '1' and GATE0 is '1', Timer0 is enabled while INT0 pin is in high. When GATE1 is set to '0' and TR1 is set to '1', Timer0 is enabled.	R/W	0
2	CT0	When this field is set to '1', Timer0 is enabled as counter mode.	R/W	0
1:0	M0	Timer0 mode select 0: Mode0, 12-bit Timer 1: Mode1, 16-bit Timer 2: Mode2, 8-bit Timer with auto-load 3: Mode3, two 8-bit Timer	R/W	0

- TL0/TL1/TH0/TH1 (TIMER REGISTERS, 0x8A, 0x8B, 0x8C, 0x8D)

A pair of register, which are (TH0, TL0) and (TH1, TL1), can be used as 16-bit timer register for Timer0 and Timer1 and it can be used as 8-bit register respectively.

Bit	Name	Descriptions	R/W	Reset Value
7:0	TH1	Timer1 High Byte Data	R/W	0x00

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Bit	Name	Descriptions	R/W	Reset Value
7:0	TH0	Timer0 High Byte Data	R/W	0x00

Bit	Name	Descriptions	R/W	Reset Value
7:0	TL1	Timer1 Low Byte Data	R/W	0x00

Bit	Name	Descriptions	R/W	Reset Value
7:0	TL0	Timer0 Low Byte Data	R/W	0x00

In mode0, 13-bit register of timer0 consists of all 8-bits of TH0 and the lower 5-bits of TL0. The upper 3-bit of TL0 are disregarded. When this 13-bit register is overflowed, set TF0 to '1'. The operation of timer1 is same as that of timer0.
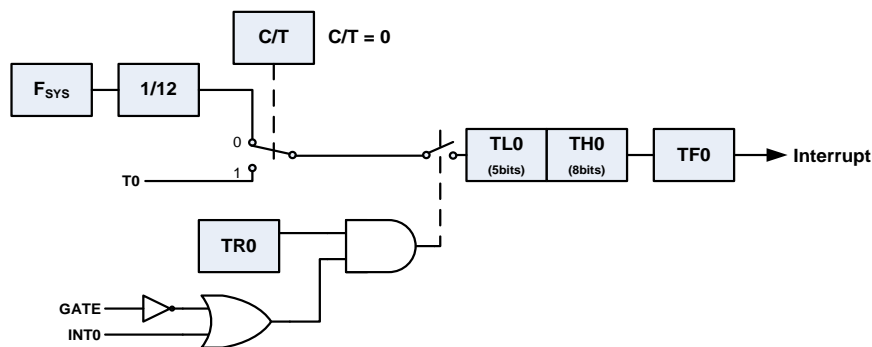
Figure 12. Timer0 Mode0

In Mode1, the operation is same as it of Mode0 except all timer registers are enabled as a 16-bit counter.
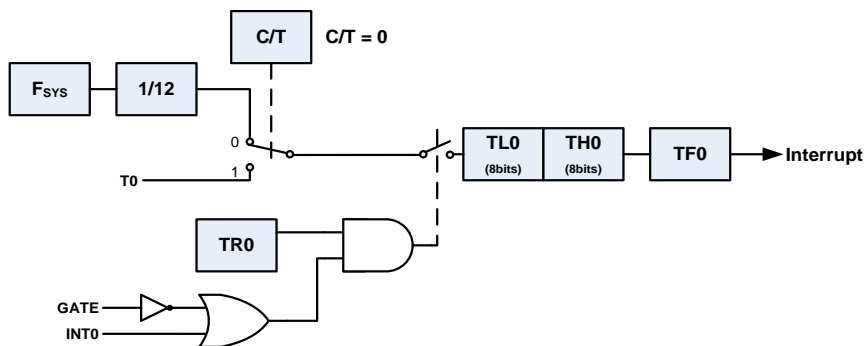
Figure 13. Timer0 Mode1

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In mode2, TL0 of Timer0 is enabled as an 8-bit counter and TH0 reloads TL0 automatically.

TF0 is set to '1' by overflowing of TL0. TH0 value retains the previous value regardless of the reloading. The operation of Timer1 is same as that of Timer0.
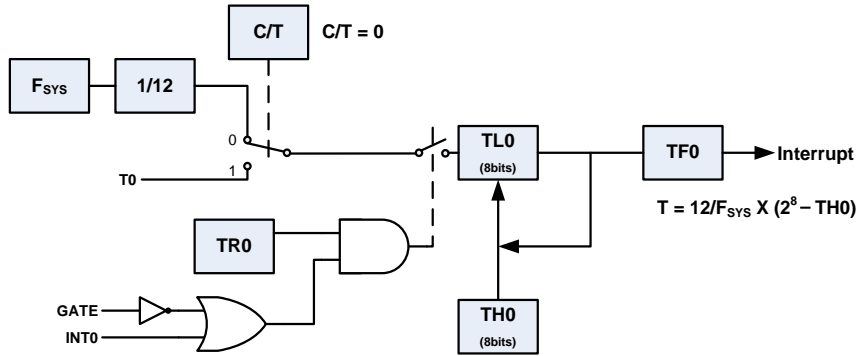
Figure 14. Timer0 Mode2

In Mode3, Timer0 uses TL0 and TH0 as an 8-bit timer respectively. In other words, it uses two counters. TL0 controls as the control signals of Timer0. TH0 is always used as a timer function and it controls as TR1 of Timer1. The overflow is stored in TF1. At this time, Timer1 is disabled and it retains the previous value.
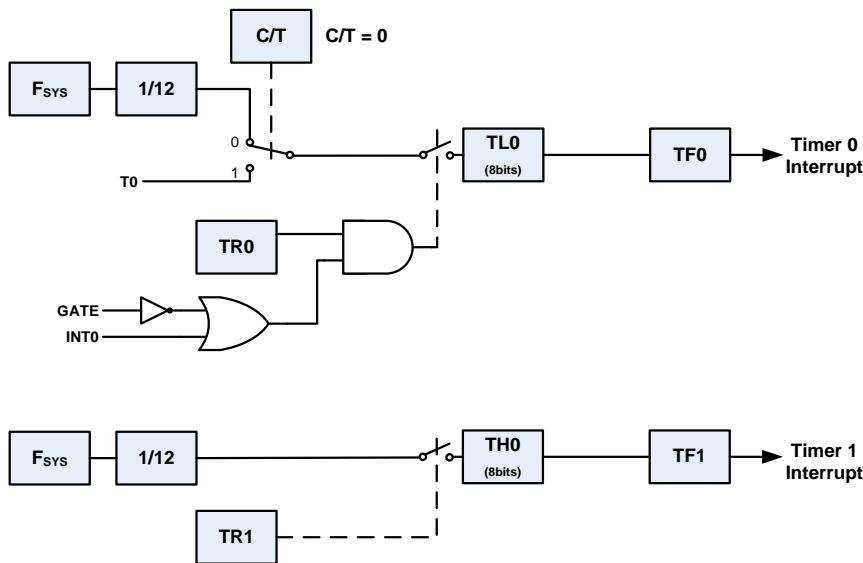
Figure 15. Timer0 Mode3

8.4 TIMER 2/3

The MG2475 includes two additional 16-bit timers, named Timer2 and Timer3.

- T23CON (TIMER2/3 CONTROL REGISTER, 0xA9)

This register is used to control the operation mode of Timer2 and Time3.

Bit	Name	Descriptions			R/W	Reset Value
7	T3_DIV2	Timer3 clock division ratio selection			R/W	0
6	T3_DIV1	**Bit values**	**Clock ratio**		R/W	1
5	T3_DIV0	3'b000	Divided by 1		R/W	0
		3'b001	Divided by 2			
		3'b010	Divided by 3 (default value)			
		3'b011	Divided by 4			
		3'b100	Divided by 8			
		3'b101	Divided by 16			
		3'b110	Divided by 32			
		3'b111	Divided by 64			
4	TR3	Timer3 Run. When this field is set to '1', Timer3 is operated.			R/W	0
3	T2_DIV2	Timer2 clock division ratio selection			R/W	0
2	T2_DIV1	**Bit values**	**Clock ratio**		R/W	1
1	T2_DIV0	3'b000	Divided by 1		R/W	1
		3'b001	Divided by 2			
		3'b010	Divided by 4			
		3'b011	Divided by 8 (default value)			
		3'b100	Divided by 16			
		3'b101	Divided by 32			
		3'b110	Divided by 64			
		3'b111	Divided by 8			
0	TR2	Timer2 Run. When this field is set to '1', Timer2 is operated.			R/W	0

- TL2/TL3/TH2/TH3 (TIMER2/3 TIMER REGISTER, 0xAC, 0xAD, 0xAA, 0xAB)

Register (TH2, TL2) and (TH3, TL3) are 16-bit timer counter register for Timer2 and Timer3.

The maximum allowed set value is 0xFFFE.

Bit	Name	Descriptions	R/W	Reset Value
7:0	TL3	Timer3 Low Byte Data	R/W	0x00

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Bit	Name	Descriptions	R/W	Reset Value
7:0	TL2	Timer2 Low Byte Data	R/W	0x00

Bit	Name	Descriptions	R/W	Reset Value
7:0	TH3	Timer3 High Byte Data	R/W	0x00

Bit	Name	Descriptions	R/W	Reset Value
7:0	TH2	Timer2 High Byte Data	R/W	0x00

Timer2 acts as a general 16-bit timer. Time-out period is calculated by the following equation;

$$\mathrm{T}2 = \frac{T23CON[3:1]division \times (256 \times TH2 + TL2 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupt causing abnormal operation of the system will occur. It is recommended to set sufficient time-out period for Timer2 (over 100μs).

Timer3 acts as a general 16-bit timer. Time-out period of Timer3 is calculated by the following equation;

$$\mathrm{T}3 = \frac{T23CON[7:4]division \times (256 \times TH3 + TL3 + 1)}{fsystem}$$

If the time-out period is set too short, excessive interrupt causing abnormal operation of the system will occur. It is recommended to set Timer3 to a sufficient time-out period.

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8.5 PWMs

The PWM is a user-programmable PWM and can also supports timer and counter controller features. Its use is to implement functions like Pulse Width Modulation (PWM), timer and counter facilities.

The following lists the main features of PWM core.

- 5 channel support
- 16-bit counter/timer facility
- Single-run or continuous run of PTC counter
- Programmable PWM mode
- HI/LO Reference and Capture registers
- PWM/Timer/Counter functionalities can cause an interrupt to the CPU

$$T = \frac{CNTR}{f_{system}}$$

When operating in PWM mode, the PWM core generates binary signal with user programmable low and high periods.

When operating in timer/counter mode, the PWM core counts number of clock cycles of system clock. After reaching low and/or high reference, the PWM core can generate an interrupt. Input signal PWM pad can be used to capture value of the CNTR register into low and high capture registers.

When operating from the system clock, PTC_GATE pin can be used to gate internal timer/counter circuitry. In both PWM and timer/counter modes, CNTR can run for a single cycle and it can automatically restart after each complete cycle. Cycle completes after reaching value in the LRC register. These two modes are called single-run and continuous- run.

- PWM Mode

To operate in PWM mode, HRC and LRC should be set with the value of low and high periods of the PWM output signal. HRC is number of clock cycles after reset of the CNTR when PWM output should go high. And LRC is number of clock cycles after reset of the CNTR when PWM output should go low.

CNTR can be reset with the hardware reset, bit CTRL[CNTRRST] or periodically when CTRL[SINGLE] bit is cleared. To enable PWM output driver, CTRL[OE] should be set. To enable continues operation, CTRL[SINGLE] should be cleared and CTRL[EN] should be set. If gate function is enabled, PWM periods can be automatically adjusted with the capture input. PWM output signal is controlled with the HRC and LRC, and these two registers can be set without software control with the PTC_GATE pin signal.

Usually interrupts are enabled in timer/counter mode. This is done with the CTRL[INTE].

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- Gate Feature

If system clock is used to increment CNTR, PTC_GATE pin input signal can be used to gate the system clock and not increment the CNTR register. Which level of the PTC_GATE pin has gating capability depends on value of the CTRL[NEC].

- Interrupt Feature

Whenever CNTR equals to the value of the HRC or LRC, an interrupt request can be asserted. This depends if CTRL[INTE] bit is set.

- Capture Feature

PWM pin input signal can be used to capture value of the current CNTR into HRC or LRC registers. Into which reference/capture register value is captured, depends on edge of the PWM pin input signal. On positive edge value is captured into HRC register and on negative edge value is captured into LRC register. In order to enable capture feature, CTRL[CAPTE] must be set.

- PWMx_CNTR

CNTR register is the actual counter register. It is incremented at every counter/timer clock cycle. In order to count, CNTR must first be enabled with the CTRL[EN]. CNTR can be reset with the CTRL[RST]. CNTR can operate in either single-run mode or continues mode. Mode is selected with the CTRL[SINGLE].

PWMx_CNTRH(PWM CHx COUNTER REGISTER MSB PART, 0x2580(CH0), 0x2588(CH1), 0x2590(CH2), 0x2598(CH3), 0x25A0(CH4))

Bit	Name	Descriptions	R/W	Reset Value
15:8	CNTR	MSB Part of CNTR register	R/W	0

PWMx_CNTRL(PWM CHx COUNTER REGISTER LSB PART, 0x2581(CH0), 0x2589(CH1), 0x2591(CH2), 0x2599(CH3), 0x25A1(CH4))

Bit	Name	Descriptions	R/W	Reset Value
7:0	CNTR	LSB Part of CNTR register	R/W	0

- PWMx_HRC

HRC register is a second out of two reference/capture registers. It has two functions;

- In reference mode it is used to assert high PWM output or to generate an interrupt.
- In capture mode it captures CNTR value on high value of PWM pin input signal.

The HRC should have lower value than LRC. This is because PWM output goes first high and later low.

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PWMx_HRCH (PWM CHx HIGH REF/CAP REGISTER, MSB Part, 0x2582(CH0), 0x258A(CH1), 0x2592(CH2), 0x259A(CH3), 0x25A2(CH4))

Bit	Name	Descriptions	R/W	Reset Value
15:8	HRC	MSB Part of HRC register	R/W	0

PWMx_HRCL (PWM CH0 HIGH REF/CAP REGISTER, LSB Part, 0x2583(CH0), 0x258B(CH1), 0x2593(CH2), 0x259B(CH3), 0x25A3(CH4))

Bit	Name	Descriptions	R/W	Reset Value
7:0	HRC	LSB Part of HRC register	R/W	0

- PWMx_LRC

LRC register is a first out of two reference/capture registers. It has two functions;

- In reference mode it is used to assert low PWM output or to generate an interrupt
- In capture mode it captures CNTR value on low value of PWM pin input signal

The LRC should have higher value than HRC. This is because PWM output goes high first and then low later.

PWMx_LRCH (PWM CHx LOW REF/CAP REGISTER, MSB Part, 0x2584(CH0), 0x258C(CH1), 0x2594(CH2), 0x259C(CH3), 0x25A4(CH4))

Bit	Name	Descriptions	R/W	Reset Value
15:8	LRC	MSB Part of LRC register	R/W	0

PWMx_LRCL (PWM CHx LOW REF/CAP REGISTER, LSB Part, 0x2585(CH0), 0x258D(CH1), 0x2595(CH2), 0x259D(CH3), 0x25A5(CH4))

Bit	Name	Descriptions	R/W	Reset Value
7:0	LRC	LSB Part of LRC register	R/W	0

- PWMx_CTRL

Control bits in CTRL register control operation of PWM core.

- PWMx_CTRL (PWM CHx CONTROL REGISTER, 0x2586(CH0), 0x258E(CH1), 0x2596(CH2), 0x259E(CH3), 0x25A6(CH4))

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Bit	Name	Descriptions	R/W	Reset Value
7	INTE	Interrupt Enable	R/W	0
6	CAPTE	When set, PWM pin input signal can be used to capture CNTR into LRC or HRC registers. Into which reference/capture register capture occurs depends on edge of the PWM pin input signal. When cleared, capture function is masked.	R/W	0
5	CNTRRST	When set, CNTR is under reset. When cleared, normal operation of the counter is allowed.	R/W	0
4	SINGLE	When set, CNTR is not incremented anymore after it reaches value equal to the LRC value. When cleared, CNTR is restarted after it reaches value in the LCR register.	R/W	0
3	OE	The value of this bit is reflected on the PWM pin output signal. It is used to enable PWM output driver.	R/W	0
2	NEC	When set, CNTR increments on low period of PTC_GATEx pin. When cleared, CNTR increments on high period of PTC_GATEx pin. This bit has effect only on 'gating' function of PTC_GATEx pin when GATE bit is set.	R/W	0
1	GATE	PTC_GATEx pin gate function enable When set, the PTC_GATEx pin is used to increase the internal 16-bit counter /timer(CNTR).	R/W	0
0	EN	When set, CNTR can be incremented.	R/W	0

- PWM_INTR (PWM INTERRUT FLAG REGISTER, 0x257F)

Bit	Name	Descriptions	R/W	Reset Value
7:5	Reserved	-	-	-
4	PWM4INTR	PWM CH4 Interrupt flag. When this field is set to '1' cleared by software.	R/W	0
3	PWM3INTR	PWM CH3 Interrupt flag. When this field is set to '1' cleared by software.	R/W	0
2	PWM2INTR	PWM CH2 Interrupt flag. When this field is set to '1' cleared by software.	R/W	0
1	PWM1INTR	PWM CH1 Interrupt flag. When this field is set to '1' cleared by software.	R/W	0
0	PWM0INTR	PWM CH0 Interrupt flag. When this field is set to '1' cleared by software.	R/W	0

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8.6 Watchdog Timer

Watchdog Timer (WDT) monitors whether MCU is normally operating or not. If a problem is caused, it immediately resets MCU. In fact, when a system does not clear WDT counter value, WDT considers that a problem is caused. Therefore, it automatically resets MCU. WDT is used when a program is not completed normally because a software error is caused in any environment such as electrical noise, unstable power, and static electricity.

When Power-up, the internal counter value of WDT is set to '0' and watchdog timer is operated. If overflow is caused in the internal counter, system reset is caused. At this moment, timeout period is about 1.0 second. A user may not use WDT by setting ENB bit of WDTCON register. When WDT operates, an application program must clear CLR bit periodically to prevent a system from being reset.

The overflow interval can be set by DUR bits. The interval calculated as follows;

$$T = \frac{2^{DUR}}{fRTCCLK}$$

To protect WDTCON register write access, special write sequence is required.

WDTCON ← 0x55 (write password 1)

WDTCON ← 0xAA (write password 2)

WDTCON ← (Control Value)

If the special sequence is not applied, it immediately resets MCU.

- WDTCON (WATCHDOG TIMER CONTROL REGISTER, MCU SFR 0xD2)

Bit	Name	Descriptions	R/W	Reset Value
7	ENB	Watchdog Timer Enable Bar. Active Low	R/W	0
6	CLR	Watchdog Timer Clear. Auto Clear Bit. This bit clear Internal WDT Counter.	WO	0
5	SYNCBUSY	Synch Busy. This bit indicates during WDT register update.	R/W	0
3:0	DUR	Watchdog Timer Duration	R/W	0xF

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8.7 UART 0/1

Serial communication is categorized as synchronous mode or asynchronous mode in terms of its data transmission method. Synchronous mode is to transmit the data based on the standard clock pulse. Asynchronous mode is to transmit the data bit by arranging the baud rate of data bit each other without standard clock. That is, when a transmitter transmits the data as arranged frequency, a receiver read the data according to the arranged method previously.

The MG2475 has UART0 and UART1 to enable two-way communication.

These devices support asynchronous mode. The following registers are used to control UART. The baudrate can be set by following expression;

$$Baudrate = \frac{fsystem}{XCR \times Divisor(16bits)}$$

Table 10 below shows the values of example baud-rate setting.

Table 10. The example of baud-rate setting

Baudrate	8MHz			16MHz		
	XCR	DLM	DLL	XCR	DLM	DLL
57,600	0x06	0x00	0x17	0x8B	0x00	0x02
115,200	0x17	0x00	0x03	0x06	0x00	0x17
230,400	0x05	0x00	0x07	0x17	0x00	0x03

- RBR (UART0 RECEIVE BUFFER REGISTER, 0x2500)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RBR	Read the received data	RO	0x00

- THR (UART0 TRANSMITTER HOLDING REGISTER, 0x2500)

Bit	Name	Descriptions	R/W	Reset Value
7:0	THR	This register stores the data to be transmitted. The address is the same as RBR register. When accessing this address, received data(RBR) is read and the data to be transmitted is stored.	WO	0x00

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- DLL (UART0 DIVISOR LSB REGISTER, 0x2500)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DLL	This register can be accessed only when DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLM register occupying the lower 8 bits. This full 16-bit register is used to divide clock.	R/W	0x00

- IER (UART0 INTERRUPT ENABLE REGISTER, 0x2501)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved		0
3	EDSSI	Enable MODEM Status Interrupt. When this field is set to '1', Modem status interrupt is enabled.	R/W	0
2	ELSI	Enable Receiver Line Status Interrupt.	R/W	0
1	ETBEI	Enable Transmitter Holding Register Empty Interrupt	R/W	0
0	ERBEI	Enable Received Data Available Interrupt	R/W	0

- DLM (UART0 DIVISOR LATCH MSB REGISTER, 0x2501)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DLM	This register can be accessed only when DLAB bit in the LCR register is set to '1'. This register shares a 16-bit register with the DLL register occupying the higher 8 bits. This full 16-bit register is used to divide clock.	R/W	0x00

- IIR (UART0 INTERRUPT IDENTIFICATION REGISTER, 0x2502)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0
3:1	INTID	Interrupt Identification. Refer to the [Table 7] below.	RO	0
0	PENDING	Shows whether the interrupt is pending or not. When this field is '0', the interrupt is pending.	RO	1

Note: IIR register uses the same address as FCR register below. IIR register is read only and FCR register is write-only.

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Table 11. UART0 Interrupt List

INTID	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
011	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the LSR (Line Status Register).
010	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
110	2nd	Timeout Indication	There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 character times.	Reading from the FIFO (Receiver Buffer Register)
001	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR
000	4th	Modem Status	CTS, DSR, RI or DCD	Reading the Modem status register

- FCR (UART0 FIFO CONTROL REGISTER, 0x2502)

Bit	Name	Descriptions	R/W	Reset Value
7:6	URXFTRIG	Adjust the trigger level of Receiver FIFO. Interrupt occurs when FIFO receives the data byte based on this field value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 byte. When FIFO receives 14 byte, interrupt occurs. 0: 1byte 1: 4 byte 2: 8 byte 3: 14 byte	WO	3
5:3		Reserved	WO	0
2	UTXFRST	When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset.	WO	0
1	URXFRST	When this field is set to '1', Receiver FIFO is cleared and the circuits related to it are reset.	WO	0
0		Reserved	WO	0

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- LCR (UART0 LINE CONTROL REGISTER, 0x2503)

Bit	Name	Descriptions	R/W	Reset Value
7	DLAB	Divisor Latch Access Enable. When this field is set to '1', Divisor register (DLM, DLL) can be accessed. When this field is set to '0', general register can be accessed.	R/W	0
6	SB	Set Break. When this field is set to '1', serial output is forced to be '0'(break state).	R/W	0
5	SP	Stick Parity. When PEN and EPS are '1' while this field set to '1', a parity of '0' is transmitted. In reception mode, it checks whether parity value is '0' or not. When PEN is '1' and EPS is '0' while this field is to '1', parity of '1', is transmitted. In reception mode, it checks whether parity value is '1' or not.	R/W	0
4	EPS	Even Parity Enable. When this field is set to '1', parity value is even. When set to '0', parity value is odd.	R/W	0
3	PEN	Parity Enable. When this field is set to '1', parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is '0', parity is not generated.	R/W	0
2	STB	Number of Stop Bits. When this field is set to '1', 2 stop bit is used. When transmitting a word (character) of 5 bit length, 1.5 stop bit is used. When this field is '0', 1 stop bit is used.	R/W	0
1:0	WLS	Word Length Select. 0: 5bit Word 1: 6bit Word 2: 7bit Word 3: 8bit Word	R/W	3

- LSR (UART0 LINE STATUS REGISTER, 0x2505)

Bit	Name	Descriptions	R/W	Reset Value
7	ERCVR	Error in Receiver Indicator. 1: At least one parity error, framing error or break indications have been received. The bit is cleared upon reading from the register.	RO	0

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		0: Otherwise.		
6	TEMT	Transmitter Empty indicator. 1: Both the transmitter FIFO and transmitter shift register are empty. The bit is cleared when data is being been written to the transmitter FIFO. 0: Otherwise.	RO	1
5	THRE	Transmit FIFO is empty. 1: The transmitter FIFO is empty. Generates Transmitter Holding Register Empty interrupt. The bit is cleared when data is being been written to the transmitter FIFO. 0: Otherwise.	RO	1
4	BI	Break Interrupt (BI) indicator. 1: A break condition has been reached in the current character. The break occurs when the line is held in logic 0 for a time of one character (start bit + data + parity + stop bit). In that case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. The bit is cleared upon reading from the register. Generates receiver Line Status interrupt. 0: No break condition in the current character.	RO	0
3	FE	Framing Error (FE) indicator. 1: The received character at the top of the FIFO did not have a valid stop bit. Of course, generally, it might be that all the following data is corrupt. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. 0: No framing error in the current character.	RO	0
2	PE	Parity Error (PE) indicator. 1: The character that is currently at the top of the FIFO has been received with parity error. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. 0: No parity error in the current character.	RO	0
1	OE	Overrun Error (OE) indicator. 1: If the FIFO is full and another character has been received in the receiver shift register. If another character is starting to arrive, it will overwrite the data in the shift register but the FIFO will remain intact. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. 0: No overrun state	RO	0
0	DR	Data Ready (DR) indicator. 0: No characters in the FIFO.	RO	0

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		1: At least one character has been received and is in the FIFO.		

- XCR (UART0 DIVISOR LSB REGISTER, 0x2507)

Bit	Name	Descriptions	R/W	Reset Value
7:0	XCR	This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 8 bit register. XCR register with DLM, DLL registers used in baudrate generation.	R/W	0x10

- ECR (UART0 EXTRA FEATURE CONTROL REGISTER, 0x2505)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved.	WO	0
2:0	ECR	Extra feature control register. 0: Default register access 2: RX FIFO Interrupt level (RIL) register access enable. 5: TX FIFO level count (TLC) register and RX FIFO level count (RLC) register access enable.	WO	0

- TLC (UART0 TX FIFO LEVEL COUNT REGISTER, 0x2503)

Bit	Name	Descriptions	R/W	Reset Value
7:0	TXLVLCNT	This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the TX FIFO	RO	0x00

- RIL (UART0 RX FIFO INTERRUPT LEVEL REGISTER, 0x2504)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RXINTLVL	This register can be accessed when ECR register is set to '2'. When RIL register is set to zero value, the URXFTRIG field of FCR is valid. If RIL register is set to non-zero value, the receiver FIFO interrupt occurs when received bytes is greater than or equal to RIL register value.	R/W	0x00

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- RLC (UART0 RX FIFO LEVEL COUNT REGISTER, 0x2504)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RXLVLCNT	This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the RX FIFO.	RO	0x00

- VSPMUX (VOICE SOURCE PATH MUX CONTROL REGISTER, 0x277F)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved.	RO	0
2:0	VSPMUX	When VSPMUX register set to '1', UART0 FIFO size is changed 128-entry. Otherwise, UART0 FIFO size is 16-entry. The detailed information is in the Voice Part.	R/W	0

The following registers are to control UART1.

- RBR (UART1 RECEIVE BUFFER REGISTER, 0x2510)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RBR	Read the received data	RO	0x00

- THR (UART1 TRANSMITTER HOLDING REGISTER, 0x2510)

Bit	Name	Descriptions	R/W	Reset Value
7:0	THR	This register stores the data to be transmitted. The address is same as RBR register. By accessing this address, received data(RBR) can be read and the data to be transmitted can be stored.	WO	0x00

- DLL (UART1 DIVISOR LSB REGISTER, 0x2510)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DLL	This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 16-bit register with DLM register and it is a lower 8 bit of 16-bit. This 16-bit register is used to divide clock.	R/W	0x00

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- IER (UART1 INTERRUPT ENABLE REGISTER, 0x2511)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0
3	EDSSI	Enable MODEM Status Interrupt. When this field is set to '1', Modem status interrupt is enabled.	R/W	0
2	ELSI	Enable Receiver Line Status Interrupt.	R/W	0
1	ETBEI	Enable Transmitter Holding Register Empty Interrupt	R/W	0
0	ERBEI	Enable Received Data Available Interrupt	R/W	0

- DLM (UART1 DIVISOR LATCH MSB REGISTER, 0x2511)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DLM	This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 16-bit register with DLL register and it is a higher 8 bit of 16-bit. This 16-bit register is used to divide clock.	R/W	0x00

- IIR (UART1 INTERRUPT IDENTIFICATION REGISTER, 0x2512)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0
3:1	INTID	Interrupt Identification. Refer to the [Table 8] below.	RO	0
0	PENDING	Shows whether the interrupt is pending or not. When this field is '0', the interrupt is pending.	RO	1

NOTE: IIR register uses the same address as FCR register below. IIR register is read only and FCR register is write-only.

Table 12. UART1 Interrupt List

INTID	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
011	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the LSR (Line Status Register).
010	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
110	2nd	Timeout Indication	There is at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4	Reading from the FIFO (Receiver Buffer Register)

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			character times.	
001	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR
000	4th	Modem Status	CTS, DSR, RI or DCD	Reading the Modem status register

- FCR (UART1 FIFO CONTROL REGISTER, 0x2512)

Bit	Name	Descriptions	R/W	Reset Value
7:6	URXFTRIG	Adjust the trigger level of Receiver FIFO. Interrupt occurs when FIFO receives the data byte based on this field's value below. For example, when URXFTRIG field is set to '3', interrupt does not occur until FIFO receives 14 bytes. When FIFO receives 14 byte, interrupt occurs. 0: 1byte 1: 4 byte 2: 8 byte 3: 14 byte	WO	3
5:3		Reserved	WO	0
2	UTXFRST	When this field is set to '1', Transmitter FIFO is cleared and the circuits related to it are reset.	WO	0
1	URXFRST	When this field is set to '1', Receiver FIFO is cleared and the circuits related to it are reset.	WO	0
0		Reserved	WO	0

- LCR (UART1 LINE CONTROL REGISTER, 0x2513)

Bit	Name	Descriptions	R/W	Reset Value
7	DLAB	Divisor Latch Access Enable. When this field is set to '1', Divisor register (DLM, DLL) can be accessed. When this field is set to '0', general register can be accessed.	R/W	0
6	SB	Set Break. When this field is set to '1', serial output is forced to be '0'(break state).	R/W	0
5	SP	Stick Parity. When PEN and EPS are '1' while this field set to '1', a parity of '0' is transmitted. In reception mode, it checks whether parity value is '0' or not. When PEN is '1' and EPS is '0' while this field	R/W	0

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Bit	Name	Descriptions	R/W	Reset Value
		is to '1', parity of '1', is transmitted. In reception mode, it checks whether parity value is '1' or not.		
4	EPS	Even Parity Enable. When this field is set to '1', parity value is even. When set to '0', parity value is odd.	R/W	0
3	PEN	Parity Enable. When this field is set to '1', parity is calculated for the byte to be transmitted and transferred with it. In reception mode, checks parity. When this field is '0', parity is not generated.	R/W	0
2	STB	Number of Stop Bits. When this field is set to '1', 2 stop bit is used. When transmitting a word (character) of 5 bit length, 1.5 stop bit is used. When this field is '0', 1 stop bit is used.	R/W	0
1:0	WLS	Word Length Select. 0: 5bit Word 1: 6bit Word 2: 7bit Word 3: 8bit Word	R/W	3

- LSR (UART1 LINE STATUS REGISTER, 0x2515)

Bit	Name	Descriptions	R/W	Reset Value
7	ERCVR	Error in Receiver Indicator. 1: At least one parity error, framing error or break indications have been received. The bit is cleared upon reading from the register. 0: Otherwise.	RO	0
6	TEMT	Transmitter Empty indicator. 1: Both the transmitter FIFO and transmitter shift register are empty. The bit is cleared when data is being been written to the transmitter FIFO. 0: Otherwise.	RO	1
5	THRE	Transmit FIFO is empty. 1: The transmitter FIFO is empty. Generates Transmitter Holding Register Empty interrupt. The bit is cleared when data is being been written to the transmitter FIFO. 0: Otherwise.	RO	1
4	BI	Break Interrupt (BI) indicator. 1: A break condition has been reached in the current character. The break occurs when the line is held in logic 0 for a time of one character	RO	0

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		(start bit + data + parity + stop bit). In that case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. The bit is cleared upon reading from the register. Generates receiver Line Status interrupt. 0: No break condition in the current character.		
3	FE	Framing Error (FE) indicator. 1: The received character at the top of the FIFO did not have a valid stop bit. Of course, generally, it might be that all the following data is corrupt. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. 0: No framing error in the current character.	RO	0
2	PE	Parity Error (PE) indicator. 1: The character that is currently at the top of the FIFO has been received with parity error. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. 0: No parity error in the current character.	RO	0
1	OE	Overrun Error (OE) indicator. 1: If the FIFO is full and another character has been received in the receiver shift register. If another character is starting to arrive, it will overwrite the data in the shift register but the FIFO will remain intact. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. 0: No overrun state	RO	0
0	DR	Data Ready (DR) indicator. 0: No characters in the FIFO 1: At least one character has been received and is in the FIFO.	RO	0

- XCR (UART1 CLOCK DIVISOR REGISTER, 0x2517)

Bit	Name	Descriptions	R/W	Reset Value
7:0	XCR	This register can be accessed only when DLAB bit in LCR register is set to '1'. This register consists of 8 bit register. XCR register with DLM and DLL registers used in UART baudrate generation.	R/W	0x10

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- ECR (UART1 EXTRA FEATURE CONTROL REGISTER, 0x2515)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved.	RO	0
2:0	ECR	Extra feature control register 0: Default register access. 2: RX FIFO Interrupt level (RIL) register access enable. 5: TX FIFO level count (TLC) register and RX FIFO level count (RLC) register access enable.	WO	0

- TLC   (UART1 TX FIFO LEVEL COUNT REGISTER, 0x2513)

Bit	Name	Descriptions	R/W	Reset Value
7:0	TXLVLCNT	This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the TX FIFO	RO	0x00

- RIL (UART1 RX FIFO INTERRUPT LEVEL REGISTER, 0x2514)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RXINTLVL	This register can be accessed when ECR register is set to '2'. when RIL register is set to zero value, the URXFTRIG field of FCR is valid. If RIL register is set to non-zero value, the receiver FIFO interrupt occurs when received bytes is greater than or equal to RIL register value.	R/W	0x00

- RLC   (UART1 RX FIFO LEVEL COUNT REGISTER, 0x2514)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RXLVLCNT	This register can be accessed when ECR register is set to '5'. This register indicates filled data size in the RX FIFO.	RO	0x00

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- VSPMUX (VOICE SOURCE PATH MUX CONTROL REGISTER, 0x277F)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved.	RO	0
2:0	VSPMUX	When VSPMUX register is set to '2', UART1 FIFO size is changed 128-entry. Otherwise, UART1 FIFO size is 16-entry. The detailed information is in the Voice Part.	R/W	0

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8.8 SPI MASTER/SLAVE

During an SPI transmission, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The operation is different in either Master mode or Slave mode

In the Master mode, the data transmission is done by writing to the SPDR (SPI Data Register, 0x2542).

After transmission, data reception is initiated by a byte transmitted to the Slave device from the Master SPI clock. When the SPI interrupt occurs, the value of the SPDR register becomes the received data from the SPI slave device. Even though the SPDR TX and RX have the same address, no data collision occurs because the processes of writing and reading data happen sequentially.

In the Slave mode, the data must be ready in the SPDR when the Master calls for it. Data transmission is accomplished by writing to the SPDR before the SPI clock is generated by the Master. When the Master generates the SPI clock, the data in the SPDR of the Slave is transferred to the Master. If the SPDR in the Slave is empty, no data exchange occurs. Data reception is done by reading the SPDR when the next SPI interrupt occurs.
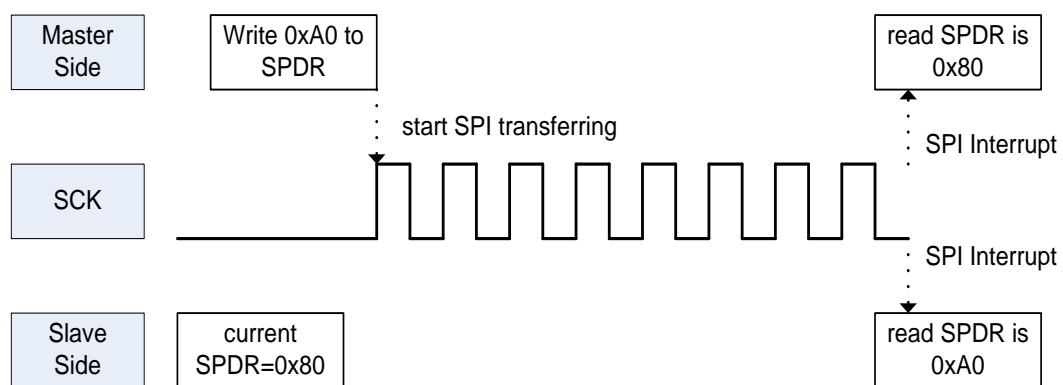
Figure 16. SPI Data Transfer

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- SPCR (SPI CONTROL REGISTER, 0x2540)

Bit	Name	Descriptions	R/W	Reset Value
7	SPIE	SPI Interrupt Enable. When this field is set to '1', SPI interrupt is enabled.	R/W	0
6	SPE	SPI Enable. When this field is set to '1', SPI is enabled.	R/W	0
5		Reserved		0
4	MSTR	Master Mode Select. When this field is set to '1', a Master mode is selected.	R/W	1
3	CPOL	Clock Polarity. If there is no data transmission while this field is set to '0', SCK pin retains '0'. If there is no data transmission while this field is set to '1', SCK pin retains '1'. This field is used to set the clock and data between a Master and Slave with CPHA field. Refer to the below for a more detailed explanation.	R/W	0
2	CPHA	Clock Phase. This field is used to set the clock and data between a Master and Slave with CPOL field.	R/W	0
1:0	SPR	SPI Clock Rate Select. With ESPR field in SPER register(0x2543), selects SPI clock(SCK) rate when the device is configured as a Master. Refer to the ESPR field below.	R/W	0

There are four methods of data transfer based on the settings of CPOL and CPHA. Polarity of SPI serial clock(SCK) is determined by CPOL value and it determines whether SCK activates high or low.

If CPOL value is '0', SCK pin retains '0' during no data transmission. If CPOL value is '1', SCK pin retains '1' during no data transmission. CPHA field determines the format of data to be transmitted.

The table below describes the clock polarity and the data transition timing.

| CPOL	CPHA	SCK when idle	Data Transition Timing
0	0	Low	Falling Edge of SCK
0	1	Low	Rising Edge of SCK
1	0	High	Rising Edge of SCK
1	1	High	Falling Edge of SCK

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The following describes this block when slave mode is selected. When the values of CPOL and CPHA are the same, (a) and (b) below, output data is changed at the falling edge of SCK. Input data is captured at the rising edge of SCK. When the CPOL and CPHA values are different, (b) and (c) below, output data is changed at the rising edge of received SCK. Input data is captured at the falling edge of SCK.
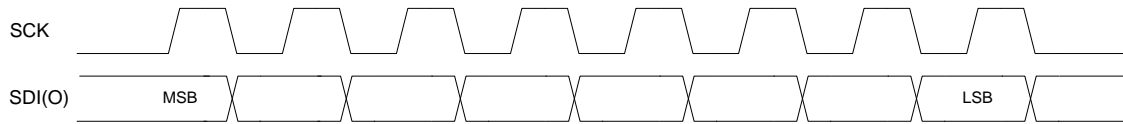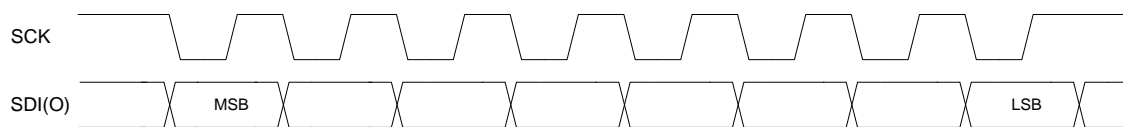
(a) CPOL=0, CPHA=0
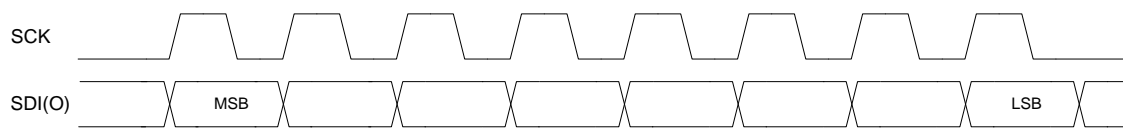
(b) CPOL=0, CPHA=1
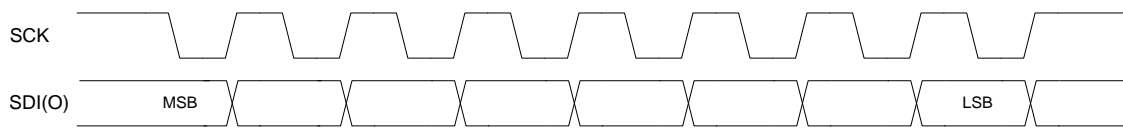
(c) CPOL=1, CPHA=0

(d) CPOL=1, CPHA=1

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- SPSR (SPI STATUS REGISTER, 0x2541)

Bit	Name	Descriptions	R/W	Reset Value
7	SPIF	SPI Interrupt Flag. When SPI interrupt occurs, this field is set to '1'. Set whenever data transmission is finished and it can be cleared by software.	R/W	0
6	WCOL	Write Collision. This field is set to '1' when writing data to the SPDR register while SPITX FIFO is full. It can be cleared by software.	R/W	0
5:4		Reserved		0
3	WFFUL	Write FIFO Full. This field is set to '1' when Write FIFO is full. This field is read only.	RO	0
2	WFEMPTY	Write FIFO Empty. This field is set to '1' when Write FIFO is cleared. This field is read only.	RO	1
1	RFFUL	Read FIFO Full. This field is set to '1' when Read FIFO is full. This field is read only.	RO	0
0	RFEMPTY	Read FIFO Empty. This field is set to '1' when Read FIFO is cleared. This field is read only.	RO	1

- SPDR (SPI DATA REGISTER, 0x2542)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SPDR	This register is read/write buffer.	R/W	-

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- SPER (SPI E REGISTER, 0x2543)

Bit	Name	Descriptions	R/W	Reset Value
7:6	ICNT	Interrupt Count. This field indicates the number of byte to transmit. SPIF bit is set to '1' whenever each byte is transmitted.	R/W	0
5:2		Reserved		0
1:0	ESPR	Extended SPI Clock Rate Select. With SPR field in SPCR Register (0x2540), this field selects SPI clock (SCK) rate when a device is configured as a Master. {ESPR, SPR} / (System Clock Divider): 0000 — Reserved 0001 — Reserved 0010 — 8 0011 — 32 0100 — 64 0101 — 16 0110 — 128 0111 — 256 1000 — 512 1001 — 1024 1010 — 2048 1011 — 4096 * ESPR field : high bit SPR field: low bit	R/W	2

The value of ESPR and SPR is used to divide system clock to generate SPI clock (SCK).

For example, if the value of ESPR and SPR is '0010' and system clock is 8MHz, SPI clock (SCK) is 1MHz.

- VSPMUX (VOICE SOURCE PATH MUX CONTROL REGISTER, 0x277F)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved.	R/W	0
2:0	VSPMUX	When VSPMUX register set to '3'. SPI FIFO size is changed 256 entries. Otherwise, SPI FIFO size is 16 entries. The detailed information is in the Voice Part.	R/W	0

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8.9 I2C MASTER/SLAVE

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.

Devices controlling the buses are called as Master. Master is responsible for generation of bus control and synchronizing signals. Slaves just follow the Master. Any I2C device can be either receiver or transmitter.   The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

I2C core serves both as I2C compatible master and slave. This core supports the following functionalities:

- Both Master and slave operation
- Both Interrupt and non interrupt data-transfers
- Start/Stop generation
- Software programmable acknowledge bit
- Software programmable time out feature
- programmable address register
- Programmable SCL frequency
- Soft reset of I2C Master/Salve
- Programmable maximum SCL low period

- I2C_PRER (I2C PRESCALER REGISTER, 0x2794)

I2C_PRER is used to pre-scale the SCL clock line.

Bit	Name	Descriptions	R/W	Reset Value
7:0	PRER	Prescaler for Master SCL generation	R/W	0x10

I2C Maximum Transmission Rate

f_{SCL} = fsys /(I2C_PRER*2+4) (fsys : I2C block system clock, default 8MHz)

The 4 extra cycles are for clock synchronization and the LOW to HIGH transition of SCL can be delayed if the device with the longest LOW period of SCL line is connected to the I2C bus.

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- I2C_CTR (I2C CONTROL REGISTER, 0x2792)

Bit	Name	Descriptions	R/W	Reset Value
7	CENB	I2C Core Enable(0:enabled, 1:disabled)	R/W	1
6	INTE	Interrupt Enable (1:enabled, 0:disabled)	R/W	0
5	MS	I2C Mode Selection(1: Master, 0:Slave)	R/W	0
4	START/STOP	Select the START/STOP condition generation under the master mode. Changing this bit from 0 to 1, START condition is generated. Changing this bit from 1 to 0, STOP condition is generated.	R/W	0
3	REP_ST	When set to 1, a repeated START condition is generated. If master wish to make another transfer immediately after the current, it can start a new transfer directly by transmitting a repeated START condition instead of a STOP followed by a START. Please refer to [Figure 16] below.	R/W	0
2	NACK_GEN	NACK Generate	R/W	0
1	RXFIFO_RST	Receive FIFO Reset. Auto Clear	R/W	0
0	TXFIFO_RST	Transmit FIFO Reset. Auto Clear	R/W	0

I2C single byte write, then repeated start and single byte read.

The identifiers used are:

- ADDR- Address

- DATA – Data

- S – Start bit

- Sr – Repeated start bit

- P – Stop bit

- W/R- Read(1)/ Write(0)

- A – ACK

- N – NACK

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Figure 17. I2C single byte write, then repeated start and single byte read

- I2C_DAT (I2C TRASMIT/RECEIVE DATA REGISTER, 0x2790)

Bit	Name	Descriptions	R/W	Reset Value
7:0	I2C_DAT	Read only for received data. write only for send data	R/W	-

- I2C_ADDR (I2C SLAVE ADDRESS REGISTER, 0x2791)

Bit	Name	Descriptions	R/W	Reset Value
7:0	I2C_ADDR	Slave Address	R/W	0xFF

- I2C_STR (I2C INTERRUPT FLAG/STATUS REGISTER, 0x2793)

Bit	Name	Descriptions	R/W	Reset Value
7	ADDRESSED	Addressed flag This bit will be set when address of the I2C matches the I2C_ADDR register in the slave mode or when a slave address is sent under the master mode. At read, this bit is cleared.	RO	0
6	MNACKED	Mastered Nacked flag This bit indicates that I2C core detects the non-acknowledgement signal during the acknowledge clock pulse in the master mode. At read, this bit is cleared.	RO	0
5	SNACKED	Slave Nacked Flag This bit indicates that I2C core detects the non-acknowledgement signal during the acknowledge clock pulse in the slave mode. At read, this bit is cleared.	RO	0
4	FINT	FIFO Interrupt flag For the kinds of this flag, please refer to the I2C_FINTVAL (0x279E) register.	RO	0
3	BBUSY	Bus Busy flag This indicates that I2C transfer is in progress and bus in not free. This bit will be set on detection of START condition and will be	RO	0

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Bit	Name	Descriptions	R/W	Reset Value
		cleared on STOP condition. At read, this bit is cleared.		
2	BTRANS	Byte Transferred flag This bit indicates that one byte of data is being transferred. This bit will be 1 only after all 8bits is sent. (1: Byte transfer completed, 0: Byte transfer in progress) At read, this bit is cleared.	RO	0
1		Reserved		
0	TO	Time Out	RO	0

- I2C_HOLD (I2C SCL/SDA HOLD CYCLE REGISTER, 0x2795)

Bit	Name	Descriptions	R/W	Reset Value
7:4	CHOLD	SCL Hold Cycles	R/W	0
3:0	DHOLD	SDA Hold Cycles	R/W	0

- I2C_TO (I2C TIME-OUT REGISTER, 0x2796)

This register is for detecting the SCL clock low timeout condition.

Bit	Name	Descriptions	R/W	Reset Value
7:0	TO	Time-Out Value	R/W	0xFF

If the current state of SCL stays LOW for a time period greater than time-out value set by I2C_TO register when transfer on the bus is active, the internal time-out reset is generated and the internal state of the I2C is reset, terminating any ongoing transfers. When this register value is 0xFF, the time-out function of SCL line is disabled.

- I2C_RXLVL (I2C RX FIFO INTERRUPT LEVEL REGISTER, 0x2797)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RXLVL	RX FIFO Level Interrupt High Threshold	R/W	0

- I2C_RXCNT (I2C RX FIFO CURRENT LEVEL REGISTER, 0x2798)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RXCNT	RX FIFO Current Level	R/W	0

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- I2C_RXSTS (I2C RX FIFO STATUS REGISTER, 0x2799)

Bit	Name	Descriptions	R/W	Reset Value
7:6		Reserved		2'b00
5	OVF	RX FIFO Overflow	RO	0
4	FULL	RX FIFO Full	RO	0
3	LVL	RX FIFO Level Hit (RXCNT >= RXLVL)	RO	0
2	EMPT	RX FIFO Empty	RO	1
1	UDF	RX FIFO Underflow	RO	0
0	EMPT	RX FIFO Empty	RO	1

- I2C_TXLVL (I2C TX FIFO INTERRUPT LEVEL REGISTER, 0x279A)

Bit	Name	Descriptions	R/W	Reset Value
7:0	TXLVL	TX FIFO Level Interrupt Low Threshold	R/W	0

- I2C_TXCNT (I2C TX FIFO CURRENT LEVEL REGISTER, 0x279B)

Bit	Name	Descriptions	R/W	Reset Value
7:0	TXCNT	TX FIFO Current Level	R/W	0

- I2C_TXSTS (I2C TX FIFO STATUS REGISTER, 0x279C)

Bit	Name	Descriptions	R/W	Reset Value
7:6		Reserved		2'b00
5	OVF	TX FIFO Overflow	RO	0
4	FULL	TX FIFO Full	RO	0
3	LVL	TX FIFO Level Hit (TXCNT <= TXLVL)	RO	0
2	EMPT	TX FIFO Empty	RO	1
1	UDF	TX FIFO Underflow	RO	0
0	EMPT	TX FIFO Empty	RO	1

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- I2C_FINTMSK (I2C FIFO INTERRUPT MASK REGISTER, 0x279D)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	-	-
3	TXLVL	TX FIFO Level Interrupt Mask. When zero, The Interrupt is masked	R/W	0
2	TXEMPT	TX FIFO Empty Interrupt Mask. When zero, The Interrupt is masked	R/W	0
1	RXLVL	RX FIFO Level Interrupt Mask. When zero, The Interrupt is masked	R/W	0
0	RXRDA	RX FIFO Data Available Interrupt Mask. When zero, The Interrupt is masked	R/W	0

- I2C_FINTVAL (I2C FIFO INTERRUPT FLAG REGISTER, 0x279E)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	-	-
3	TXLVL	TX FIFO Level Interrupt Flag. At read, this bit is cleared.	RO	0
2	TXEMPT	TX FIFO Empty Interrupt Flag. At read, this bit is cleared.	RO	0
1	RXLVL	RX FIFO Level Interrupt Flag. At read, this bit is cleared.	RO	0
0	RXRDA	RX FIFO Data Available Interrupt Flag. At read, this bit is cleared.	RO	0

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- I2C_IMSK (I2C INTERRUPT MASK REGISTER, 0x279F)

Bit	Name	Descriptions	R/W	Reset Value
7	ADDRESSED	Addressed Interrupt Mask. When zero, The Interrupt is masked	R/W	0
6	MNacked	Master Nacked Interrupt Mask. When zero, The Interrupt is masked	R/W	0
5	SNacked	Slave Nacked Interrupt Mask. When zero, The Interrupt is masked	R/W	0
4	FINT	FIFO Level Interrupt Mask. When zero, The Interrupt is masked	R/W	0
3	BBUSY	Bus Busy Interrupt Mask. When zero, The Interrupt is masked	R/W	0
2	BTRANS	Byte Transfer Completed Interrupt Mask. When zero, The Interrupt is masked	R/W	0
1		Reserved		
0	TO	Time Out Interrupt Mask. When zero, The Interrupt is masked	R/W	0

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8.10 IR(Infra-Red) Modulator

Embedded IR Modulator can support NEC PPM (Pulse Position Modulation) format transfer. The carrier duration and duty rate can be set by PPM_TCCNT, PPM_HCCNT. The data bit generation and the duty rate are set by PPM_T0CNT, PPM_H0CNT for bit pattern 0, and by PPM_T1CNT, PPM_H1CNT for bit pattern 1. The bit generation clock is generated by CDIV divisor.

$$Carrier\_Freq = \frac{fsystem}{TCCNT}$$

$$Carrier\_Duty = \frac{HCCNT}{TCCNT}$$

$$Bit0\_Duration = \frac{T0CNT * CDIV}{fsystem}$$

$$Bit0\_Duty = \frac{H0CNT}{T0CNT}$$

$$Bit1\_Duration = \frac{T1CNT * CDIV}{fsystem}$$

$$Bit1\_Duty = \frac{H1CNT}{T1CNT}$$

LCODE (PPM LEADER CODE REGISTER, 0x27A0)

Bit	Name	Descriptions	R/W	Reset Value
7:0	LCODE	This register is read/write buffer.	R/W	0x0F

PPM_SCODE (PPM STOP CODE REGISTER, 0x27A1)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SCODE	This register is read/write buffer.	R/W	0x00

PPM_CCODE (PPM CUSTOM CODE REGISTER, 0x27A2)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CCODE	This register is read/write buffer.	R/W	0x00

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PPM_CCODB (PPM CUSTOM CODE BAR REGISTER, 0x27A3)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CCODB	This register is read/write buffer.	R/W	0xFF

PPM_DCODE (PPM DATA CODE REGISTER, 0x27A4)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CCODE	This register is read/write buffer.	R/W	0x00

PPM_DCODB (PPM DATA CODE BAR REGISTER, 0x27A5)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CCODB	This register is read/write buffer.	R/W	0xFF

PPM_CTL (PPM CONTROL REGISTER, 0x27A6)

Bit	Name	Descriptions	R/W	Reset Value
7	EN	This register is read/write buffer.	R/W	0
6	DONE	TX Done.	RO	0
5	OE	Output Pin Enable	R/W	0
4	CONT	CONT generation	R/W	0
3	CPCC	Copy Custom Code Bar from PPM_CCODE register value	R/W	1
2	IVCC	Invert PPM_CCODE when CPCC=1	R/W	1
1	CPDC	Copy Custom Data Bar from PPM_DCODE register value	R/W	1
0	IVDC	Invert PPM_DCODE when CPDC=1	R/W	1

PPM_POSST (PPM DATA START POSITION REGISTER, 0x27A7)

Bit	Name	Descriptions	R/W	Reset Value
7:0	POSST	TX Start Bit Position	R/W	0x08

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PPM_POSSP (PPM DATA STOP POSITION REGISTER, 0x27A8)

Bit	Name	Descriptions	R/W	Reset Value
7:0	POSSP	TX Stop Bit Position	R/W	0x29

PPM_TCCNT0 (PPM CARRIER DURATION COUNTER REGISTER, 0x27A9)

Bit	Name	Descriptions	R/W	Reset Value
7:0	TCCNT	PPM Carrier Duration Generation Counter. LSB Part	R/W	0x4A

PPM_TCCNT1 (PPM CARRIER DURATION COUNTER REGISTER, 0x27AA)

Bit	Name	Descriptions	R/W	Reset Value
15:8	TCCNT	PPM Carrier Duration Generation Counter. LSB Part	R/W	0x03

PPM_HCCNT0 (PPM CARRIER HIGH COUNTER REGISTER, 0x27AB)

Bit	Name	Descriptions	R/W	Reset Value
7:0	HCCNT	PPM Carrier High Duration Counter. LSB Part	R/W	0x18

PPM_HCCNT1 (PPM CARRIER HIGH COUNTER REGISTER, 0x27AC)

Bit	Name	Descriptions	R/W	Reset Value
15:8	HCCNT	PPM Carrier High Duration Counter. MSB Part.	R/W	0x01

PPM_T0CNT (PPM BIT0 DURATION COUNTER REGISTER, 0x27AD)

Bit	Name	Descriptions	R/W	Reset Value
7:0	T0CNT	PPM Data Bit Pattern 0 Duration Counter	R/W	0x20

PPM_T1CNT (PPM BIT1 DURATION COUNTER REGISTER, 0x27AE)

Bit	Name	Descriptions	R/W	Reset Value
7:0	T1CNT	PPM Data Bit Pattern 1 Duration Counter	R/W	0x40

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PPM_H0CNT (PPM DATA CODE BAR REGISTER, 0x27AF)

Bit	Name	Descriptions	R/W	Reset Value
7:0	H0CNT	PPM Data Bit Pattern 0 High Duration Counter	R/W	x010

PPM_H1CNT (PPM DATA CODE BAR REGISTER, 0x27B0)

Bit	Name	Descriptions	R/W	Reset Value
7:0	H1CNT	PPM Data Bit Pattern 1 High Duration	R/W	0x10

PPM_CDIV0 (PPM DATA BAUDRATE DIVISOR REGISTER, 0x27B1)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CDIV0	PPM Data Baud-rate Generate Divisor. LSB Part	R/W	0x65

PPM_CDIV1 (PPM DATA BAUDRATE DIVISIOR REGISTER, 0x27B2)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CDIV1	PPM Data Baud-rate Generate Divisor. MSB Part	R/W	0x04

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8.11 VOICE

A voice function includes the following:

- I2S Interface
- Voice Encoder/Decoder (u-law / a-law / ADPCM)
- Voice FIFO
- Direct Path

The data generated through an external ADC is input to the voice block in the MG2475 via an I2S interface. Data received via I2S is compressed at the voice encoder, and stored in the Voice TXFIFO. The data is then transferred to the MAC TX FIFO through direct path and finally transmitted through the PHY layer.

By contrast, received data in the MAC RX FIFO is transferred to the Voice RXFIFO and decompressed in the voice decoder. It is finally transferred to an external DAC via I2S interface.

I2S is commonly used for transferring/receiving voice data. As well, voice data can be transferred or received via SPI or UART interface as well.

Voice encoder/decoder supports u-law, a-law and ADPCM methods.

If the voice encoder/decoder function is not needed, it can be bypassed.

8.11.1 I2S

In I2S interface, data is transferred MSB first from the left channel, and then from the right channel. There are two ways to send data via I2S TX: writing data to the register by software, or by hardware. This is enabled by using POP field in STXMODE (0x252d). Similarly, there are two ways to receive data via I2S RX: the first is reading the register by software, and the other is by the PUSH field in SRXMODE (0x253d).

There are four methods in I2S interface as follows;

- I2S mode
- Left Justified mode
- Right Justified mode
- DSP mode

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In I2S mode, left channel data is transferred in order. When left channel data is transferred, LRCK value is '0' and when right channel data is transferred, LRCK value is '1'. Transferred data and LRCK is changed at the falling edge. Refer to the (a) below.

In Left Justified mode, left channel data is transferred whenever LRCK=1 and right channel data is transferred, whenever LRCK=0. LRCK is changed at the falling edge of BLCK. Transferred data is changed at the rising edge of BCLK. Refer to the (b) below.

In Right Justified mode, left channel data allows last LSB to be output before LRCK value goes to '0' and right channel data allows last LSB to be output before LRCK value goes to '1'.

LRCK value is changed at the falling edge of BCLK. Output data is changed at the rising edge of BCLK. Refer to the (c) below.

In DSP mode, after LRCK outputs to '1' for one period of BCLK, it goes to '0'. After that, left channel data is outputted and then right channel data is outputted. LRCK value is changed at the falling edge of BCLK. Output data is changed at the rising edge of BCLK. Refer to the (d) below.

The following shows the interface method for each mode and I2S TX block is selected as Master. The setting of register is as follows. MS field in STXAIC (0x2528) register is set to '1'. WL field is set to '0'(The data of left and right channel represents 16-bit).

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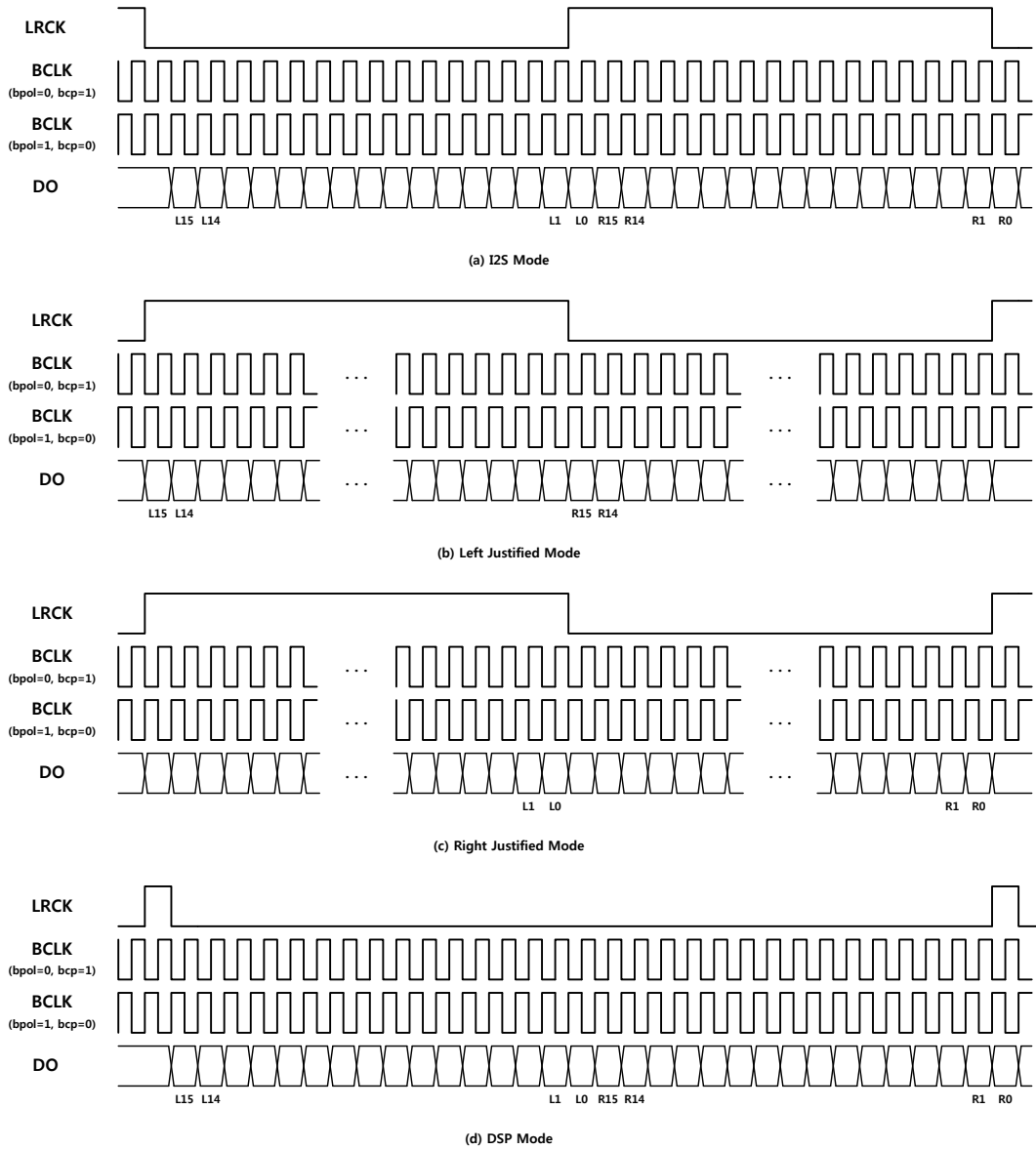
Figure 18. Four Methods in I2S Interface

- STXAIC (I2S TX INTERFACE CONTROL REGISTER, 0x2528)

Bit	Name	Descriptions	R/W	Reset Value
7	MS	When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured. Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input.	R/W	1
6:5	FMT	Three modes of operation determined by the value of this field below. • 0: I2S mode • 1: Right Justified mode • 2: Left Justified mode • 3: DSP mode	R/W	2
4:3	WL	Word Length. This field indicates the number of bits per channel. • 0: 16 bit • 1: 20 bit • 2: 24 bit • 3: 32 bit	R/W	0
2	LRSWAP	Left/Right Swap. When this field is set to '1', the order of the channel for transmitting data is changed. In other words, the data in a right channel is transmitted first.	R/W	0
1	FRAMEP	When this field is set to '1', the polarity of LRCK is changed. For example, in Left Justified mode, the left channel data is outputted when LRCK=1 and the right channel data is outputted when LRCK=0. However, when this field is set to '1', the right channel data is outputted when LRCK=1 and the left channel data is outputted when LRCK=0.	R/W	0
0	BCP	When this field is set to '1', the polarity of BCLK(Bit Clock) is changed. Clock edge, which allows the data change, is changed.	R/W	0

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- STXSDIV (I2S TX SYSTEM CLOCK DIVISOR REGISTER, 0x252A)

Bit	Name	Descriptions	R/W	Reset Value
7:0	STXSDIV	This register sets the value for dividing a system clock to generate MCLK. The equation is as follows: MCLK = System Clock/(2×STXSDIV) When this field is '0', MCLK is not generated.	R/W	0x00

- STXMDIV (I2S TX MCLK DIVISOR REGISTER, 0x252B)

Bit	Name	Descriptions	R/W	Reset Value
7:0	STXMDIV	This register sets the value for dividing MCLK to generate BCLK. When STXSDIV register value is '1', BCLK = MCLK/STXMDIV. When STXSDIV register value is greater than 2, BCLK = MCLK/(2×STXMDIV). When this register value is '0', BCLK is not generated.	R/W	0x00

- STXBDIV (I2S TX BCLK DIVISOR REGISTER, 0x252C)

Bit	Name	Descriptions	R/W	Reset Value
7:0	STXBDIV	This register sets the value for dividing BCLK to generate LRCK. LRCK = BCLK/(2×STXBDIV). When this register value is '0', LRCK is not generated.	R/W	0x00

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- STXMODE (I2S TX MODE REGISTER, 0x252D)

Bit	Name	Descriptions	R/W	Reset Value
7	CSHR	This field is meaningful when I2STX block acts in a Slave mode. When this field is set to '1', I2S TX block shares the clock of I2S RX block. In other words, the MCLK of the I2S RX block is input to the MCLK of the I2S TX block and BCLK of I2S RX block is input to the BCLK of I2S TX block. As well, LRCK of I2S RX block is input to the LRCK of I2S TX block.	R/W	0
6	MPOL	This field determines the polarity of MCLK. When this field is '0', MCLK signal retains '1'. When this field is '1', MCLK signal retains '0'.	R/W	1
5	BPOL	This field indicates the relationship between BCLK and LRCK. When this field is set to '0', LRCK value is changed at the falling edge of BCLK. When this field is set to '1', LRCK value is changed at the rising edge of BCLK.	R/W	1
4	B16	This field determines bit width to transfer data in voice block to I2S block. When this field is set to '1', data is transferred by 16-bit data format to I2S block. When this field is set to '0', data is transferred by 8-bit data format to I2S block.	R/W	1
3	POP	When this field is set to '1', data is transferred to I2S block. When this field is set to '0', data is not transferred to I2S block.	R/W	1
2:1	MODE	This field sets the mode of transferred data. • 0: BLK Mode. Transfer a '0'. • 1: MRT Mode. Only the data in Right channel is transferred.('0' is transferred in Left channel) • 2: MLT Mode. Only the data in Left channel is transferred.('0' is transferred in Right channel) • 3: STR Mode. All data in Left or Right channel are transferred.	R/W	3
0	CLKENA	Clock Enable. When this field is set to '1', I2S TX is enabled.	R/W	0

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- SRXAIC (I2S RX INTERFACE CONTROL REGISTER, 0x2538)

Bit	Name	Descriptions	R/W	Reset Value
7	MS	When this field is set to '1', Master mode is configured. When this field is set to '0', Slave mode is configured. (When this field is set to '0', FMT filed I2S mode is not supported.) Any device can act as the system master by providing the necessary clock signals. A slave will usually derive its internal clock signal from an external clock input.	R/W	1
6:5	FMT	Three modes determined by the value of this field below. • 0: I2S mode (when MS filed is set to '0', this mode is not supported.) • 1: Right Justified mode • 2: Left Justified mode • 3: DSP mode	R/W	2
4:3	WL	Word Length. This field indicates the number of bit per each channel. • 0: 16 bit • 1: 20 bit • 2: 24 bit • 3: 32 bit	R/W	0
2	LRSWAP	Left/Right Swap. When this field is set to '1', the order of the channel for transmitting data is changed. In other words, the data in a right channel is transmitted first.	R/W	0
1	FRAMEP	When this field is set to '1', the polarity of LRCK is changed. For example, in Left Justified mode(FMT=2), data is stored in the left channel when LRCK=1 and data is stored in the right channel when LRCK=0. However, when this field is set to '1', data is stored in the right channel when LRCK=1 and the data is stored in the left channel when LRCK=0.	R/W	0
0	BCP	When this field is set to '1', the polarity of BCLK(Bit Clock) is changed. Clock edge, which allows the data change, is changed.	R/W	0

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- SRXSDIV (I2S RX SYSTEM CLOCK DIVISOR REGISTER, 0x253A)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRXSDIV	This register sets the value for dividing a system clock to generate MCLK. The equation is as follows: MCLK = System Clock/(2× SRXSDIV) When this field is '0', MCLK is not generated.	R/W	0x00

- SRXMDIV (I2S RX MCLK DIVISOR REGISTER, 0x253B)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRXMDIV	This register sets the value for dividing MCLK to generate BCLK. When SRXSDIV register value is '1', BCLK = MCLK/SRXMDIV. When SRXSDIV register value is greater than 2, BCLK = MCLK/(2×SRXMDIV). When this register value is '0', BCLK is not generated.	R/W	0x00

- SRXBDIV (I2S RX BCLK DIVISOR REGISTER, 0x253C)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRXBDIV	This register sets the value for dividing BCLK to generate LRCK. LRCK = BCLK/(2(SRXBDIV). When this register value is '0', LRCK is not generated.	R/W	0x00

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- SRXMODE (I2S RX MODE REGISTER, 0x253D)

Bit	Name	Descriptions	R/W	Reset Value
7	CSHR	This field is meaningful when I2SRX block acts in a Slave mode. When this field is set to '1', I2S RX block shares the clock of I2S TX block. In other words, MCLK of I2S TX block is input to the MCLK of I2S RX block and BCLK of I2S TX block is input to the BCLK of I2S RX block. As well, LRCK of I2S TX block is input to the LRCK of I2S RX block.	R/W	0
6	MPOL	This field determines the polarity of MCLK. When this field is '0', MCLK signal retains '1'. When this field is '1', MCLK signal retains '0'.	R/W	0
5	BPOL	This field indicates the relationship between BCLK and LRCK. When this field is set to '0', LRCK value is changed at the falling edge of BCLK. When this field is set to '1',LRCK value is changed at the rising edge of BCLK.	R/W	0
4	B16	This field determines bit width to transfer data received from external ADC via I2S interface to voice block. When this field is set to '1', data is transferred by 16-bit data format to voice block. When this field is set to '0', data is transferred by 8-bit data format to voice block.	R/W	0
3	PUSH	When this field is set to '1', data received from external ADC via I2S interface is transferred to voice block. When this field is set to '0', data received from external ADC via I2S interface is not transferred to voice block.	R/W	0
2:1	MODE	This field sets the mode of transferred data. • 0: BLK Mode. Transfer a '0'. • 1: MRT Mode. Only the data in Right channel is transferred.('0' is transferred in Left channel) • 2: MLT Mode. Only the data in Left channel is transferred.('0' is transferred in Right channel) • 3: STR Mode. All data in Left or Right channel are transferred.	R/W	0
0	CLKENA	Clock Enable. When this field is set to '1', I2S RX is enabled.	R/W	0

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8.11.2 VOICE ENCODER/DECODER

MG2475 includes three voice encoder/decoder algorithms.

- μ-law

- a-law

- ADPCM

The μ-law algorithm is a companding algorithm primarily used in the digital telecommunication systems of North America and Japan. As with other companding algorithms, its purpose is to reduce the dynamic range of an audio signal. In the analog domain this can increase the signal-to-noise ratio (SNR) achieved during transmission and in the digital domain, it can reduce the quantization error (hence increasing signal to quantization noise ratio). These SNR improvements can be traded for reduced bandwidth and equivalent SNR instead.

The a-law algorithm is a standard companding algorithm used in European digital communications systems to optimize/modify the dynamic range of an analog signal for digitizing.

The a-law algorithm provides a slightly larger dynamic range than the μ-law at the cost of worse proportional distortion for small signals.

Adaptive DPCM (ADPCM) is a variant of DPCM (Differential (or Delta) pulse-code modulation) that varies the size of the quantization step, to allow further reduction of the required bandwidth for a given signal-to-noise ratio. DPCM encodes the PCM values as differences between the current and the previous value. For audio this type of encoding reduces the number of bits required per sample by about 25% compared to PCM.

In order to control voice encoder/decoder, there are several registers. This section describes the major commonly used registers.   For more detailed information, please contact RadioPulse Inc.

- ENCCTL (VOICE ENCODER CONTROL REGISTER, 0x2745)

Bit	Name	Descriptions	R/W	Reset Value
7:6		Reserved	R/W	0
5	B16	When the bit width of data received to voice encoder is 16-bit, set this field to '1'. When it is 8-bit, set this field to '0'.	R/W	0
4	MUT	Mute Enable. When this field is set to '1', the Mute function is enabled.	R/W	0
3:2	SEL	Encoder Select. Selects voice encoder algorithm. • 0: No Encoding • 1: μ-law	R/W	0

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		• 2: a-law • 3: ADPCM		
1	INI	Encoder Initialize. When this field is set to '1', the pointer in voice encoder is initialized. This field cannot be read.	WO	0
0	ENA	Encoder Enable. When this field is set to '1', voice encoder acts.	R/W	0

- DECCTL (VOICE DECODER CONTROL REGISTER, 0x274D)

Bit	Name	Descriptions	R/W	Reset Value
7	LPB	Loopback Test. When this field is set to '1', Loopback test mode is selected. In this case, the output of voice encoder is connected to the input of voice decoder.	R/W	0
6		Reserved	RO	0
5	B16	The bit width of data which is output from voice decoder is 16-bit, set this field to '1'. When this field is set to '0', the bit width of data which is output from voice decoder is 8-bit.	R/W	0
4	MUT	Mute Enable. When this field is set to '1', Mute function is enabled.	R/W	0
3:2	SEL	Decoder Select. Select voice decoder. • 0: No Decoding • 1: µ-law • 2: a-law • 3: ADPCM	R/W	0
1	INI	When this field is set to '1', the pointer in voice decoder is initialized. This field cannot be read.	WO	0
0	ENA	Decoder Enable. When this field is set to '1', voice decoder enabled.	R/W	0

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8.11.3 VOICE FIFO

Data received via I2S interface is compressed by voice encoder; compressed data is stored in Voice TXFIFO (0x2800~0x287F). The size of Voice TXFIFO is 128 byte.

Data in MAC RXFIFO is transferred through direct path, and stored in Voice RX FIFO (0x2900~0x297F). Data in Voice RXFIFO is decompressed by the voice decoder and transmitted to an external component via I2S. The size of Voice RXFIFO is 128 byte.

VOICE TX FIFO CONTROL

- VTFDAT (VOICE TX FIFO DATA REGISTER, 0x2750)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VTFDAT	When writing data to this register, data is stored in Voice TX FIFO in order. When reading this register, data stored in Voice TX FIFO can be read.	R/W	0x00

- VTFCTL (VOICE TX FIFO CONTROL REGISTER, 0x2752)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0
3	VTDENA	Voice TX Direct Path Transfer Enable. When this field is set to '1', Voice TX Direct Path Transfer is enabled. This field value is cleared automatically.	WO	0
2	MUT	When this field is set to '1', the default mute data by selected codec (ENCCTL.SEL) is transferred instead of data in Voice TX FIFO. This field can be read.	R/W	0
1	CLR	When this field is set to '1', Write pointer and Read pointer of Voice TX FIFO are initialized. The status value of underflow and overflow is initialized.	WO	0
0	INI	When this field is set to '1', all data in Voice TXFIFO is replaced by the value in VTFMUT register.	WO	0

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- VTFRP (VOICE TX FIFO READ POINTER REGISTER, 0x2753)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VTFRP	This register indicates the address of Voice TXFIFO to be read next. Since the size of FIFO is 128 byte, LSB is used to test wrap-around.	R/W	0x00

- VTFWP (VOICE TX FIFO WRITE POINTER REGISTER, 0x2754)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VTFWP	This register indicates the address of Voice TXFIFO to be written next. Since the size of FIFO is 128 byte, LSB is used to test wrap-around.	R/W	0x00

- VTFSTS (VOICE TX FIFO STATUS REGISTER, 0x275A)

Bit	Name	Descriptions	R/W	Reset Value
7:5		Reserved	RO	0
4	ZERO	When INI field in VTFCTL register is set to '1', data in Voice TX FIFO is initialized by data in VTFMUT register. During this initialization is processed, this field is set to '1'. After initialization is finished, this field is set to '0'.	RO	0
3	PSH	This field is set to '1' while pushing data into Voice TX FIFO.	RO	0
2	POP	This field is set to '1' while popping data on Voice TX FIFO.	RO	0
1:0		Reserved	RO	0

- VTDSIZE (VOICE TX DIRECT PATH TRANSFER SIZE REGISTER(VOICE TX FIFO->MAC TX FIFO), 0x275B)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VTDSIZE	Set the data size for Direct Path Transfer operation.	R/W	0x00

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VOICE RX FIFO CONTROL

- VRFDAT (VOICE RX FIFO DATA REGISTER, 0x2760)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VRFDAT	When writing data to this register, data is stored in Voice RX FIFO in order. When reading this register, data stored in Voice RX FIFO can be read.	R/W	0x00

- VRFCTL (VOICE RX FIFO CONTROL REGISTER, 0x2762)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0
3	VRDENA	Voice RX Direct Paht Transfer Enable. When this field is set to '1', Voice RX Direct Path Transfer is enabled. This field value is cleared automatically	WO	0
2	MUT	When this field is set to '1', the default mute data by selected codec (DECCTL.SEL) is transferred instead of data in the Voice RX FIFO. This field can be read.	R/W	0
1	CLR	When this field is set to '1', Write pointer and Read pointer of Voice RX FIFO are initialized. The status value of underflow and overflow is initialized.	WO	0
0	INI	When this field is set to '1', all data in Voice RXFIFO is replaced by the value in VRFMUT register.	WO	0

- VRFRP (VOICE RX FIFO READ POINTER REGISTER, 0x2763)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VRFRP	This register indicates the address of Voice RXFIFO to be read next. Since the size of FIFO is 128 byte, the LSB is used to test wrap-around.	R/W	0x00

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- VRFWP (VOICE RX FIFO WRITE POINTER REGISTER, 0x2764)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VRFWP	This register indicates the address of Voice RXFIFO to be written next. Since the size of FIFO is 128 byte, the LSB is used to test wrap-around	R/W	0x00

- VRFSTS (VOICE RX FIFO STATUS REGISTER, 0x276A)

Bit	Name	Descriptions	R/W	Reset Value
7:5		Reserved	RO	0
4	ZERO	When INI field in VRFCTL register is set to '1', data in the Voice TX FIFO is initialized by the data in the VRFMUT register. During the processing of this initialization, this field is set to '1', and set to '0' when initialization is finished.	RO	0
3	PSH	This field is set to '1' while pushing data into the Voice RX FIFO.	RO	0
2	POP	This field is set to '1' while popping data on the Voice RX FIFO.	RO	0
1:0		Reserved	RO	0

- VRDSIZE (VOICE RX DIRECT PATH TRANSFER SIZE REGISTER (MAC RX FIFO->VOICE RX FIFO), 0x276B)

Bit	Name	Descriptions	R/W	Reset Value
7:0	VRDSIZE	Sets the data size for Direct Path Transfer.	R/W	0x00

VOICE INTERFACE CONTROL

- VTFINTENA (VOICE TX FIFO INTERRUPT ENABLE REGISTER, 0x2770)

Bit	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice TX FIFO Empty Interrupt Enable	R/W	0
6	FULL	Voice TX FIFO Full Interrupt Enable	R/W	0
5:0		Should be set as '0'.	R/W	0

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- VRFINTENA (VOICE RX FIFO INTERRUPT ENABLE REGISTER, 0x2771)

Bit	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice RX FIFO Empty Interrupt Enable	R/W	0
6	FULL	Voice RX FIFO Full Interrupt Enable	R/W	0
5:0		Should be set as '0'.	R/W	0

- VDMINTENA (VOICE DIRECT PATH TRANSFER CONTROLLER INTERRUPT ENABLE REGISTER, 0x2772)

Bit	Name	Descriptions	R/W	Reset Value
7:5		Should be set as '0'.	R/W	0
4	VTDDONE	Voice TX Direct Path Transfer Done Interrupt Enable	R/W	0
3:1		Should be set as '0'.	R/W	0
0	VRDDONE	Voice RX Direct Path Transfer Done Interrupt Enable	R/W	0

- VTFINTSRC (VOICE TX FIFO INTERRUPT SOURCE REGISTER, 0x2773)

Bit	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice TX FIFO Empty Interrupt Source. When EMPTY field in VTFINTENA register is set to '1' and EMPTY field in VTFINTVAL register is set to '1', this field is set to '1'. Cleared by software.	R/W	0
6	FULL	Voice TX FIFO Full Interrupt Source	R/W	0
5:0		Reserved	RO	0

- VRFINTSRC (VOICE RX FIFO INTERRUPT SOURCE REGISTER, 0x2774)

Bit	Name	Descriptions	R/W	Reset Value
7	EMPTY	Voice RX FIFO Empty Interrupt Source	R/W	0
6	FULL	Voice RX FIFO Full Interrupt Source	R/W	0
5:0		Reserved	RO	0

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- VDMINTSRC (VOICE DIRECT PATH TRANSFER CONTROLLER INTERRUPT SOURCE REGISTER, 0x2775)

Bit	Name	Descriptions	R/W	Reset Value
7:5		Should be set as '0'.	R/W	0
4	VTDDONE	Voice TX Direct Path Transfer Done Interrupt Source	R/W	0
3:1		Should be set as '0'.	R/W	0
0	VRDDONE	Voice RX Direct Path Transfer Done Interrupt Source	R/W	0

- SRCCTL (VOICE SOURCE CONTROL REGISTER, 0x277A)

Bit	Name	Descriptions	R/W	Reset Value
7		Should be set as '0'.	R/W	0
6:5	MUX	Selects the specific interface to communicate between voice encoder/decoder and external data. • 0: I2S • 1: SPI • 2: UART0 • 3: UART1	R/W	0
4:0		Should be set as '0'.	R/W	0

- VSPCTL (VOICE SOURCE PATH CONTROL REGISTER, 0x277E)

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved	RO	0
6	DECMUT	This register is used to send mute data from voice decoder to the external interface. When this field is set to '1', VSPMUT1 and VSPMUT0 value are transferred to the external interface.	R/W	0
5	DECINI	When using 8-bit external interface, 16-bit data transferred from voice decoder needs to be changed to 8-bit. When this field is set to '1', corresponding control circuit is initialized.	R/W	0
4	DECB16	When using 8-bit external interface such as UART and so on, 16-bit data transferred from voice decoder needs to be changed to 8-bit. When this field is set to '1', high 8-bit data of 16-bit data is transferred first and then low 8-bit data is transferred.	R/W	0
3		Reserved	RO	0

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2	ENCMUT	This register is used to send mute data from external interface to voice encoder. When this field is set to '1', VSPMUT1and VSPMUT0 values are transferred to voice encoder.	R/W	0
1	ENCINI	When using 8-bit external interface, 16-bit data transferred to voice encoder needs to be changed to 16-bit. When this field is set to '1', corresponding control circuit is initialized.	R/W	0
0	ENCB16	When using 8-bit external interface, 8-bit input data needs to be changed to 16-bit, which is compatible with the voice encoder. When this field is set to '1', it is changed to 16-bit.(8-bit received first: high bit 8-bit received later: low bit)	R/W	0

- VSPMUX (VOICE SOURCE PATH MUX CONTROL REGISTER, 0x277F)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved.	RO	0
2:0	VSPMUX	• 0: The 128 bytes Voice RX/TX FIFO mapped to Voice RX/TX FIFO. • 1: Voice RX/TX FIFO mapped to UART0 RX/TX FIFO. • 2: Voice RX/TX FIFO mapped to UART1 RX/TX FIFO. • 3: Voice RX/TX FIFO mapped to SPI RX/TX FIFO. • The others: Not valid	R/W	0

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8.12 Random Number Generator (RNG)

The random number generator (RNG) generates 32-bit random number with seed. Whenever ENA bit in RNGC register is set to '1', the generated number is stored in RNGD3 ~ RNGD0 register.

- RNGD3 (RNG DATA3 REGISTER, 0x2550)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RNGD3	This register stores MSB (RNG[31:24]) of 32-bit random number.	RO	0xB7

- RNGD2 (RNG DATA2 REGISTER, 0x2551)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RNGD2	This register stores 2nd MSB (RNG[23:16]) of 32-bit random number.	RO	0x91

- RNGD1 (RNG DATA1 REGISTER, 0x2552)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RNGD1	This register stores 3rd MSB (RNG[15:8]) of 32-bit random number.	RO	0x69

- RNGD0 (RNG DATA0 REGISTER, 0x2553)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RNGD0	This register stores LSB (RNG[7:0]) of 32-bit random number.	RO	0xC9

- SEED3 (RNG SEED3 REGISTER, 0x2554)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SEED3	This register stores MSB (SEED[31:24]) of required seed to generate random number.	WO	0x00

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- SEED2 (RNG SEED2 REGISTER, 0x2555)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SEED2	This register stores 2nd MSB (SEED[23:16]) of required seed to generate random number.	WO	0x00

- SEED1 (RNG SEED1 REGISTER, 0x2556)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SEED1	This register stores 3rd MSB (SEED[15:8]) of required seed to generate random number.	WO	0x00

- SEED0 (RNG SEED0 REGISTER, 0x2557)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SEED0	This register stores LSB (SEED[7:0]) of required seed to generate random number.	WO	0x00

- RNGC (RNG DATA3 REGISTER, 0x2558)

Bit	Name	Descriptions	R/W	Reset Value
7:1		Reserved	RO	0
0	ENA	RNG Enable. When this field is set to '1', RNG acts. This field value is changed to '0' automatically.	R/W	0

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8.13 Quadrature Signal Decoder

The Quadrature Signal Decoder block notifies the MCU of the counter value based on the direction and movement of a pointing device, such as a mouse, after receiving Quadrature signal from the pointing device.

Quadrature signal is changed with 90° phase difference (1/4 period) between two signals as shown in [Figure 18]. In addition, counter value means 1/4 of one period. Since this block can receive three Quadrature signals, it can support not only the two-dimensional movement such as mouse but also the pointing device which is in three dimensions.

The (a) of [Figure 18] shows that the XA signal is changing before the XB signal. In this case, the pointing device is moving in the down direction. The (b) of [Figure 17] shows that XB signal is changing before XA signal. In this case, the pointing device is moving in the up direction. The rules for YA, YB, ZA and ZB are the same as described above for XA and XB.

(a)

(b)
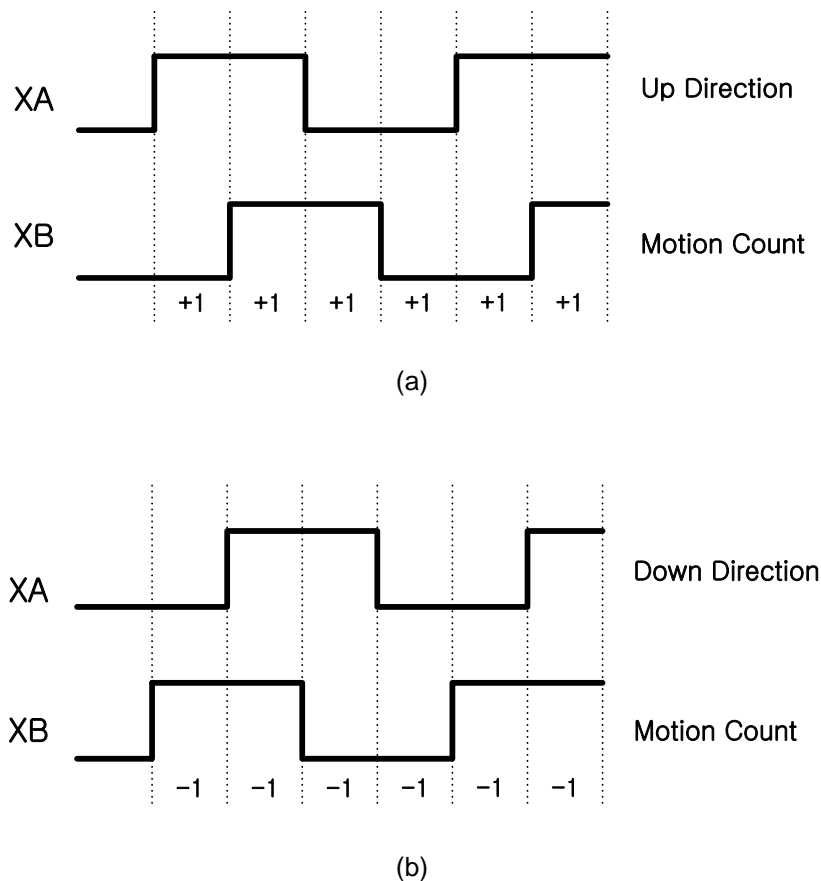
Figure 19. Quadrature signal timing between XA and XB

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- UDX (UpDown X Register, 0x2560)

Bit	Name	Descriptions	R/W	Reset Value
7:1		Reserved	RO	0
0	UPDN_X	This field notifies the MCU of movement in the X-axis direction. 1: Up 0: Down	RO	0

- CNTX (Count X Register, 0x2561)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CNTX	This field notifies the MCU of the count value for movement in the X-axis.	RO	0x00

- UDY (UpDown Y Register, 0x2562)

Bit	**Name**	**Descriptions**	**R/W**	**Reset Value**
7:1		Reserved	RO	0
0	UPDN_Y	This field notifies the MCU of movement in the Y-axis. 1: Up 0: Down	RO	0

- CNTY (Count Y Register, 0x2563)

Bit	**Name**	**Descriptions**	**R/W**	**Reset Value**
7:0	CNTY	This field notifies the MCU of the count value for movement in the Y-axis.	RO	0x00

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- UDZ (UpDown Z Register, 0x2564)

Bit	Name	Descriptions	R/W	Reset Value
7:1		Reserved	RO	0
0	UPDN_Z	This field notifies the MCU of movement in the Z-axis. 1: Up 0: Down	RO	0

- CNTZ (Count Z Register, 0x2565)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CNTZ	This field notifies the MCU of the count value for movement in the Z-axis.	RO	0x00

- QCTL (Quad Control Register, 0x2566)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved	RO	0
2	ENA	Quad Enable. When this field is set to '1', Quadrature Signal Decoder is enabled.	R/W	0
1	INI	Quad Initialize. When this field is set to '1', internal register values of Quadrature Signal Decoder are initialized.	R/W	1
0		Reserved	RO	0

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8.14 ECC (Error Checking and Correction)

The ECC of MG2475 is implemented to maintain the integrity and reliability of memorys, such as flash and data memory. The 24-bit ECC parity code per 512-bytes is generated by ECC logic and stored to the spare area of flash by S/W to do the comparison between the original ECC code and the new generated value after that.   If the values of ECC code are all same, No Error is detected.   If not, the Error is detected. In case of the 1-bit error detecton, the corrupted value can be corrected by 24-bit ECC parity code. Please refer to the below [Figure 20] for the detailed how to use the ECC logic.
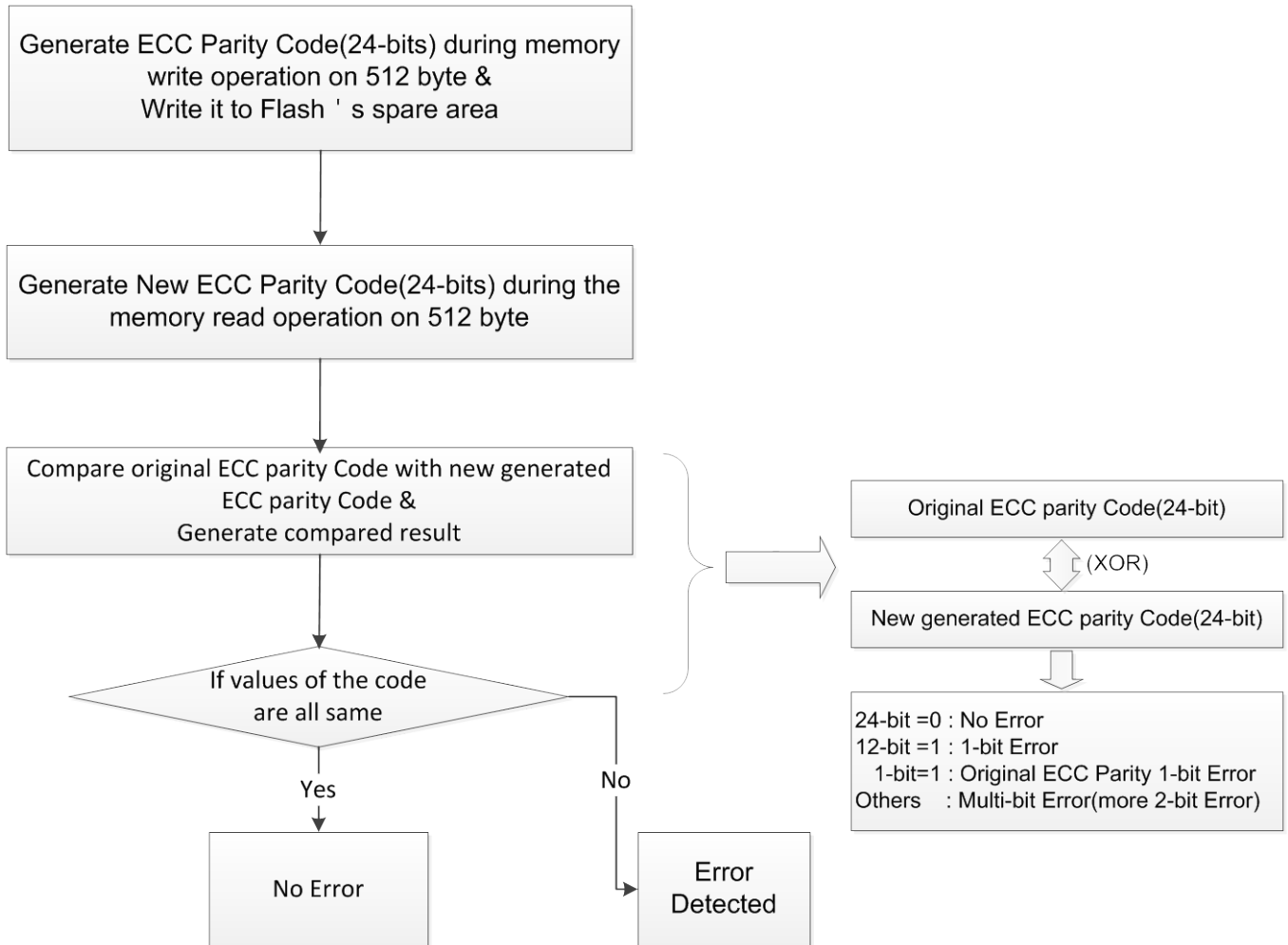
Figure 20. ECC usage flow

8.14.1 Registers Description

For normal operation of ECC logic, the clock of flash controller should be enabled. (The bit 5 of SFR PERI_CLK_STP1(0x99) should be set to 1.)

- ECC_DAT (Data Register for ECC Code Generation, 0x25B0)

Bit	Name	Descriptions	R/W	Reset Value
7:0	ECC_DAT	To calculate the 24-bit ECC parity code, the data should be written to this register on memory access of 512 bytes.	R/W	0

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- ECC_CTL (ECC Cotrol Register, 0x25B1)

Bit	Name	Descriptions	R/W	Reset Value
7:1		Reserved	RO	0
0	ECC_EN	ECC calculation enable/disable bit(1:enabled, 0:disabled)	R/W	0

- ECC_CP (ECC Column Parity Register, 0x25B5)

Bit	Name	Descriptions	R/W	Reset Value
7:0	ECC_CP	Column Parity Register of 24-bits ECC Code ({P4,P4C,P2,P2C,P1,P1C,P2048,P2048C})	RO	0

- ECC_RP1 (ECC Row Parity Register 1, 0x25B6)

Bit	Name	Descriptions	R/W	Reset Value
7:0	ECC_RP1	Row Parity Register 1 of 24-bits ECC Code ({P64,P64C,P32,P32C,P16,P16C,P8,P8C}	RO	0

- ECC_RP2 (ECC Row Parity Register 2, 0x25B7)

Bit	Name	Descriptions	R/W	Reset Value
7:0	ECC_RP2	Row Parity Register 2 of 24-bits ECC Code ({P1024,P1024C,P512,P512C,P256,P256C,P128,P128C})	RO	0

8.14.2 How to correct the 1-bit error

The ECC logic has the capability of correcting error in case of 1-bit error when detecting the memory data is corrupted as follows.

> Stored ECC (in Flash Spare Area)[P2048,P2048C,P1024,…,P2,P2C,P1,P1C]
> **Bitwise XOR**
> Computed data`s ECC result[P2048,P2048C,P1024,…,P2,P2C,P1,P1C]

	No Error	1-bit Error	ECC Parity 1-bit Error	Multi-bits Error
XORed Results	24 bits : 0	12 bits : 1 **NOTE:** Error bit calculation(Byte position is {P2048,P1024,P512,P256,P128,P64,P32, P16,P8} , Bit location is {P4,P2,P1}.)	1 bit : 1	Others

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8.15 General DMA Controller

Direct Memory Access (DMA) can transfer data from a source to a destination without any action by the CPU. The various parameter of a DMA transfer are configured using channel configuration.

- Source address

- Destination address

- Transfer count

- Control

MG2475 has two types of data memory area. SRAM resieds in the address range 0x0000 – 0x1BFF, the register resides in the address range 0x1D00 – 0x2AFF. DMA supports the data transfer from SRAM to register or register to SRAM. It does not support data transfer from SRAM to SRAM or from register to register. It shows at [Figure 21].
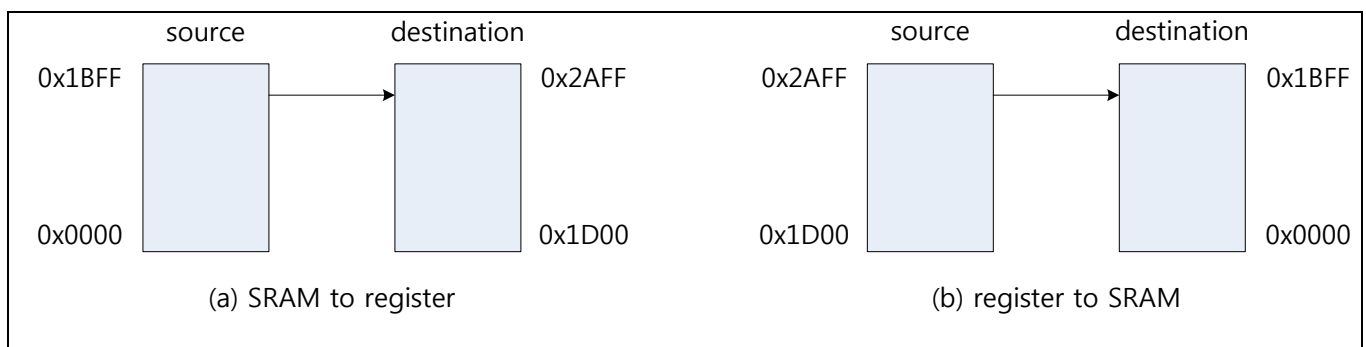
Figure 21. Restriction of address setting

By configuring the SRCINC, DSTINC field of control register(0x27C5, 0x27CD, 0x27D5, 0x27DD), it can perform several types of transfers that can significantly improve processing efficiency for applications that need to move large amounts of data. It shows at [Figure 22].

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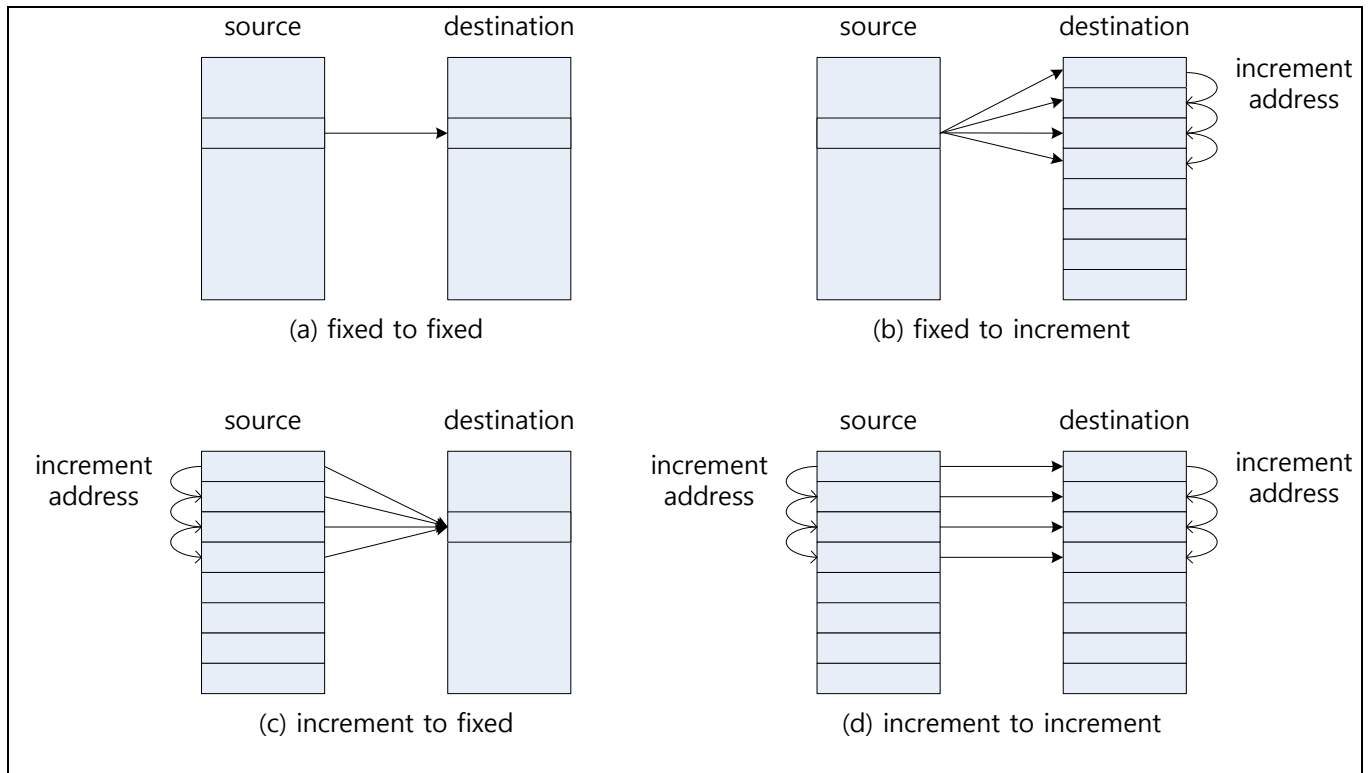
Figure 22. Transfer Type by control setting

The DMA controller manages 4 DMA channel.Each channel contains information such as source address, destination address, transfer count, and control. Each DMA channel has a separate DMA request input that activates a transaction for a particular channel. When multiple DMA channel requests are active, the DMA channels are processed by by DMA controller based on the channel priority. The default priority of each channel that channel 0 is highest, channel 3 is lowest. It is possible to set higher priority using PRIORITY field of each channel control register. [Figure 23] shows the example.

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setting	Priority
Channel 0 PRIORITY = 0	1st
Channel 1 PRIORITY = 0	2nd
Channel 2 PRIORITY = 0	3rd
Channel 3 PRIORITY = 0	4th

(a) example 1

setting	Priority
Channel 0 PRIORITY = 0	3rd
Channel 1 PRIORITY = 1	1st
Channel 2 PRIORITY = 1	2nd
Channel 3 PRIORITY = 0	4th

(b) example 2

setting	Priority
Channel 0 PRIORITY = 0	2nd
Channel 1 PRIORITY = 1	1st
Channel 2 PRIORITY = 0	3rd
Channel 3 PRIORITY = 0	4th

(c) example 3

setting	Priority
Channel 0 PRIORITY = 1	1st
Channel 1 PRIORITY = 1	2nd
Channel 2 PRIORITY = 1	3rd
Channel 3 PRIORITY = 1	4th

(d) example 4

Figure 23. Example of Priority setting

- DMA0_SRCH (DMA Channel 0 Source (MSB) Register, 0x27C0)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[15:8]	R/W	0x21

- DMA0_SRCL (DMA Channel 0 Source (LSB) Register, 0x27C1)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[7:0]	R/W	0x84

- DMA0_DSTH (DMA Channel 0 Source (MSB) Register, 0x27C2)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[15:8]	R/W	0x00

- DMA0_DSTL (DMA Channel 0 Source (LSB) Register, 0x27C3)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[7:0]	R/W	0x00

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- DMA0_CNT (DMA Channel 0 Count Register, 0x27C4)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CNT	Count (1 ~ 256) 0 : transfer count 1 1 : transfer count 2 … 0xFF : transfer count 256	R/W	0x00

- DMA0_CTRL (DMA Channel 0 Control Register, 0x27C5)

Bit	Name	Descriptions	R/W	Reset Value
7:5		Reserved	RO	0
4	IRQEN	Interrupt Enable	R/W	0
3	DSTINC	Destination Address Increment 0 : fixed 1 : increment	R/W	0
2	SRCINC	Source Address Increment 0 : fixed 1 : increment	R/W	0
1	PRIORITY	Priority High 0 : Normal 1 : High	R/W	0
0	ENABLE	Channel Enable	R/W	0

- DMA_STATUS (DMA Status Register, 0x27C7)

Bit	Name	Descriptions	R/W	Reset Value
7	CH3_DONE	Channel 3 Done *Note: To clear the interrupt flag, The 1 must be written into bit[3].	RO	0
6	CH2_DONE	Channel 2 Done *Note: To clear the interrupt flag, The 1 must be written into bit[2].	RO	0
5	CH1_DONE	Channel 1 Done *Note: To clear the interrupt flag, The 1 must be written into bit[1].	RO	0
4	CH0_DONE	Channel 0 Done *Note: To clear the interrupt flag, The 1 must be written into bit[0].	RO	0
3	CH3_IRQ	Channel 3 Interrupt *Note: To clear the interrupt flag, The 1 must be written into this bit.	R/W	0

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2	CH2_IRQ	Channel 2 Interrupt *Note: To clear the interrupt flag, The 1 must be written into this bit.	R/W	0
1	CH1_IRQ	Channel 1 Interrupt *Note: To clear the interrupt flag, The 1 must be written into this bit.	R/W	0
0	CH0_IRQ	Channel 0 Interrupt *Note: To clear the interrupt flag, The 1 must be written into this bit.	R/W	0

- DMA1_SRCH (DMA Channel 1 Source (MSB) Register, 0x27C8)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[15:8]	R/W	0x00

- DMA1_SRCL (DMA Channel 1 Source (LSB) Register, 0x27C9)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[7:0]	R/W	0x00

- DMA1_DSTH (DMA Channel 1 Source (MSB) Register, 0x27CA)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[15:8]	R/W	0x00

- DMA1_DSTL (DMA Channel 1 Source (LSB) Register, 0x27CB)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[7:0]	R/W	0x00

- DMA1_CNT (DMA Channel 1 Count Register, 0x27CC)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CNT	Count (1 ~ 256) 0 : transfer count 1 1 : transfer count 2 … 0xFF : transfer count 256	R/W	0x00

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- DMA1_CTRL (DMA Channel 1 Control Register, 0x27CD)

Bit	Name	Descriptions	R/W	Reset Value
7	PREI_EMPTY	Peripheral Emptry Enable	R/W	0
6	PERI_DONE	Peripheral Done Enable	R/W	0
5	PERI_FULL	Peripheral Full Enable	R/W	0
4	IRQEN	Interrupt Enable	R/W	0
3	DSTINC	Destination Address Increment 0 : fixed 1 : increment	R/W	0
2	SRCINC	Source Address Increment 0 : fixed 1 : increment	R/W	0
1	PRIORITY	Priority High 0 : Normal 1 : High	R/W	0
0	ENABLE	Channel Enable	R/W	0

- DMA1_PERI (DMA Channel 1 Peripheral Mapping Register, 0x27CE)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0x0
3:0	MAP	Peripheral Mapping 0 : UART0 1 : UART1 2 : SPIMS 3 : I2C 4 : MAC 5 : VFIFO 6 : Reserved 7 : Reserved	R/W	0x0

- DMA2_SRCH (DMA Channel 2 Source (MSB) Register, 0x27D0)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[15:8]	R/W	0x00

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- DMA2_SRCL (DMA Channel 2 Source (LSB) Register, 0x27D1)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[7:0]	R/W	0x00

- DMA2_DSTH (DMA Channel 2 Source (MSB) Register, 0x27D2)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[15:8]	R/W	0x00

- DMA2_DSTL (DMA Channel 2 Source (LSB) Register, 0x27D3)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[7:0]	R/W	0x00

- DMA2_CNT (DMA Channel 2 Count Register, 0x27D4)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CNT	Count (1 ~ 256) 0 : transfer count 1 1 : transfer count 2 … 0xFF : transfer count 256	R/W	0x00

- DMA2_CTRL (DMA Channel 2 Control Register, 0x27D5)

Bit	Name	Descriptions	R/W	Reset Value
7	PREI_EMPTY	Peripheral Empty Enable	R/W	0
6	PERI_DONE	Peripheral Done Enable	R/W	0
5	PERI_FULL	Peripheral Full Enable	R/W	0
4	IRQEN	Interrupt Enable	R/W	0
3	DSTINC	Destination Address Increment 0 : fixed 1 : increment	R/W	0
2	SRCINC	Source Address Increment 0 : fixed 1 : increment	R/W	0
1	PRIORITY	Priority High 0 : Normal 1 : High	R/W	0
0	ENABLE	Channel Enable	R/W	0

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- DMA2_PERI (DMA Channel 2 Peripheral Mapping Register, 0x27D6)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0x0
3:0	MAP	Peripheral Mapping 0 : UART0 1 : UART1 2 : SPIMS 3 : I2C 4 : MAC 5 : VFIFO 6 : Reserved 7 : Reserved	R/W	0x0

- DMA3_SRCH (DMA Channel 3 Source (MSB) Register, 0x27D8)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[15:8]	R/W	0x00

- DMA3_SRCL (DMA Channel 3 Source (LSB) Register, 0x27D9)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SRC	Source Address[7:0]	R/W	0x00

- DMA3_DSTH (DMA Channel 3 Source (MSB) Register, 0x27DA)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[15:8]	R/W	0x00

- DMA3_DSTL (DMA Channel 3 Source (LSB) Register, 0x27DB)

Bit	Name	Descriptions	R/W	Reset Value
7:0	DST	Destination Address[7:0]	R/W	0x00

- DMA3_CNT (DMA Channel 3 Count Register, 0x27DC)

Bit	Name	Descriptions	R/W	Reset Value
7:0	CNT	Count (1 ~ 256) 0 : transfer count 1	R/W	0x00

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		1 : transfer count 2 … 0xFF : transfer count 256		

- DMA3_CTRL (DMA Channel 3 Control Register, 0x27DD)

Bit	Name	Descriptions	R/W	Reset Value
7	PREI_EMPTY	Peripheral Emptry Enable	R/W	0
6	PERI_DONE	Peripheral Done Enable	R/W	0
5	PERI_FULL	Peripheral Full Enable	R/W	0
4	IRQEN	Interrupt Enable	R/W	0
3	DSTINC	Destination Address Increment 0 : fixed 1 : increment	R/W	0
2	SRCINC	Source Address Increment 0 : fixed 1 : increment	R/W	0
1	PRIORITY	Priority High 0 : Normal 1 : High	R/W	0
0	ENABLE	Channel Enable	R/W	0

- DMA3_PERI (DMA Channel 3 Peripheral Mapping Register, 0x27DE)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0x0
3:0	MAP	Peripheral Mapping 0 : UART0 1 : UART1 2 : SPIMS 3 : I2C 4 : MAC 5 : VFIFO 6 : Reserved 7 : Reserved	R/W	0x0

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8.16 Security Engine

This security H/W engine is reposible for the data encryption and decryption based on ZigBee and IEEE 802.15.4. Security Controller consists of the block for processing encryption/decryption operation and the block for controlling.

In order to implement CCM* mode by ZigBee and CTR/CBC-MAC/CCM mode by IEEE 802.15.4, 128-bit key value and a nonce are needed. MG2475 can have two 128-bit key values, KEY0 and KEY1. For encryption, the desired nonce value should be stored in the TX Nonce and KEY0 or KEY1 should be selected for use. For decryption, the desired nonce value should be stored in the RX Nonce and KEY0 or KEY1 should be selected for use. For more detailed information, refer to the IEEE802.15.4 standard document.

The SAES_ST (0x2A54) register is used only for AES operation. In this case, required data for this operation should be stored in SAESBUF registers and KEY0 or KEY1 should be selected for use.

The following describes the registers for controlling security block.

- KEY0 (ENCRYPTION KEY 0 REGISTER, 0x2A00~0x2A0F)

Bit	Name	Descriptions	R/W	Reset Value
127:0	KEY0	16-byte key (KEY0) for AES-128 0x2A0F: Most significant byte	R/W	0

- RXNONCE (RX NONCE FOR AUTHENTICATION REGISTER, 0x2A10~0x2A1C)

Bit	Name	Descriptions	R/W	Reset Value
103:0	RXNONCE	Used for decryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter 0x2A1C: Most significant byte of source address 0x2A14: Most significant byte of frame counter 0x2A10: Key sequence counter	R/W	0

- SAESBUF (STANDALONE AES OPERATION BUFFER REGISTERS, 0x2A1D~0x2A2C)

Bit	Name	Descriptions	R/W	Reset Value
7:0	SAESBUF	This register is used for storing data only when processing an AES-128 operation by the AES engine. After the AES-128	R/W	0x00

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		operation, the result is stored in this register. 0x2A2C : MSB of Plaintext and Ciphertext 0x2A1D : LSB of Plaintext and Ciphertext		

- SAES_ST (STANDALONE AES ENCRYPTION OPERATION START REGISTER, 0x2A54)

Bit	Name	Descriptions	R/W	Reset Value
7:1		Reserved		
0	SAES_START	If 1 is written to this bit, the standalone AES encryption operation is started using the SAESBUF registers.	WO	

- KEY1 (ENCRYPTION KEY 1 REGISTER, 0x2A2D~0x2A3C)

Bit	Name	Descriptions	R/W	Reset Value
127:0	KEY1	16-byte key (KEY1) for AES-128 0x2A3C: Most significant byte	R/W	0

- TXNONCE (TX NONCE FOR AUTHENTICATION REGISTER, 0x2A3D~0x2A49)

Bit	Name	Descriptions	R/W	Reset Value
103:0	TXNONCE	Used for encryption: 8-byte source address + 4-byte frame counter + 1-byte key sequence counter 0x2A49: Most significant byte of source address 0x2A41: Most significant byte of frame counter 0x2A3D: Key sequence counter	R/W	0

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- SECCTRL (SECURITY CONTROL REGISTER, 0x2A4A)

Bit	Name	Descriptions	R/W	Reset Value
7	SA_KEYSEL	Selects the KEY value for standalone SAES operation. When this field is '1', KEY1 is selected and when '0', KEY0 is selected.	R/W	0
6	TX_KEYSEL	Selects the KEY value for AES operation during packet transmission. When this field is '1', KEY1 is selected and when '0', KEY0 is selected.	R/W	0
5	RX_KEYSEL	Selects the KEY value for AES operation when packet reception. When this field is '1', KEY1 is selected and when '0', KEY0 is selected.	R/W	0
4:2	SEC_M	In CBC-MAC operation, it represents the data length used in the authentication field in byte. SEC_M / Authentication field length 1 / 4 2 / 6 3 / 8 4 / 10 5 / 12 6 / 14 7 / 16	R/W	0x0
1:0	SEC_MODE	Security mode. 0x0: No security 0x1: CBC-MAC mode 0x2: CTR mode 0x3: CCM mode	R/W	0x0

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- TXL (AES OPERATION LENGTH FOR TRANSMIT PACKET REGISTER, 0x2A4B)

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved	RO	0
6:0	TXL	This field represents the length used in the AES operation for the packet to be transmitted. It has a different meaning for each security mode as follows. • Security mode: CTR It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in memory buffer. • Security mode: CBC-MAC It represents the number of byte between length byte and the data to be authenticated. • Security mode: CCM It represents the length of data which is used not in encoding or decoding but in authentication.	R/W	0

- RXL (AES OPERATION LENGTH FOR RECEIVED PACKET REGISTER, 0x2A4C)

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved	RO	0
6:0	RXL	This field represents the length used in the AES operation for the received packet and it has a different meaning for each security mode as follows. • Security mode: CTR It represents the number of bytes between length byte and the data to be encrypted or decrypted of data in FIFO. • Security mode: CBC-MAC It represents the number of bytes between length byte and the data to be authenticated. • Security mode: CCM It represents the length of data which is used not in encoding or decoding but in authentication.	R/W	0

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- SENC_BASE(SECURITY ENCRYPTION DATA MEMORY BASE ADDRESS REGISTER, 0x2A4E)

Bit	Name	Descriptions	R/W	Reset Value
0	ENC_BASE	It should be set to higher 8-bits value of data memory address for encryption.	R/W	0

- SENC_DATA_LEN(SECURITY ENCRYPTION DATA LENGTH REGISTER, 0x2A4F)

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved		
6:0	SENC_DATA_LEN	It should be set to value that two is added to the data length to be encrypted.	R/W	0

- SDEC_BASE (SECURITY DECRYPTION DATA MEMORY BASE ADDRESS REGISTER, 0x2A51)

Bit	Name	Descriptions	R/W	Reset Value
0	DEC_BASE	It should be set to higher 8-bits value of data memory address for decryption.	R/W	0

- SDEC_DATA_LEN (SECURITY DECRYPTION DATA LENGTH REGISTER, 0x2A52)

Bit	Name	Descriptions	R/W	Reset Value
7		Reserved		
6:0	SDEC_DATA_LEN	It should be set to value that the selected authentication field length and two are added to the data length to be decrypted.	R/W	0

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- SEC_DONE_STS (SECURITY OPERATION DONE STATUS REGISTER, 0x2A53)

Bit	Name	Descriptions	R/W	Reset Value
7:3		Reserved	RO	0
2	SAES_DONE	When the standalone AES operation is finished, this bit is set to 1. It is cleared by writing 1 into this bit.	R/W	0
1	ENC_DONE	When the encryption operation is finished, this bit is set to 1. It is cleared by writing 1 into this bit.	R/W	0
0	DEC_DONE	When the decryption operation is finished, this bit is set to 1. It is cleared by writing 1 into this bit.	R/W	0

- SEC_START (SECURITY OPERATION START STROBE REGISTER, 0x2A55)

Bit	Name	Descriptions	R/W	Reset Value
7:4		Reserved	RO	0xF
3	DEC_START	Decryption operation is started if this bit is set to1, auto cleared	R/W	0
2	ENC_START	Encryption operation is started if this bit is set to 1, auto cleared	R/W	0
1:0		Reserved	RO	0

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8.17 Battery Monitor

MG2475 supports the 7-level battery monitor(3.0V~2.0V, step=0.2V). The battery voltage level can be get using the API, "BATT_GetVoltageLevel". The return value of the API indicates the battery voltage level as below.

- Battery voltage level (For the detailed, refer to the API reference document)

Return value Of BATT_GetVoltageLevel	Battery Voltage
0x00	Voltage >= 3.0
0x01	3.0V > Voltage >= 2.8V
0x02	2.8V > Voltage >= 2.6V
0x03	2.6V > Voltage >= 2.4V
0x04	2.4V > Voltage >= 2.2V
0x05	2.2V > Voltage >= 2.0V
0xFF	2.0V > Voltage

8.18 Power Management

MG2475 has four operation modes to allow low power consumption. PM0 is the normal operating mode. The other 3 modes, PM1/PM2/PM3, are called power down modes.

- PM0

PM0 is the normal operating mode where the RF transceiver, MCU, and peripherals are active. In PM0, all voltage regulators are on.

- PM1

PM1 is the power down mode where the 32MHz crystal oscillator and the 16MHz RC oscillator are powered down. The voltage regulator for digital core, the 32kHz RC oscillator, and the sleep timer are on. MG2475 wakes up from PM1 to PM0 by turning on the 16MHz RC oscillator and the 32MHz crystal oscillator when interrupts are occurred. MG2475 will run on the 16MHz RC oscillator and automatically switch clock source to the 32MHz crystal oscillator after the 32MHz crystal oscillator has settled.

- PM2

PM2 is the power down mode where the 32MHz crystal oscillator, the 16MHz RC oscillator, and the voltage regulator for digital core are powered down. In PM2, the 32kHz RC oscillator and the sleep timer are on. MG2475 wakes up from PM2 to PM0 by turning on the voltage regulator, the 16MHz RC oscillator, and the 32MHz crystal oscillator when interrupts are occurred. Each I/O pins retain the output value set GPIOPS0(0x22E7), GPIOPS1(0x22E8), GPIOPS3(0x22E9), GPIOPE0(0x22EA), GPIOPE1(0x22EB), and GPIOPE3(0x22EC) before entering PM2. PM2 is used when it is relatively long until the expected time for wakeup event.

- PM3

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PM3 is the power down mode where all clock oscillators, the voltage regulator, and sleep timer are powered down. MG2475 wakes up from PM3 to PM0 by turning on the voltage regulator, the 16MHz RC oscillator, and the 32MHz crystal oscillator when interrupts are occurred. Each I/O pins retain the output value set GPIOPS0(0x22E7), GPIOPS1(0x22E8), GPIOPS3(0x22E9), GPIOPE0(0x22EA), GPIOPE1(0x22EB), and GPIOPE3(0x22EC) before entering PM3. PM3 is used to achieve ultra low power consumption.

- Power Management Control

Power down modes (PM1/PM2/PM3) can be set by PDMODE[1:0] in PDCON(0x22E0) register. After setting PDMODE, each power mode can be started by making PCON bit[1] to 1.

MG2475 will wake up from power down modes to PM0 by interrupts, which are the selected I/O pins, the sleep timer, and the external reset.

All I/O pins can be set as wake up source by set GPIOMSK0(0x22F0), GPIOMSK1(0x22F1), and GPIOMSK3(0x22F2) and polarity of the I/O pins can be set by GPIOPOL0(0x22ED), GPIOPOL1(0x22EE), and GPIOPOL3(0x22EF).

Minimum operation time in PM0 must be over 30usec to re-enter into PM1/PM2/PM3.

8.19 Sleep Timer

Sleep timer is used to exit from the power down modes(PM1/PM2/PM3) The desired clock is generated from the 32kHz RC oscillator. The sleep timer is activated as setting STEN bit in PDCON(0x22E0) to 1 and the interrupt interval can be programmed by setting RTINT1(0x22E3), RTINT2(0x22E4), RTINT3(0x22E5), and EXPRTVAL bits in PDMON(0x22E6). Sleep timer interval can be programmed by setting RTCPRD_SEL in PDMON(0x22E6).

Sleep timer can be also used to RTC interrupt source in the normal operation mode(PM0).

When RTCPRD_SEL in PDMON(0x22E6) is set to 1,

Sleep timer interval(sec) is calculated by $65536*EXPRTVAL[1:0] + RTVALSEC[15:0] + 3.904m*RTVALSUB[7:0]$

When the RTCPRD_SEL in PDMON(0x226) is set to 0,

Sleep timer interval(sec) is calculated by $512*EXPRTVAL[1:0] + 7.808m*RTVALSEC[15:0] + 30.5u * RTVALSUB[7:0]$ and minimum sleep timer interval must be over 71usec

8.20 32kHz RC Oscillator

MG2475 has a low-power 32kHz RC oscillator for Sleep timer and watchdog timer. 32kHz RC oscillator is activated when OSC_32K_EN in PDCON(0x22E0[3]) is set to 1. When the 32MHz crystal oscillator is selected and it is stable, i.e. OSCOK in PDMON(0x22E6[6]) is 1, Frequency calibration of the 32kHz RC oscillator is continuously performed by setting OSC_32K_CAL_EN in OSC32K1(0x22B6[2]). This calibration is performed in PM0 and retains the last calibration value in power down mode.

8.21 16MHz RC Oscillator

MG2475 can run on the 16MHz RC oscillator until 32MHz crystal oscillator is stable for fast turn-on time. The

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16MHz RC oscillator is activated when OSC_16M_EN in PDCON(0x22E0) is set to 1. The 16MHz RC oscillator consumes less power than the 32MHz crystal oscillator, but it cannot be used for RF transceiver operation.

8.22 32MHz Crystal Oscillator

The crystal oscillator generates the reference clock for MG2475. An external 32MHz with two loading capacitors (C11 and C12) is used for the 32MHz crystal oscillator. The load capacitance seen by the 32MHz crystal is given by

$$C_L = \frac{1}{\dfrac{1}{C_{11}} + \dfrac{1}{C_{12}}} + C_{parasitic}$$

where $C_{parasitic}$ represents all parasitic capacitances such as PCB stray capacitance and the package pin capacitance.

8.23 Retention Mode

MG2475 can retain the value of the some registers during PM2 and PM3. These registers are restored to the saved value during wakeup, the other registers are reseted. It is possible, depending on the setting of RETENTION_MODE bits(PDMON, 0x22E6), to save or reset value of registers during PM2 and PM3. Table shows the list of registers that is saved.

Address	Name	RETENTION_MODE		
		0x	**11**	**10**
0x1800~ 0x1BFF[Note2]	Data Memory 1KB (0x1800~0x1BFF)	Reset	Reset	Saved
0x0000 ~ 0x17FF	Data Memory 6KB (0x0000~0x17FF)	Reset	Saved	Saved
0x2170 ~ 0x2193	MAC register(ref to Section 9.1.7)	Reset	Saved	Saved
0x2200 ~ 0x22FF	PHY register (ref to Section 0)	Reset	Saved	Saved
SFR 0x00 ~ 0x7F	GPRs 128Byte	Reset	Saved	Saved
SFR 0x80 ~ 0xFF	SFRs [Note1]	Reset	Saved	Saved
SFR 0x87	PCON	Reset	Reset	Reset
SFR 0x91	EXIF1	Reset	Reset	Reset
SFR 0xC0	WCON	Reset	Reset	Reset
SFR 0xD8	EXIF2	Reset	Reset	Reset
SFR 0xED	P0_IRQ_STS	Reset	Reset	Reset
SFR 0xF5	P1_IRQ_STS	Reset	Reset	Reset
SFR 0xFD	P3_IRQ_STS	Reset	Reset	Reset

NOTE: 1 : except (0x87, 0x91, 0xC0, 0xD2, 0xD8, 0xED, 0xF5, 0xFD)

　　　　2: The 0x1800~0x1BFF data memory has the optional power-off feature for flexible low power selection.

8.24 Always-On Registers

All registers bits retain their previous values when entering PM2 or PM3.

- PDCON (POWER DOWN CONTROL REGISTER, 0x22E0)

Bit	Name	Descriptions	R/W	Reset Value
7	BODEN	It enables the Brown out detector (BOD), when DVDD_3V falls under operation voltage. 1: Enables the Brown out detector. 0: Disables the Brown out detector.	R/W	1
6	AVREGEN	It controls voltage regulators in Analog part. It must be set to 0 before entering PM0/PM1/PM2 1: Enables voltage regulators in Analog part. 0: Disables voltage regulators in Analog part.	R/W	1
5	STEN	Register for controlling the sleep timer. When STEN is set to 1, the sleep timer operates by 32kHz RC oscillator. 1: Enables the sleep timer. 0: Disables the sleep timer.	R/W	0
4	OSC_16M_EN	It decides oscillation of the 16MHz RC oscillator. The 16MHz RC oscillator is used for fast turn on from PM1/2/3 or initial power up sequence. 1: Enables the 16MHz RC oscillator. 0: Disables the 16MHz RC oscillator.	R/W	1
3	OSC_32K_EN	It decides oscillation of the 32kHz RC oscillator. Output clock of the 32kHz RC oscillator is used for sleep timer and the watchdog timer. 1: Enables the 32kHz RC oscillator. 0: Disables the 32kHz RC oscillator.	R/W	1
2		Reserved bit (This bit should be zero.)	RO	0
1:0	PDMODE	Register for power down mode of MG2475 00: Normal operation mode 01: PM1 10: PM2 11: PM3	R/W	00

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- RTINT1 (SLEEP TIMER INTERVAL CONTROL REGISTER, 0x22E3)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RTVALSEC[15:8]	This field determines the Sleep timer interval with RTINT2, RTINT3, and EXPRTVAL bits in PDMON.	R/W	0x00

- RTINT2 (SLEEP TIMER INTERVAL CONTROL REGISTER, 0x22E4)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RTVALSEC[7:0]	This field determines the Sleep timer interval with RTINT1, RTINT3, and EXPRTVAL bits in PDMON.	R/W	0x01

- RTINT3 (SLEEP TIMER INTERVAL CONTROL REGISTER, 0x22E5)

Bit	Name	Descriptions	R/W	Reset Value
7:0	RTVALSUB[7:0]	This field determines the Sleep timer interval with RTINT1, RTINT2, and EXPRTVAL bits in PDMON.	R/W	0x00

- PDMON (RC OSCILLATOR CALIBRATION REGISTER, 0x22E6)

Bit	Name	Descriptions	R/W	Reset Value
7	RTCPRD_SEL	This field determines step of the Sleep timer interval 0: 30.5usec 1: 3.904msec	R/W	1
6	OSCOK	32MHz crystal oscillator status: 0: 32MHz crystal oscillator is not yet stable. 1: 32MHz crystal oscillator is stable.	RO	0
5	-	Reserved	RO	000
4:3	EXPRTVAL	This field determines the Sleep timer interval with RTINT1, RTINT2, and RTINT3.	R/W	00
2		Reserved	RO	0
1:0	RETENTION	Retention Mode 0x : No retention, 7KB data memory are off during PM2, PM3. It is not recovered to previous values. 10 : Retention 1, 7KB data memory are always-on during PM2, PM3. 11 : Retention 2, 6KB data memory(0x0000~0x17FF) is always-on during PM2, PM3.	R/W	10

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- GPIOPS0 (PORT 0, PULL-UP/PULL-DOWN SELECT REGISTER, 0x22E7)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO0_PS	This field selects the configuration of Port 0 as pull-up/pull-down inputs 0: pull-down 1: pull-up	R/W	0xFF

- GPIOPS1 (PORT 1, PULL-UP/PULL-DOWN SELECT REGISTER, 0x22E8)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO1_PS	This field selects the configuration of Port 1 as pull-up/pull-down inputs 0: pull-down 1: pull-up	R/W	0xFF

- GPIOPS3 (PORT 3, PULL-UP/PULL-DOWN SELECT REGISTER, 0x22E9)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO3_PS	This field selects the configuration of Port 3 as pull-up/pull-down inputs 0: pull-down 1: pull-up	R/W	0xFF

- GPIOPE0 (PORT 0, INPUT MODE, 0x22EA)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO0_PE	This field selects input mode of the Port 0. 0: tri-state 1: pull-up/pull-down (see GPIOPS0(0x22E7))	R/W	0xFF

- GPIOPE1 (PORT 1, INPUT MODE, 0x22EB)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO1_PE	This field selects input mode of the Port 1. 0: tri-state 1:pull-up/pull-down(see PIOPS0(0x22E8))	R/W	0xFF

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- GPIOPE3 (PORT 3, INPUT MODE, 0x22EC)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO3_PE	This field selects input mode of the Port 3. 0: tri-state 1:pull-up/pull-down(see PIOPS0(0x22E9))	R/W	0xFF

- GPIOPOL0 (PORT 0, INTERRUPT POLARITY, 0x22ED)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO0_POLH	This field changes the polarity of the Port 0. Port 0 is used the wake up source in the PM1/2/3 0: recognizes low level as interrupt signal. 1: recognizes high level as interrupt signal.	R/W	0x00

- GPIOPOL1 (PORT 1, INTERRUPT POLARITY, 0x22EE)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO1_POLH	This field changes the polarity of the Port 1. Port 1 is used the wake up source in the PM1/2/3 0: recognizes low level as interrupt signal. 1: recognizes high level as interrupt signal.	R/W	0x00

- GPIOPOL3 (PORT 3, INTERRUPT POLARITY, 0x22EF)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO3_POLH	This field changes the polarity of the Port 3. Port 3 is used the wake up source in the PM1/2/3 0: recognizes low level as interrupt signal. 1: recognizes high level as interrupt signal.	R/W	0x00

- GPIOMSK0 (PORT 0, INTERRUPT MASK, 0x22F0)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO0_MSK	Port 0 interrupt mask. Port 0 is used the wake up source when this field is set to 1 in PM1/2/3. 0: No interrupt will be acknowledged. 1: Port 0 is individually enabled and Port 0 is used the wake up source.	R/W	0x00

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- GPIOMSK1 (PORT 1, INTERRUPT MASK, 0x22F1)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO1_MSK	Port 1 interrupt mask. Port 1 is used the wake up source when this field is set to 1 in PM1/2/3. 0: No interrupt will be acknowledged. 1: Port 1 is individually enabled and Port 1 is used the wake up source.	R/W	0x00

- GPIOMSK3 (PORT 3, INTERRUPT MASK, 0x22F2)

Bit	Name	Descriptions	R/W	Reset Value
7:0,	GPIO3_MSK	Port 3 interrupt mask. Port 3 is used the wake up source when this field is set to 1 in PM1/2/3. 0: No interrupt will be acknowledged. 1: Port 3 is individually enabled and Port 3 is used the wake up source.	R/W	0x0C

- AONREG0 (Always On Register 0, 0x22F7)

Bit	Name	Descriptions	R/W	Reset Value
7:0,	AONREG0	General Purpose Always On Register	R/W	0x00

- AONREG1 (Always On Register 1, 0x22F8)

Bit	Name	Descriptions	R/W	Reset Value
7:0,	AONREG1	General Purpose Always On Register	R/W	0x00

- GPIOSPU0 (PORT 0, Strong Pull-up , 0x22F9)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO0_SPU	Port 0 Strong pull-up. 0: disable. 1: Port 0 is individually enabled.	R/W	0x00

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- GPIOSPU1 (PORT 1, Strong Pull-up, 0x22FA)

Bit	Name	Descriptions	R/W	Reset Value
7:0	GPIO1_SPU	Port 1 Strong pull-up. 0: disable. 1: Port 1 is individually enabled.	R/W	0x00

- GPIOSPU3 (PORT 3, Strong Pull-up, 0x22FB)

Bit	Name	Descriptions	R/W	Reset Value
7:0,	GPIO3_SPU	Port 3 Strong pull-up. 0: disable. 1: Port 3 is individually enabled.	R/W	0x00

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9 TRANSCEIVER

9.1 MAC

The MAC block transmits the data received from high layer to baseband modem, or encrypts it and then transmits to baseband modem. In addition, it indicates the status of PHY and transmits the data received from baseband modem to high layer, or transmits the decrypted data to high layer.
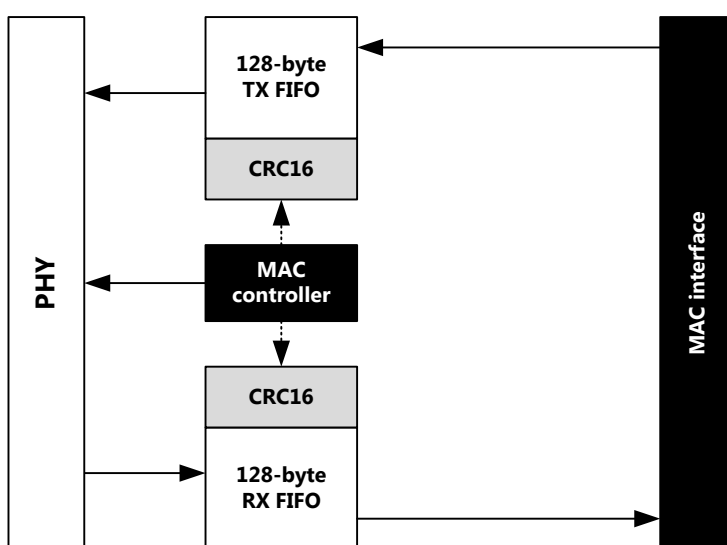
Figure 24. MAC block diagram

[Figure 24] shows the MAC block structure. The RX and TX FIFOs are separately implemented. The size of each FIFO is 128 bytes in order to process one IEEE802.15.4 packet along with buffering one packet. The following table shows the address space of each FIFO.

9.1.1 Dual PAN ID

MG2475 supports Dual PAN mode, allowing the device to exist .on 2 PAN's simultaneously. It includes hardware support for a device to operate in two networks.

PAN0	PAN1
SelPAN0	SelPAN1
PANId0	PANId1
ShortAddress0	ShortAddress1
IEEE address0	IEEE address 1

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- EXTADDR0 (EXTENDED ADDRESS0 REGISTER, 0x2170~0x2177 **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
63:0	EXTADDR0	64-bit IEEE address in PAN0 0x2177: Most significant byte	R/W	0

- PANID0 (PAN0 IDENTIFIER REGISTER, 0x2178~0x2179 **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
15:0	PANID0	16-bit PAN0 ID 0x2179: Most significant byte	R/W	0x2475

- SHORTADDR0 (SHORT ADDRESS0 REGISTER, 0x217A~0x217B **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
15:0	SHORTADDR0	16-bit short (network) address in PAN0 0x217B: Most significant byte	R/W	0

- EXTADDR1 (EXTENDED ADDRESS1 REGISTER, 0x2180~0x2187 **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
63:0	EXTADDR1	64-bit IEEE address in PAN1 0x2187: Most significant byte	R/W	0

- PANID1 (PAN1 IDENTIFIER REGISTER, 0x2188~0x2189 **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
15:0	PANID1	16-bit PAN0 ID 0x2189: Most significant byte	R/W	0x2475

- SHORTADDR1 (SHORT ADDRESS0 REGISTER, 0x218A~0x218B **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
15:0	SHORTADDR1	16-bit short (network) address in PAN1 0x218B: Most significant byte	R/W	0

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- SEL_PAN (PAN SELECTION REGISTER, 0x218C **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
[7:3]		Reserved	RO	0x0
[2]		Reserved	RO	0x1
[1]	SEL_PAN1	When this field is set to '1', data in the TX F1 mode is enabled.	R/W	0
[0]	SEL_PAN0	When this field is set to '1', function for PAN0 mode is enabled.	R/W	1

9.1.2 MAC Control

- MACCTRL (MAC CONTROL REGISTER, 0x2190 **[RETENTION]**)

Bit	Name	Descriptions				R/W	Reset Value
7:6	SEL_CRC_FIELD	2bytes FCS Fields can be replaced by a modem internal status. By receiving a packet, at the end of FCS Fields, Mac Controller substitute internal indicators for FCS value.				R/W	0x0
		Name	**Value**	**FCS [7:0]**	**FCS[15:8]**		
		CRC	0x0	CRC[7:0]	CRC[15:8]		
		RSSI	0x1	RSSI[7:0]	{XCOR[7:1], CRC_OK}		
		DATA RATE	0x2	RSSI[7:0]	{0,DATA_RATE[2:0], MIX_STATUS, LNA_STATUS[1:0], CRC_OK}		
		AMP GAIN	0x3	{RSSI[7:1], MIX_GAIN}	{LNA_STATUS[1:0], VLPF_GAIN[5:0]}		
5	Reserved	Only "0" is allowed					0x0
4	PREVENT_ACK	When this field is set to '1', the RX interrupt will not be generated, if the DSN field of received ACK packet is different from the value in MACDSN register during packet reception.				R/W	0
3	PAN_COORDINATOR	When this field is set to '1', function for PAN coordinator is enabled.				R/W	0
2	ADR_DECODE	When this field is set to '1', the RX interrupt will not be generated if address information of the received packet is not matched with device itself.				R/W	0
1	AUTO_CRC	When this field is set to '1', the RX interrupt will not be generated if the CRC of the received packet is not valid.				R/W	
0	RESEVED	Only "0" is allowed				R/W	1

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- MACDSN (MAC DSN, 0x217C)

Bit	Name	Descriptions	R/W	Reset Value
7:0	MACDSN	If the DSN field of the received ACK packet is not equal to MACDSN, the RX interrupt does not occurred.	R/W	0

9.1.3 MAC Frame Filtering

- FCFRSVD (Frame Control Fields Reserved bits filtering register 0x218D **[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
7:4	FCF_RSVD_VERSION	Frame Control Fields[13:12] bits filtering register During reception, the MAC frame filter parses bit[13:12] of frame control field of the received frame data. if this register bits are set to following values, the recived frame data will be filtered according to below table descrition.<table><tr><th>Bits</th><th>VALUE</th><th>FCF[13:12]</th><th>Description</th></tr><tr><td>[4]</td><td>1</td><td>0x0</td><td>Packet Discard</td></tr><tr><td></td><td>0</td><td>0x0</td><td>Don't care</td></tr><tr><td>[5]</td><td>1</td><td>0x1</td><td>Packet Discard</td></tr><tr><td></td><td>0</td><td>0x1</td><td>Don't care</td></tr><tr><td>[6]</td><td>1</td><td>0x2</td><td>Packet Discard</td></tr><tr><td></td><td>0</td><td>0x2</td><td>Don't care</td></tr><tr><td>[7]</td><td>1</td><td>0x3</td><td>Packet Discard</td></tr><tr><td></td><td>0</td><td>0x3</td><td>Don't care</td></tr></table>	R/W	0xE
3	BYTE_ADDR_CHK			
2:0	FCF_RSVD_789	Frame Control Fields[9:7] bits filtering register During reception, the MAC frame filter parses bit[9:7] of frame control field of the received frame data. if this register bits are set to following values, the recived frame data will be filtered according to below table descrition<table><tr><th>Bit</th><th>Description</th></tr><tr><td>[0]</td><td>1: FCF[7] == 0x1 Packet Discard 0: FCF[7] == 0x1 Don't care</td></tr><tr><td>[1]</td><td>1: FCF[8] == 0x1 Packet Discard 0: FCF[8] == 0x1 Don't care</td></tr><tr><td>[2]</td><td>1: FCF[9] == 0x1 Packet Discard 0: FCF[9] == 0x1 Don't care</td></tr></table>		

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- ADDRFLT1 (Address Filter Register 0x2191**[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
7:5	Reserved	Only "0" allowed	R/W	0x0
4	Reserved	Only "0" allowed	R/W	1
3	DEST_ADDR_MODE	This register enables the frame filtering about addressing mode subfield except for Beacon and Acknowledge frame. If source and destination mode value of received packet is zero, the MAC frame filtering prevents the received frame.	R/W	0
2	SRC_ADDR_MODE	This register enables the frame filtering about addressing mode subfield except for acknowledge frame. If source and destination mode value of received packet is zero, the MAC frame filtering prevents the received frame.	R/W	0
1	DEST_ADDR_RSVD	When this vaule is set to logic one, a MAC Frame Filter prevents the frame with reserved destination addressing mode.	R/W	0
0	SRC_ADDR_RSVD	When this vaule is set to logic one, a MAC Frame filter prevents the frame with reserved source addressing mode.	R/W	0

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- ADDRFLT2 (Address Filter Register 0x2192**[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
7:4	FCF_FRAME_TYPE	This register checks the validity of the frame type subfield in received packet. According to the contents of these register bits, the MAC address filter passes frames with a specific reserved frame type	R/W	0x0
3:0	FCF_BEACON		R/W	0x0

Bit	VALUE	FCF[2:0]	Description
[4]	1	0x4	Packet Discard
	0	0x4	Don't care
[5]	1	0x5	Packet Discard
	0	0x5	Don't care
[6]	1	0x6	Packet Discard
	0	0x6	Don't care
[7]	1	0x7	Packet Discard
	0	0x7	Don't care

Frame Type Value FCF[2:0]	Description
0x0	Beacon
0x1	Data
0x2	Acknowledgement
0x3	MAC command
0x4 ~ 0x7	Reserved

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- ADDRFLT3 (Address Filter Register 0x2193**[RETENTION]**)

Bit	Name	Descriptions	R/W	Reset Value
7:6	Reserved	Only "0" allowed	R/W	0x3
5	MHR_LENGTH_CHEK	When this register is set to logic one, MAC Address filter calculate the minimum packet length of received packet with Frame control field. If a packet Length is smaller than the minimum Length, a received packet will be discarded. [Table 13] shows the way of calculation.about a minimum packet length.	R/W	0x0
4:0	ACK_FCF	This register prevents the reception of a ack frame, if the FCF of received ack packet violates the rule of ACK frame condition. Refer to the following requirements (quote from IEEE 802.15.4, 7.2.2.3.1) **NOTE:** IEEE 802.15.4, section 7.2.2.3.1 Acknowledgement frame MHR fields: The frame pending subfield shall be set according to whether the device sending the acknowledgement frame has more data pending for the receipient. All other subfield shall be set to 0 and ignored on reception.	R/W	0x0

Bit	VALUE	Description
[0]	1	ACK Request Subfield
	0	Don't care
[1]	1	Security Enable Subfield
	0	Don't care
[2]	1	Intra PAN subfield
	0	Don't care
[3]	1	Destination Addressing Mode Subfield
	0	Don't care
[4]	1	Source Addressing Mode Subfield
	0	Don't care

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Table 13. Minimum Packet Length Calculation with FCF

DEST ADDR		SOURCE ADDR		Description
MODE	DestAddr Field Length	MODE	SrcAddr Field Length	AddrMode : 0x2 → PANId(2) + ShortAddr(2) = 4 AddrMode : 0x3 → PANId(2) + ExtendedAddr(8) = 10 N_FCFnCRC = 5
0x2	4	0x2	if(DestMode !=0 and SrcMode != 0 and FrameControl.IntraPAN == 1) 2 else 4	N_MHRField = N_DestField + N_SrcField + N_FCFnCRC
0x3	10	0x3	if(DestMode !=0 and SrcMode != 0 and FrameControl.IntraPAN == 1) 8 else 10	Check [PKT_LNG < N_MHRField] → Error !!
Others	0	Others	0	

- ADDRFLT4 (Address Filter Register 0x2196)

Bit	Name	Descriptions	R/W	Reset Value
7	EXTENDED_ADDR_MODE	This register enables the Extended address decoding and filtering. If desdtination addressing mode is equal to 0x3 and extended address is different with a register value(EXTADDR0, or EXTADDR1), MAC Frame filter prevents the received frame.	R/W	1
6	SHORT_ADDR_MODE	This register enables the short address decoding and filtering. If destination addressing mode is equal to 0x2 and short address is different with a register value (SHORTADDR0, or SHORTADDR1), MAC Frame filter prevents the received frame.	R/W	1
5:0	RX_FIFO_PACKET_CNT	This register contains the number of pending packets in RX FIFO. This number does not indicate the number of rx end pending interrupt. If rx dma operation is completed, this value will be decreased and a rx end interrupt will be generated.	RO	0x0

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- ADDRFLT5 (Address Filter Register 0x2197)

Bit	Name	Descriptions	R/W	Reset Value
7	RESERVED		R/W	0
6	DEST_PANID_MODE	This register enables the Destination PANId filtering. If destination addressing mode is not equal to 0x0 and the PANId of received frame is not matched with the PANId register (PANID0 or PANID1) or 0xFFFF, MAC Frame filter prevents the received frame. 1:enable 0:disable	R/W	1
5:0	RESERVED		R/W	0x0

9.1.4 MAC Header for Voice

MG2475 provides H/W implemented MAC header for voice packet.

Table 14. VOICE MAC HEADER Frame Control Fields

Information contained in this document shall be changed without notice and is presented without express or implied warranty.

Table 15. MAC Header Configuration for transmitting voice packet

Address	Voice Mac Header Description	Description
0x21A0	Total Length(12 or 79)	Vary
0x21A1	TX Option(ACK request On/Off)	Vary
0x21A2	TX Packet Type(Command or Voice)	Vary
0x21A3	DSN	Vary
0x21A4	PAN ID LSB	
0x21A5	PAN ID MSB	
0x21A6	DST Short Address LSB	
0x21A7	DST Short Address MSB	
0x21A8	SRC Short Address LSB	
0x21A9	SRC Short Address MSB	
0x21AA	If(VOICE)Retry TX count Value	Vary
	Else Command data	Vary
0x21AB	If(ADPCM) IMA Predict1 value	Vary
	Else 0x00	
0x21AC	If(ADPCM) IMA Predict0 value	Vary
	Else 0x00	
0x21AD	If(ADPCM) IMA Index value	Vary
	Else 0x00	
MAC TX FIFO	Voice data Payload	

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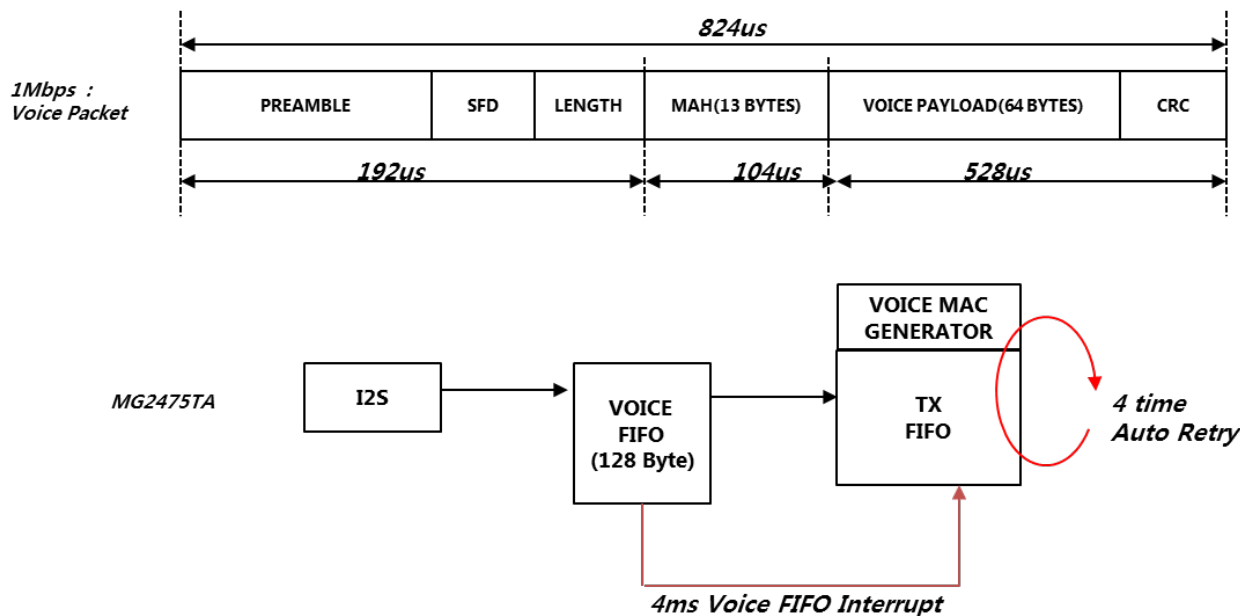
Figure 25. Voice Packet Transmission Block Diagram

- VOICEMAC (MAC header for VOICE packet register 0x21A0 ~ 0x21AF)

NAME	Address	Description	RW	Reset Value
VOICEMAC0	0x21A0	VOICE_LENGTH[7:0]	R/W	0x4F
VOICEMAC1	0x21A1	VOICE_FCF[7:0]	R/W	0x00
VOICEMAC2	0x21A2	VOICE_FCF[15:8]	R/W	0x00
VOICEMAC3	0x21A3	VOICE_DSN[7:0]	R/W	0x00
VOICEMAC4	0x21A4	VOICE_PAN_ID[7:0]	R/W	0x00
VOICEMAC5	0x21A5	VOICE_PAN_ID[15:8]	R/W	0x00
VOICEMAC6	0x21A6	VOICE_DST_SHORT_ADDRESS[7:0]	R/W	0x00
VOICEMAC7	0x21A7	VOICE_DST_SHORT_ADDRESS[15:8]	R/W	0x00
VOICEMAC8	0x21A8	VOICE_SRC_SHORT_ADDRESS[7:0]	R/W	0x00
VOICEMAC9	0x21A9	VOICE_SRC_SHORT_ADDRESS[15:8]	R/W	0x00
VOICEMAC10	0x21AA	VOICE_RETRY_COUNT[7:0]	R/W	0x00
VOICEMAC11	0x21AB	VOICE_RESERVED_0[7:0]	R/W	0x00
VOICEMAC12	0x21AC	VOICE_RESERVED_1[7:0]	R/W	0x00
VOICEMAC13	0x21AD	VOICE_RESERVED_2[7:0]	R/W	0x00
VOICEMAC14	0x21AE	VOICE_RESERVED_3[7:0]	R/W	0x00
VOICEMAC15	0x21AF	VOICE_RESERVED_4[7:0]	R/W	0x00

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- VOICECFG0 (VOICE MAC HEADER Control Register, 0x21B0)

Bit	Name	Descriptions	R/W	Reset Value
7:4	VOICE_MAC_LEN	This register defines the length of voice mac header length. In voice packet transmission, MAC header for voice is adjustable by this register. For example, If 0x9 is written in this register, 0x21A0 ~ 0x21A9 registers will be used as voice MAC header, and a voice payload, stored in Tx FIFO, will be attached at the end of 0x21A9 register.	R/W	0xD
3	VOICE_DSN_AUTO_INC	This register enables voice sequence number to increase automatically. Voice operation uses a transmission retry method. It repeatedly tranmit the same frame data. At first transmitted frame data, the sequence number will automatically increase by 1. The other repeated frames are the same with first. The sequence number of repeated frame data remains with that of first frame data.	R/W	0
2	VOICE_RX_MODE	When this register is set to "1", the received voice frame except for voice command frame is automatically transferred to voice RX FIFO. If transfer is completed, Rx End interrupt will be generated.	R/W	1
1	VOICE_TX_MODE	When This rgister is set to "1". Voice payload is a frame data which is stored in not XDATA but voice FIFO. A Tx FIFO use a voice fifo data, which contains a encoded voice data, as voice frame payloads.	R/W	0
0	VOICE_MAH_MODE	This register enbles the MAC header for voice. When this register is set to "1". VOICE MAC Generation block operates.	R/W	0

9.1.5 Receive Mode

When receiving the data from the PHY block, the MAC block stores the data in the RX FIFO.

The frame data in the RX FIFO is transferred to XDATA by DMA operation. It is impossible to directly access the RX FIFO. The stored memory addres is a user defined XDATA address. The RX Controller controls the process described above.

The size of the RX FIFO is 128 bytes and it is implemented by a circular FIFO with a write pointer and a read pointer. The RX FIFO can store several frame data received from the PHY block.

When the frame data is received from the PHY block, the CRC information is checked to verify data integrity.

When AUTO_CRC control bit of MACCTRL (0x2190[1]) register is set to '1', CRC information is verified by the RX CRC block automatically. When the AUTO_CRC control bit of the MACCTRL (0x2190[1]) register is not set to '0', the CRC information should be verified by the software.

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On recived frames, the frame length is stored in the Rx FIFO. During frame receive, the LQI ,RSSI, or data rate value can be substitued for FCS field. (refer to register bit SEL_CRC_FIELD - 0x2190[7:6]).

When a packet reception is completed in the PHY block, a PHY interrupt is sent to the MCU.
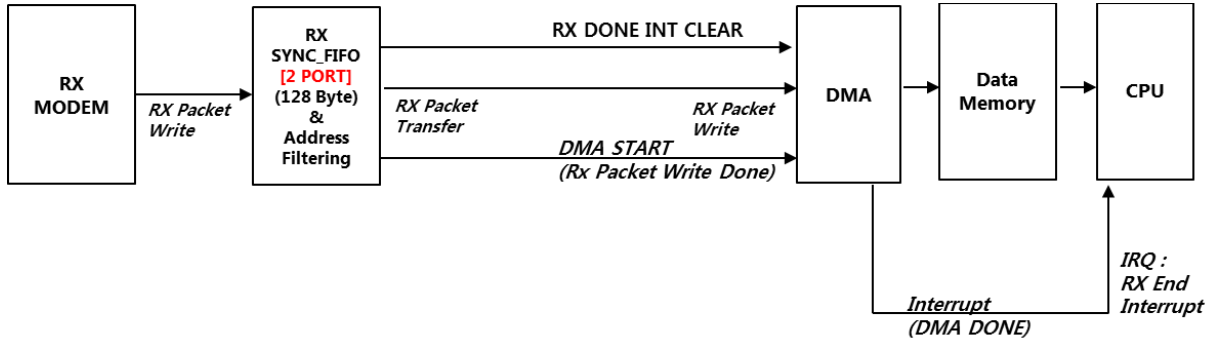
Figure 26. Rx FIFO and DMA Control

A Rx FIFO can not be directly accessed from cpu. a frame data should be always transferred to XDATA by DMA operation.

- Before receiving a frame data, Source address is set to a Rx FIFO address (0x2194)

- Destination address is XDATA address which is defined by user.

- After a reception of a frame data is completed DMA operation.will automatically start.

  − DMA transfers a frame data from a Rx FIFO to a XDATA.

- After DMA operation is completed, Rx End interrupt will be generated.

9.1.6 Transmit Mode

When transmitting the data in the TX FIFO, the CRC operation is processed to verify data integrity. When the AUTO_CRC control bit of the MACCTRL (0x2191) register is set to '1', CRC information is generated by TX CRC block automatically. Otherwise, CRC operation should be operated by software.

For frame transmission, the first byte of the Tx FIFO must contain the frame length information followed by the frame data.
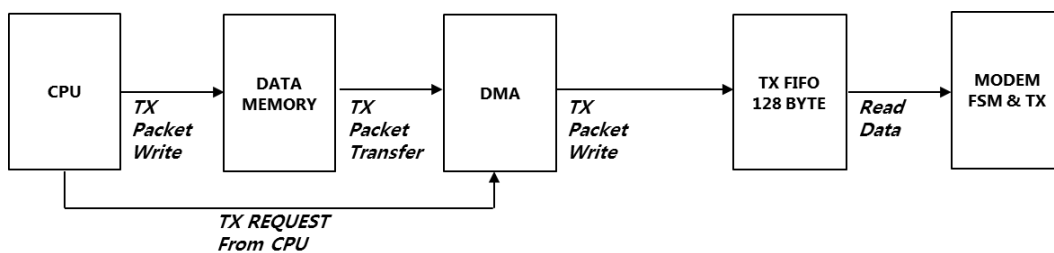
Figure 27. Tx Packet Transfer to Tx FIFO with DMA operation

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A tx FIFO can not be directly accessed from cpu. a frame data should be always transferred from XDATA to Tx FIFO by DMA operation.

- Set source address for storing frame data and transfer packet size.

- Destination address is a tx fifo address (0x2195)

- Start DMA operation.

  – DMA transfer a frame data to tx fifo by push operation.

- If DMA operation is completed, automatically a frame data in TX FIFO is transmitted.

- After finishing transmission mode, Tx End interrupt will be generated.

9.1.7 MAC Retention Register

Table 16. MAC Retention Register

Name	Address
EXTADDR0	0x2170~0x2177
PANID0	0x2178~0x2179
SHORTADDR0	0x217A~0x217B
EXTADDR1	0x2180~0x2187
PANID1	0x2188~0x2189
SHORTADDR1	0x218A~0x218B
SEL_PAN	0x218C
FCFRSVD	0x218D
MACCTRL	0x2190
ADDRFLT1	0x2191
ADDRFLT2	0x2192
ADDRFLT3	0x2193

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9.2 PHY

The baseband PHY (a.k.a. modem) is composed of the O-QPSK modulator and demodulator with simple convolutional channel coder. [Figure 28] shows the baseband PHY structure.

The modulation starts from fetching the data in the TX MAC FIFO. The PHY payload (PHY service data unit; PSDU) can be optionally encoded with the convolutional channel encoder. After appending the preamble, SFD and length field to the PHY payload, a constructed frame (PHY protocol data unit; PPDU) is mapped to designated symbols according to the data-rate control of the PHY controller. Each symbol is accordingly spread by the DSSS chip modulator. The spread PHY bit stream in the chip-level is then modulated to the O-QPSK signal and transmitted by the RF transmitter. For the 250Kbps data-rate packet, its structure is fully compatible with the IEEE802.15.4 O-QPSK PHY specification.
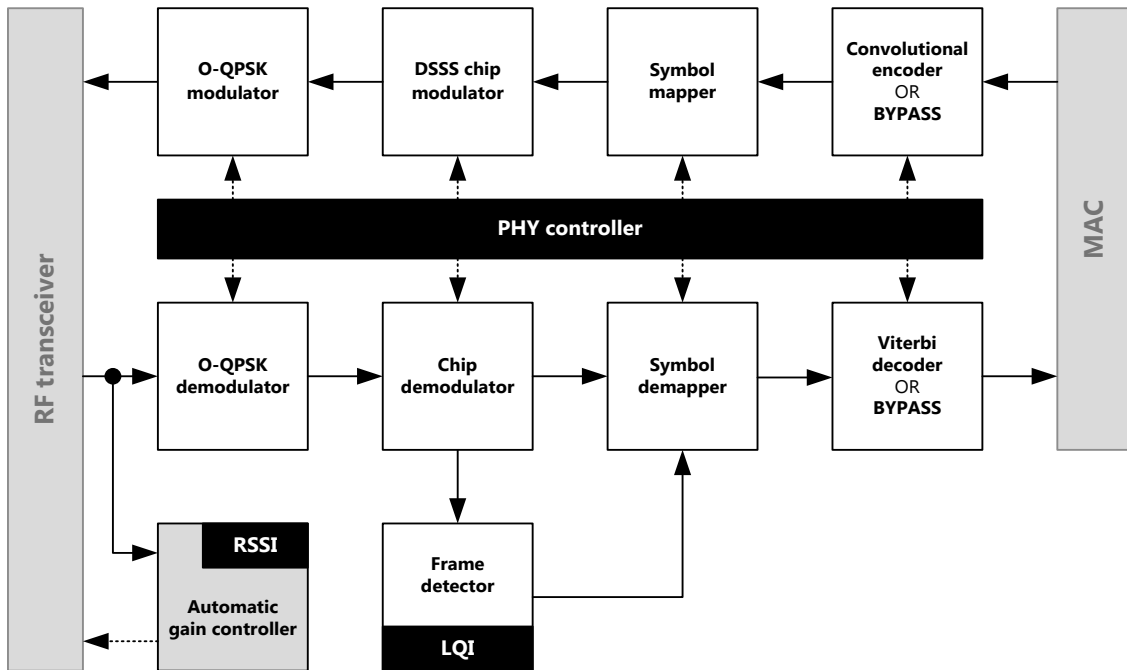
Figure 28. Baseband PHY

With the RF receiver, the received O-QPSK signal is demodulated to the chip sequences. The gain amplifying blocks in the RF receiver are controlled by the automatic gain controller (AGC). The chip sequence is appropriately de-spread by the chip demodulator, and then the start of the designated frame is determined by detecting the synchronization header (preamble and SFD). When the SFD is detected, the baseband PHY generates the interrupt which indicates the start of a packet.

The length and the PHY payload followed by the synchronization header are decoded by the symbol demapper and Viterbi decoder (if the convolutional encoding is applied), and stored in the RX MAC FIFO. When the last data of the PHY payload is stored, the interrupt is generated to indicate the end of the packet reception. After a packet reception interrupt occurs, the RX MAC procedure is performed.

When a packet is received, the baseband PHY provides both of the received signal strength Indicator (RSSI) and the link quality indicator (LQI). They can be used to decide the quality of the communication channel.

While a packet does not exist, the baseband PHY continuously provides the RF channel energy level at antenna. The measured energy level is used to decide the communication channel state. Clear channel assessment (CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple users try to use a channel simultaneously. When a channel is determined to be busy, packet transmission is deferred until the channel state changes to idle.

9.2.1 Interrupt

The baseband PHY has 5 interrupt sources to notify the MCU of specific events.

- RX END (RXEND_INT)

This interrupt notifies the MCU of the completion of a packet reception. When this interrupt has been generated, the received data in RX MAC FIFO can be handled. Also, the quality of the transmission channel can be checked by reading the RSSI/LQI registers.

- RX START (RXSTART_INT)

This interrupt notifies the MCU of the start of a packet reception.

NOTE: It is not recommended to use RX START Interrupt normally.

- TX END (TXEND_INT)

This interrupt notifies the MCU of the end of a packet transmission. A new packet cannot be transmitted until a packet transmission is completed. When a communication channel is busy, a TX END Interrupt can be delayed until a communication channel goes to the idle state and the transmission is completed successfully.

- MODEM READY (MDREADY_INT)

This interrupt notifies the MCU that the state of the baseband PHY has changed from the idle state to the ready state (either RX or TX) for requesting "modem ON". The baseband PHY is in the idle state when the supply power is turned on, but needs to be changed to the ready state in order to transmit or receive the packet. This interrupt occurs when the RF transceiver has been stabilized by following the "modem ON" request.

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• MODEM READY FAIL (MDREADYFAIL_INT)

This interrupt notifies the MCU that the modem block has failed to change state from the idle state to the ready state. When the PLL in the RF transceiver is unlocked during dedicated time interval, this interrupt is generated and the state of the baseband PHY remains at the PLL setting state (although it is a transition state as shown in Figure 25).

The interrupt source can be identified through the INTSTS register. Some interrupt sources can be masked by setting the INTCON register. The baseband PHY also provides the INTIDX register for indicating the interrupt source. The interrupt sources have priority: MDREADY_INT (0) > TXEND_INT (1) > RXSTART_INT (2) > RXEND_INT (3) > MDREADYFAIL_INT (4). The INTIDX register indicates the highest-priority interrupt source among the present interrupts (not cleared). In order to clear the interrupt, it is sufficient to just read the INTIDX register and then the interrupt is cleared (one by one) in priority order.

• INTCON (PHY INTERRUPT CONTROL REGISTER, 0x226D **[RETENTION]**)

This register is used to mask off the interrupt of baseband PHY.

Bit	Name	Descriptions	RW	Reset Value
7:5	(Reserved)			0x0
4	MDFAILMSK	This field masks MDFAIL_INT off. When MDFAILMSK field is set to '0', MDFAIL_INT interrupt is not generated.	R/W	0
3	RXENDMSK	This field masks RXEND_INT off. When RXENDMSK field is set to '0', RXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet reception.	R/W	0
2	RXSTMSK	This field masks RXEND_START off. When RXSTMSK field is set to '0', RXSTART_INT interrupt is not generated. RXSTART_INT is not a mandatory interrupt. It is recommended to mask off RXSTART_INT interrupt when the rapid packet reception is needed.	R/W	0
1	TXENDMSK	This field masks TXEND_INT off. When TXENDMSK field is set to '0', TXEND_INT interrupt is not generated. This interrupt should be used to support the successful packet transmission.	R/W	0
0	MDRDYMSK	This field masks MDRDY_INT off. When MRDYMSK field is set to '0', MDRDY_INT interrupt is not generated. This interrupt should be used to check whether a modem block is ready for transmission /reception or not.	R/W	0

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- INTIDX (PHY INTERRUPT STATUS AND INDEX REGISTER, 0x226E)

This register is used to indicate the kinds of the interrupt when it occurs

Bit	Name	Descriptions	RW	Reset Value
7:5		(Reserved)		0
4	ALLINTCLR	This field disables all interrupts when they occur. This field clears all interrupts occurred. When multiple interrupts occur at the same time, the modem block stores them in a buffer and processes them in order. When INTIDX field is read, the executed interrupts are cleared in order. When ALLINTCLR field is set to '0', all the interrupts in buffer are cleared at the same time.	R/W	1
3		(Reserved)		
2:0	INTIDX	This register shows the kind of the interrupt when an interrupt occurs, in order if multiple interrupts occur simultaneously. The INTSTS field in the INTSTS register should be used for looking through a list of all interrupts that have been triggered. After reading INTIDX field, executed interrupts are cleared automatically. 	INTIDX	Interrupt
--------	-----------
0	MDRDY_INT interrupt
1	TXEND_INT interrupt
2	RXSTART_INT interrupt
3	RXEND_INT interrupt
4	MDFAIL_INT interrupt			

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- INTSTS (PHY INTERRUPT STATUS REGISTER, 0x226F)

This register is used to indicate the kinds of the interrupt when the multiple interrupts occur.

Bit	Name	Descriptions	RW	Reset Value
7:5		(Reserved)		0
4:0	INTSTS	Multiple interrupt status This register shows the interrupt status when multiple interrupts occur currently. Each bit in INTSTS field represents the status of a specific interrupt. A table of Bit vs. Interrupt is shown below. {{TABLE}} When an interrupt is triggered, the INTSTS field corresponding to each interrupt is set to '0'. To clear the executed interrupt, the bit for each of the executed interrupts should be reset to '1' by software.		

Inner table (within INTSTS description):

Bit	Description
0	MDRDY_INT interrupt
1	TXEND_INT interrupt
2	RXSTART_INT interrupt
3	RXEND_INT interrupt
4	MDFAIL_INT interrupt

9.2.2 Data Rate

The MG2475 supports data rate modes of 250Kbps and 1Mbps for applications beyond IEEE802.15.4 compliances. The data rate can be selected by using the DATARATE register.

The 250Kbps and 1Mbps modes, which are listed in [Table 17], occupy 2MHz RF channel bandwidth which is the same as the IEEE 802.15.4-2.4GHz 250Kbps standard mode. The 1Mbps data-rate mode is designed by applying the convolutional coding with the similar preamble structure as 250Kbps specified in IEEE802.15.4.

Table 17. Data rate modes

Data Rate Mode	DATA_RATE (0x220B)	Comment
1Mbps	0x1	FEC RATE 1/2
250Kbps	0x4	IEEE802.15.4 compliant

- Forward Error Correction

Especially for higher data rate modes, the MG2475 uses the convolutional channel coding for forward error correction (FEC). The MG2475 supports the convolution coding with the rates of 1/2.

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As shown in [Figure 29], the convolutional encoder with the constraint length of 5 is used for the mother convolutional encoder with the rate of 1/2. $G1(x) = x^4 + x + 1$. $G2(x) = x^4 + x^3 + x^2 + 1$.
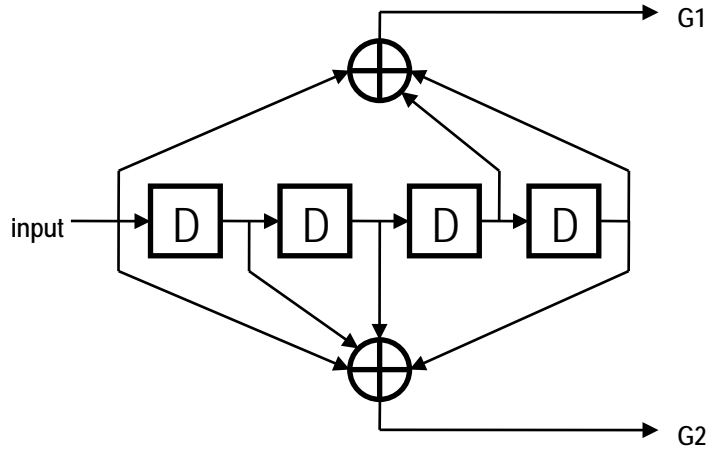
Figure 29. Convolutional encoder with rate of 1/2

Table 18. Convolutional Encoder Generators

Code rate	Generators in octal	Transmitted sequence
1/2	G1: 23 G2: 35	G1 G2

- Packet Format

  The MG2475 supports two data rates, 250Kbps and 1Mbps. The packet format comparison for high data rates (≥ 250Kbps) with an example payload length of 60-Byte is shown in [Figure 30]. The period of the preamble, SFD, and LEN for 1Mbps data-rate mode is the same for 250Kbps mode. Only PHY payload interval is reduced.
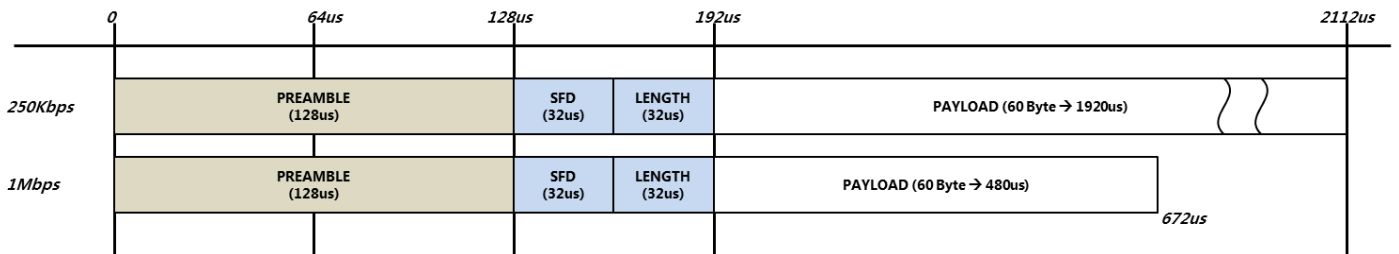
Figure 30. Data Rate packet format

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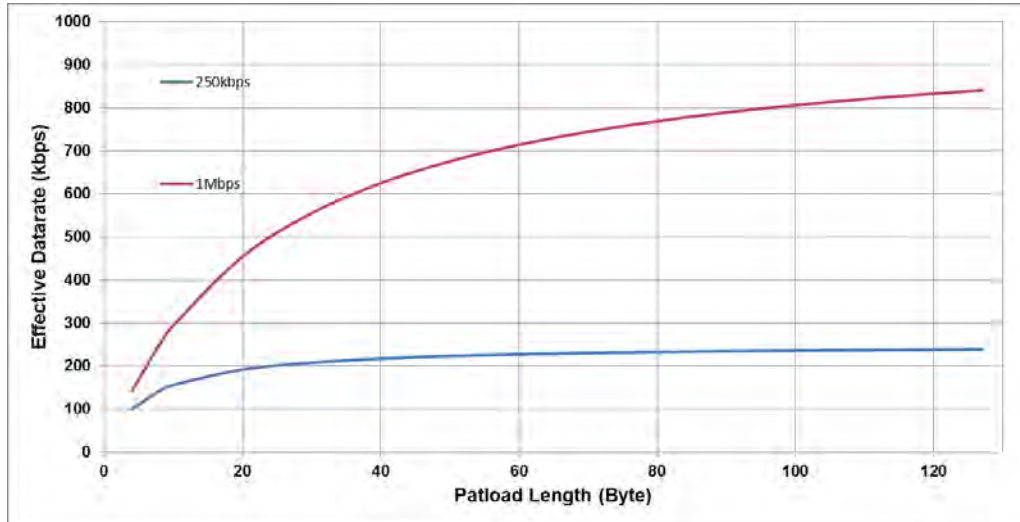
Figure 31. Effective Data Rate

- PCMD0 (PHY COMMAND0 REGISTER, 0x2200)

This register is used to control the operation of baseband PHY.

Bit	Name	Descriptions	RW	Reset Value
[7]	MODEM_OFF	When this field is set to '1', the baseband PHY status is changed to OFF. In the OFF state, the RF block is in a power-down state and the modem block is in the reset state. In this state, the MG2475 cannot receive or transmit packets. For the transmission or the reception of a packet, the baseband PHY needs to be changed to ON state.	R/W	0
[6]	MODEM_ON	When this field is set to '1', the baseband PHY status is changed to ON. In ON state,the RF and baseband PHY are in the TX or RX ready state. In this state, the modem block controls power-down or power-up for the transmitter or the receiver without an active user application program. When the modem block goes to ON status, this field is set to '0' automatically by the hardware.	R/W	0
[5:4]	(Reserved)	Only '0x0' allowed	R/W	0x0
[3]	TX_OFF	When this field is set to '1', the TX block is forced to be OFF regardless of the control of the baseband PHY state machine.	R/W	0
[2]	RX_OFF	When this field is set to '0', the RX block is forced to be OFF regardless of the control of the baseband PHY state machine.	R/W	0
[1:0]	(Reserved)	Only '0' allowed.	R/W	0

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- DATA_RATE (MODEM DATARATE CONTROL REGISTER, 0x220B **[RETENTION]**)

This register is used to set data rate.

Bit	Name	Descriptions	RW	Reset Value
[7:3]	(Reserved)	Only '0' allowed.	R/W	0x0
[2:0]	DATA_RATE	Used to select packet data rate	R/W	0x4

DATA_RATE	Data Rate
0x1	1Mbps (FEC Rate 1/2)
0x4	250Kbps

9.2.3 Clear Channel Assessment

While a packet does not exist, the baseband PHY continuously provides the RF channel energy level at antenna. As described before, the measured energy level is used to decide the communication channel state. Clear channel assessment (CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple users try to use a channel simultaneously. When a channel is determined to be busy, packet transmission is deferred until the channel state changes to idle.

- CCACFG0 (CLEAR CHANNEL ASSESSMENT0 REGISTER, 0X2236)

This register is used to set CCA operation environment.

Bit	Name	Descriptions	RW	Reset Value
[7:6]		Reserved: Only '0' allowed.	R/W	0
[5]	CCA_FIX	It fixes the communication channel state to idle. A communication channel state is determined by the CCA circuit in MG2475. When a channel state is busy, a packet is not transmitted. This field allows packet transmission regardless of the channel state. When this field is set to '1', the channel is always in idle state.	R/W	1
4		Reserved: Only '1' allowed.	R/W	1

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Bit	Name	Descriptions	RW	Reset Value
[3:2]	CCA_AWS	This field sets the time duration in which the energy of received signal is measured. It is only valid for the energy detection method. | CCA_AWS	Energy calculation duration | |-----|-----| | 0x0 | 1 usec | | 0x1 | 2 usec | | 0x2 | 4 usec | | 0x3 | 16 usec |	R/W	0x3
[1:0]	CCAMD	This field sets the method to determine the communication channel state. The following describes the three methods to detect the channel state. Energy detection (ED): This method determines the channel state as 'busy' when the energy of received signal is higher than the defined level. Carrier detection (CD): This method determines the channel state as 'busy' when an IEEE802.15.4 carrier is detected. Frame detection (FD): This method determines the channel state as 'busy' when the normal IEEE802.15.4 packet is detected. | CCAMD	Method | |-----|-----| | 0 | ED | | 1 | CD | | 2 | FD | | 3 | reserved |	R/W	0

- CCACFG1 (CLEAR CHANNEL ASSESSMENT1 REGISTER, 0X2237)

This register is used to set CCA operation environment.

Bit	Name	Descriptions	RW	Reset Value
[7:0]	CCA1	This configures the CCA decision threshold when the energy detection method is used as that of the CCA detection.	R/W	0xB2

9.2.4 Link Quality Indicator

The MG2475 uses correlation results of multiple symbols in order to calculate an estimate of the LQI value. If LQI_EN is "0x1", LQI estimation is automatically performed for every received frame. LQI values are integers ranging from 0 to 255 as required by the IEEE 802.15.4 standard.

After receiving 8 first symbols following the SFD, The MG2475 provide a correlation average value as a LQI. This is indicated by the LQI_VALID register. The value can be obtained by means of register read.

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- CTRLCFG0 (LQI CONTROL REGISTER, 0x220A[7])

This register is used to check LQI valid indicator.

Bit	Name	Descriptions	RW	Reset Value
7	XCOR_EN	Cross correlation measure Enable Register • 1 : Enable • 0 : Disable	R/W	1
6:0		Only 0x73 allowed		0x73

- XCORSTS (LQI VALUE REGISTER, 0x2269)

This register is LQI value which is computed with correlation value.

Bit	Name	Descriptions	RW	Reset Value
7:0	XCORSTS	LQI value : 0~ 255	RO	0x00

Received Signal Strength Indicator

  When a packet is received, the baseband PHY provides both of the received signal strength Indicator (RSSI). The average energy level of the received RF signal at antenna is stored at AGCSTS2. The average energy level of the received packet is stored at AGCSTS3.

  [Figure 23] shows typical measured RSSI plot over whole dynamic range. The typical dynamic range of the RSSI is about 80dB, and the accuracy is less than ± 3dB.

- AGCSTS2 (AGC STATUS2 REGISTER, 0x2264)

The stored energy level is the average of the received signal energy. The indicated value at AGCSTS2 register is stored as a 2's complement integer in dBm.

Bit	Name	Descriptions	RW	Reset Value
[7:0]	RXENRG	Average energy level of the received RF signal at antenna. **NOTE:** After writing 0xFF, read a register value. Writing operation makes a latch signal for average energy.	R	0x00

- AGCSTS3 (AGC STATUS3 REGISTER, 0x2265)

  While AGCSTS2 register indicates the average of received signal's energy level for a defined time interval, AGCSTS3 register shows the energy level of the last received packet. The value in AGCSTS3 register is retained until another packet is received.

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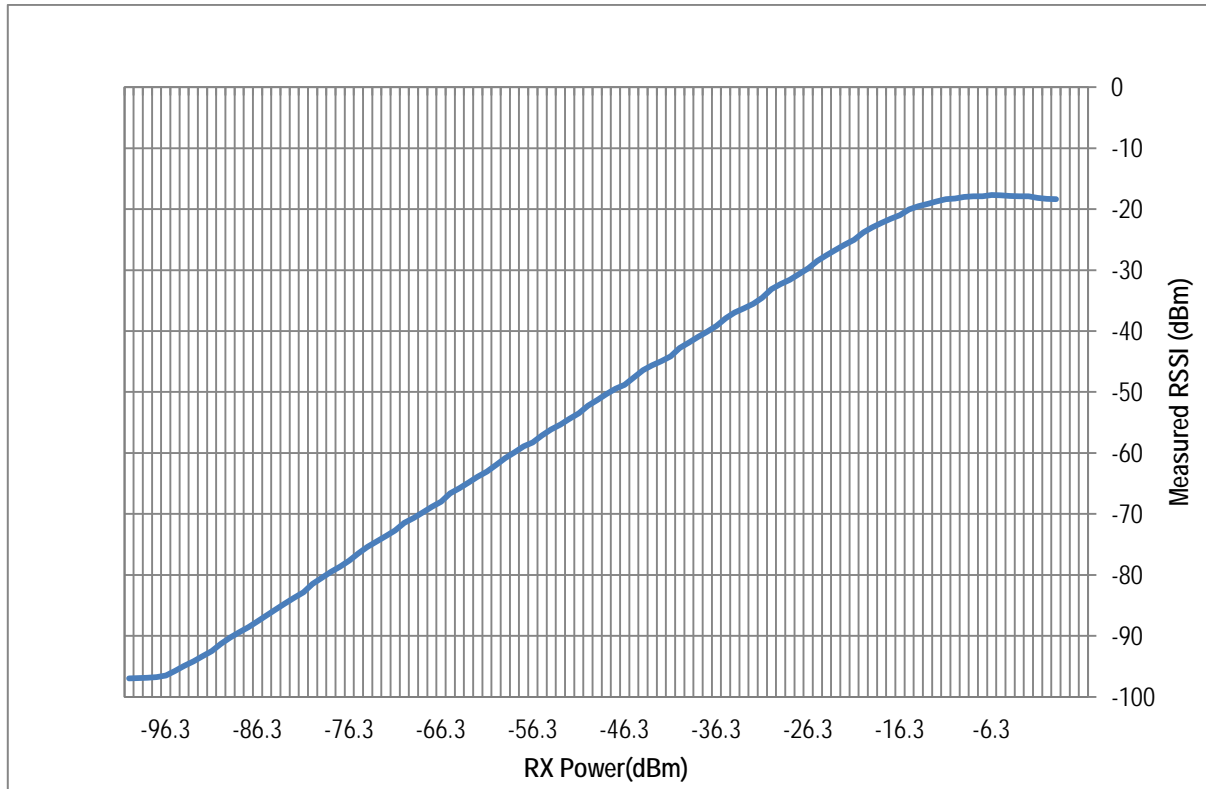| Bit	Name	Descriptions	RW	Reset Value
[7:0]	PKTENRG	Average energy level of the received packet	R	0x00

Figure 32. Measured RSSI (typical) versus RX input power (TBD)

9.2.5 Tx Packet Retransmission Mode

 MG2475 supports automatic retransmission mode with the help of H/W. this mode can be used in Voice Packet transmission.

- Retransmission Burst Mode

If a transmitted packet has no ack request, there is no need to check ack packet receive.so during transmission, MG2475 don't receive any packet.

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Retransmission Burst Mode
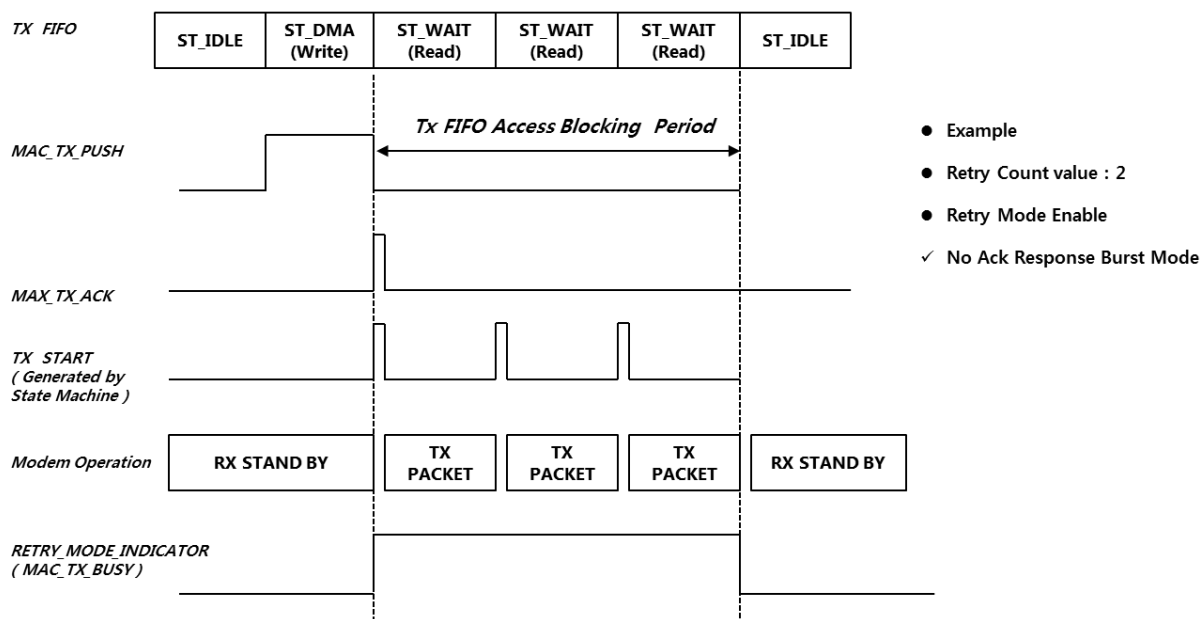
Figure 33. Tx Retransmission Burst Mode

- Retransmission Ack Mode

When a transmitted frame has a ack request, it will wait for receiving an ack frame but if it fails to receive an ack frame. The same frame will be automatically transmited in retransmission ack mode. This mode will be terminated as soon as receiving an ack frame or retry counter value reach a max retry number
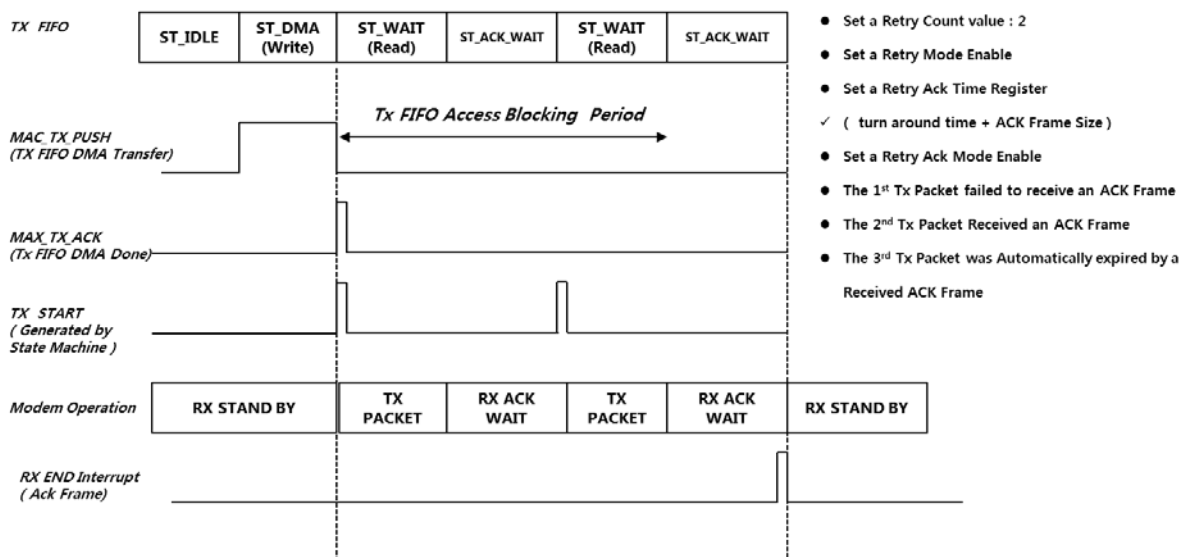

Figure 34. Retransmission Ack Mode Example

- Retransmission Ack Mode Setting
  - PREVENT_ACK
  - ACK_FRAME_IND
  - CNT_RETRY
  - RETRY_ACK_WAIT_TIME

- RETRYCFG0 (RETRY CONFIG REGISTER, 0x220C **[RETENTION]**)

Bit	Name	Descriptions	RW	Reset Value
7:5	RESERVED	Only 0 allowed	R/W	0x00
4	SEL_RETRY _TXE_INT	Selection of Tx End interrupt in Retransmission Mode • 0 : Tx End Interrupt occurrs only at last transmission • 1: Tx End Interrupt occurrs at every transmission	R/W	1
3:0	CNT_RETRY	Number of repeatition • 0 : Normal Mode (No Retransmission Mode) • N : N Times Retry	R/W	0

- RETRYCFG1 (RETRY CONFIG REGISTER, 0x220D **[RETENTION]**)

Bit	Name	Descriptions	RW	Reset Value
7	ACK_FRAME _IND	This register enables a retransmission ack mode, when RETREY_ACK_EN is set 1.	R/W	1
6:5		Reserved : Only 0x2 allowed		0x2
4	RETRY_ACK _EN	This register enables a retransmission ack mode, when ACK_FRAME_IND is set 1 • 0 : Retransmission Ack Mode Disable • 1 : Retransmission Ack Mode Enable	R/W	0
3:0	RETRY_ACK _WAIT_TIME	This register define the ack frame wait time in retransmission ack mode N : N*128us (min 0us ~ max 1920us, default 1280us)	R/W	0xA

9.2.6 RADIO

A simplified block diagram with emphasis on RF and Analog front-end is shown in [Figure 35]. Since the bidirectional differential RF pins are used for RX and TX, no external T/R switch is required. In a receive path, a direct-conversion architecture is adopted. It operates in the 2.4GHz ISM band with excellent receiver sensitivity and robustness to interferers. Transmitter architecture is based on a direct-modulation technique using a direct RF frequency synthesis.
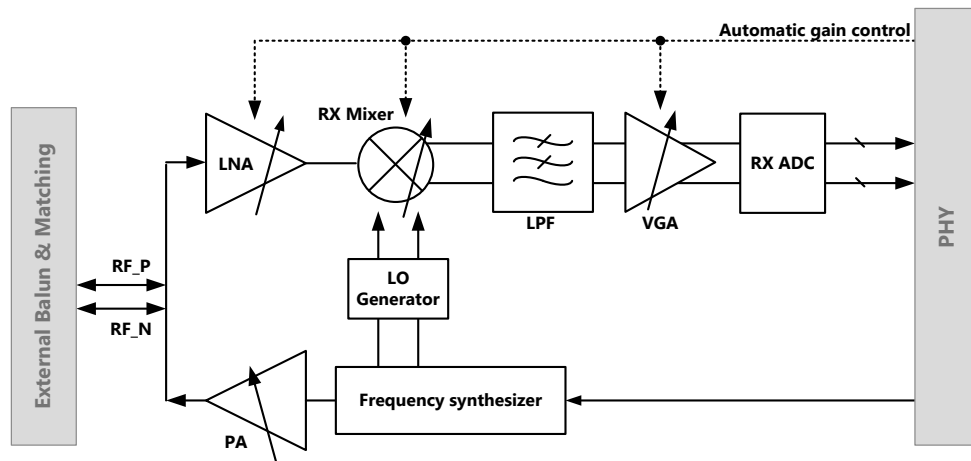

Figure 35. RF and Analog Block Diagram

  The LNA amplifies the incoming received RF signal at RF_P and RF_N pins. The gain is controlled coarsely by the AGC block.

  The RX Mixer converts the RF signal to the baseband frequency in quadrature(I and Q). Also, the gain is controlled coarsely by the AGC block.

  Channel filtering occurs in the LPF(low-pass filter). The VGA(variable-gain amplifier) provides sufficient gain, controlled by AGC, to drive the RX ADC(analog-to-digital converter).

  The RX ADC converts the VGA output signals to the signed binary digital signals.

The frequency synthesizer(PLL) generates the carrier signals for channel frequency during reception and feeds the baseband modulation signals directly to the power amplifier during transmission. The center frequency of the desired channel can be adjusted by PLLFREQ register.

  The LO generator transforms the differential outputs of the frequency synthesizer into the quadrature(I and Q) signals required for local signals in the RX Mixer.

  The TX PA(power amplifier) amplifies the modulated RF signal from the PLL. The transmit power can be controlled by setting two registers of TXPA and TXDA.

  In addition, external PA can be used with control pin(s) of TRSW and/or TRSWB. The TRSW and TRSWB is shared with GPIO P1[7] and P1[6] respectively. When MG2475 stays at the transmit mode, TRSW = 1. These pins are available by setting two registers of P1SRC_SEL (SFR) and MONCON1.

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- PLLFREQ (CHANNEL CENTER FREQUENCY CONTROL REGISTER, 0x2276 **[RETENTION]**)

This register is used to control the frequency of the frequency synthesizer for selecting the desired channel.

Bit	Name	Descriptions	RW	Reset Value
7	(Reserved)	Only '0' allowed.	R/W	0
6:0	PLL_FREQ	Channel center frequency selection register f_{center} = 2394 + PLL_FREQ (MHz) The values of 5xN + 1 where N = 0, 1, …, 22 are only valid as that of PLL_FREQ.	R/W	0x33

- TXRAMP1 (TX Power Selcetion REGISTER, 0x221B)

This register is used to control the Tx Power of the transmit PA

Bit	Name	Descriptions	RW	Reset Value
7:5		Reserved	RO	0x0
4:0	SEL_TX_POWER	This register defines the final power of ramping step. • 0x00: Minimum Power (TBD) • 0x17: Max Power (TBD)	R/W	0x17

- P0SRC_SEL (GPIO 0 SOURCE CONTRL REGISTER, 0x9B (SFR) **[RETENTION]**)

This register is used to control the GPIO source

Bit	Name	Descriptions	RW	Reset Value
7:0	P0SRC_SEL	PORT-0 source control register Each bit of port-0 can be mapped to the specific signals related to baseband. With this register control of P0SRC_SEL = 0x30, the TRSW and TRSWB which are drived by baseband modem are available through P0[5] and P0[4] respectively.	R/W	0x00

- SEL_PIN_45 (MONITOR CONTROL REGISTER, 0x2253)

This register is used to generate the TRSW and TRSWB along with P0SRC_SEL.

Bit	Name	Descriptions	RW	Reset Value
7:0	MONCON1	This setting of 0x99 generates the TRSW and TRSWB through P0[5] and P0[4].	R/W	0x14

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9.2.7 PHY Retention Register

Table 19. PHY Retention Register

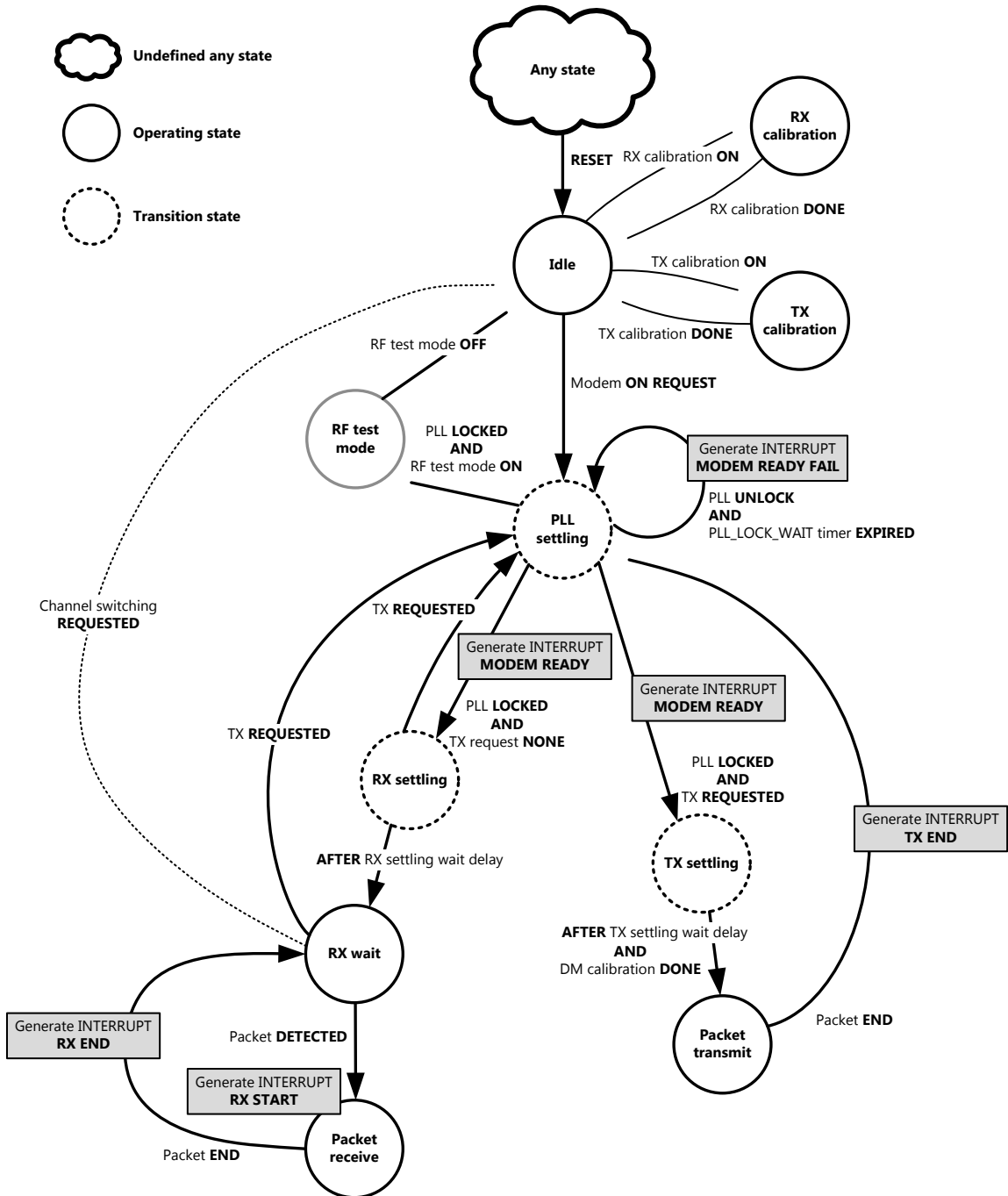| Name	Address
DATARATE	0x220B
RETRYCFG	0x220C
TXRAMP0	0x221A
INTCON	0x225D
PLLFREQ	0x2276

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9.3 Operating Modes

Figure 36. MG2475 State transition diagram

MG2475 PHY operation is controlled by the modem FSM shown in [Figure 36]. MG2475 PHY can be initialized by the reset. According to the control of the modem FSM, MG2475 operates in either packet transmitting or packet

receiving mode: When the packet to be transmitted is prepared in TX MAC FIFO, MG2475 only operates in the packet transmit mode. Besides, it operates in the packet receiving mode and waits for the packet.

Idle state: MG2475 PHY can be initialized by the reset and the state of the modem FSM is moved to the idle state. In this state, the PHY executes no operation.

RX calibration state: In order to receive the packet correctly, the DC offset of the RF receiver should be calibrated before using it. Before MODEM ON is set, the DC offset of the RF receiver is preferred to be calibrated. When the DC calibration is initiated, the state is transited to RX calibration state. When the RX calibration has completed, the state is automatically transited to idle state. After the initial DC calibration is performed, the DC calibration tracker should be enabled.

TX calibration state: The modulation block of the RF transmitter should be also calibrated. Before MODEM ON is set, the TX modulator is preferred to be calibrated. When the TX calibration is initiated, the state is transited to TX calibration state. When the TX calibration has completed, the state is automatically transited to idle state.

PLL settling state: When the TX calibration is done, the RF synthesizer for channel selection can be configured and then the PLL (RF synthesizer) is started. Additionally, the PLL may be restarted in order to change the RX or TX channel. In the PLL settling state, the modem waits for the PLL to be locked. If the PLL is locked within designed time interval, the interrupt for MODEM READY is generated. Otherwise, the interrupt for MODEM READY FAIL is generated. This state is also a transition state. If the PLL is already locked (it can be clearly identified from the PLL lock detection flag), this state can be skipped.

RF test mode state: The RF test mode state is entered by setting the register as the RF test mode. When the PLL is locked and the RF test mode is set, the modem FSM changes its state from the PLL settling to the RF test mode state. Basically, in this state, the modem operates as the transmitter only. The modem FSM leaves this state to the idle state when the RF test mode becomes disabled.

TX settling state: When the PLL is locked and the packet transmission is requested (from MAC layer), the state of the modem FSM is changed from the PLL settling to the TX settling. In this state, the modem waits for the RF transmitter to be stable. The modem FSM stays at this state during the TX (settling) wait delay which can be configured.

Packet transmit state: After TX (settling) wait delay, the state of the modem FSM is transited to the packet transmit state. In this state, the modem transmits the packet in accordance to the PHY specification. When the packet transmission is completed, the state is moved to the PLL settling state along with generating the interrupt for TX END.

RX settling state: When the PLL is locked and no packet transmission is requested, the state of the modem FSM is changed from the PLL settling to the RX settling state in order to wait for packet coming from other transmitting

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units. In this state, the modem waits for the RF receiver to be stable. The modem FSM stays at this state during the RX (settling) wait delay which can be configured. If the packet transmission is requested when the state of the modem FSM stays at this state, the modem FSM changes its state from the RX settling to the PLL settling state.

RX wait state: After RX (settling) wait delay, the state of the modem FSM is transited to the RX wait state. In this state, the modem waits for the packet reception. When the packet is detected, the state is moved to the packet receive state along with generating the interrupt for RX START. If the packet transmission is requested when the state of the modem FSM stays at this state, the modem FSM changes its state from the RX wait to the PLL settling state.

Packet receive state: When the packet is detected at the RX wait state, the state of the modem FSM is moved to the packet receive state. In this state, the modem receives the packet and puts its payload to RX MAC FIFO. At the end of the packet, the state is transited to the RX wait state along with generating the interrupt for RX END.

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10 IN-SYSTEM PROGRAMMING (ISP)

The in-system programming (ISP) function enables a user to download an application program to the internal flash memory. When it is power-on, the MG2475 checks the value of MS pin. When the value of the MS pin is '1', ISP mode is selected. The following procedure is to use the ISP function.

- MS pin should be set to '1'
- Make RS-232 connection with the PC by using the serial port or the USB-to-Serial adapter. The configuration is 8-bit, no parity, 1 stop bit and 115200 baud rate.
- Power up the device.
- Execute the ISP Host program on PC. (It is included in Development Kit)
- Load an application program in Intel HEX format.
- Download.

When the procedure is finished, an application program is stored in the internal flash memory. To execute the application program, a device should be reset after setting MS pin to '0'.

After reset, the application program in the internal flash memory is executed by the internal MCU.

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11 PACKAGE INFORMATION

- MG2475 package type is 40-pin QFN package with down-bonding.

Figure 37. Package Drawing-QFN40
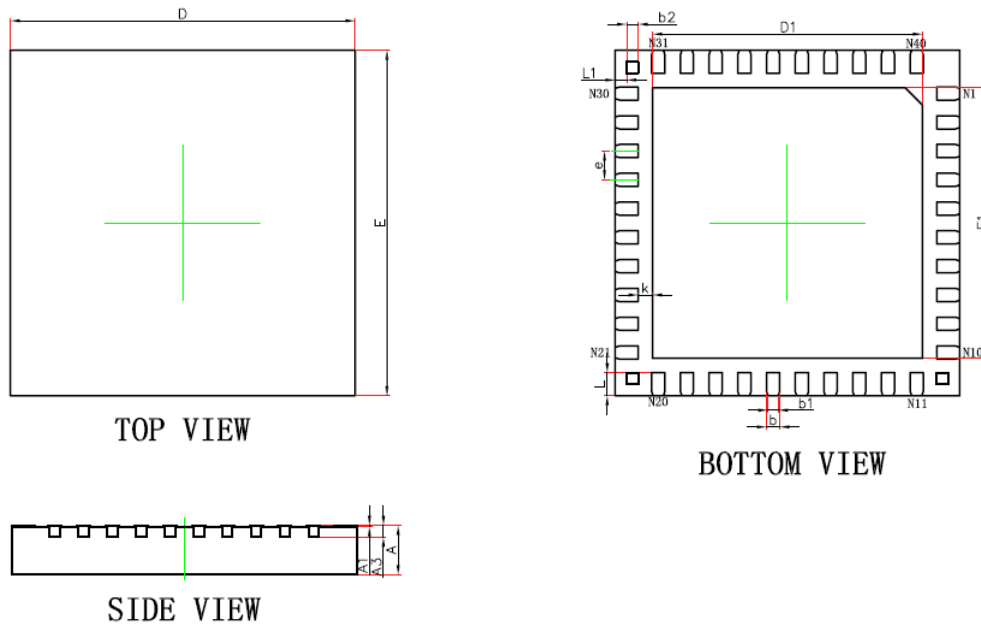
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
D1	4.600	4.800	0.181	0.189
E1	4.600	4.800	0.181	0.189
e	0.500BSC.		0.020BSC.	
k	0.250REF.		0.010REF.	
b	0.180	0.280	0.007	0.011
b1	0.180REF.		0.007REF.	
b2	0.200REF.		0.008REF.	
L	0.324	0.476	0.013	0.019
L1	0.200REF.		0.008REF.	

- Marking

(1) PIN 1 indicator
(2) Package assembly & test site(JG)
(3) Year code
(4) Weekly code

(5) Product Code(MG2475)
(6) Product Version(A)
(7) User F/W Version(ZZ)
(8) Package type (F3=40QFN)
(9) Flash size(4=64KB)
(10) Application(0=General Purpose)
(11) Temperature spec (C=Commercial)

(12) Lot No

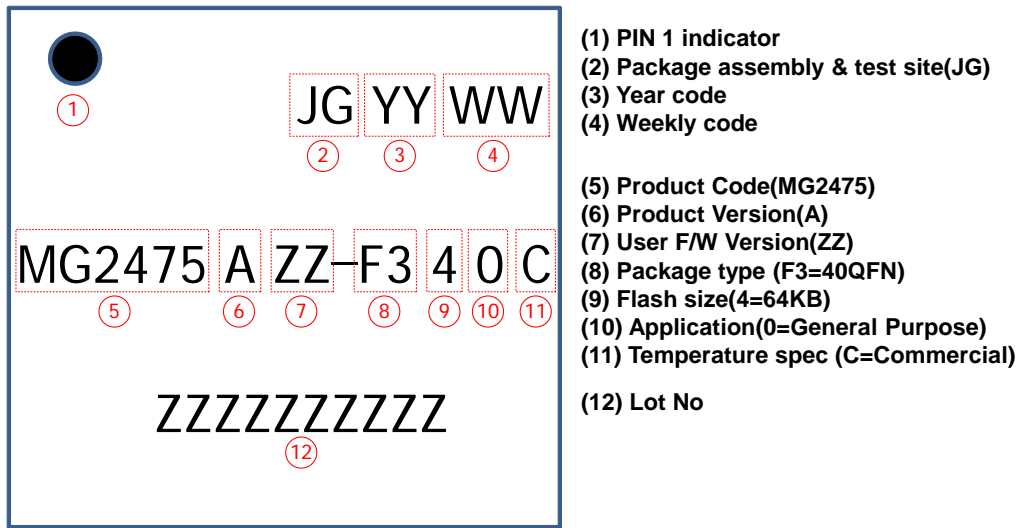**Figure 38. Chip Marking**

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About RadioPulse Inc.

RadioPulse is a Being Wireless solution provider offering wireless communication & network technologies and developing next generation wireless networking technologies.

The new wireless networking solutions envisioned by RadioPulse will enable user to enjoy wireless technologies with easy interface.

Founded in April of 2003, the company maintains it headquarters and R&D center in Korea.