

Automotive-grade N-channel 600 V, 0.037 Ω typ., 66 A MDmesh™ DM2 Power MOSFET in a TO-247 package

Datasheet - production data

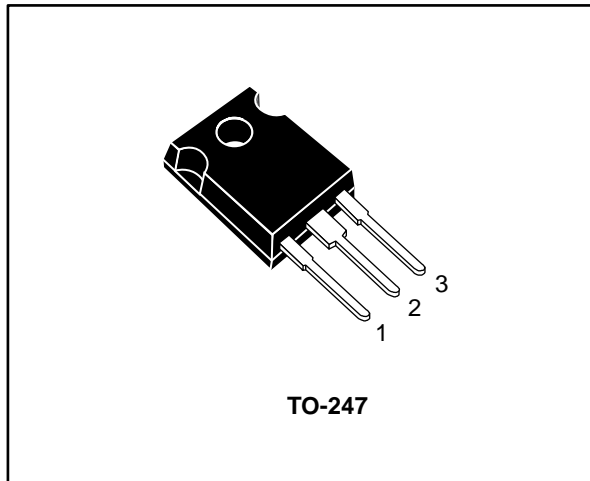
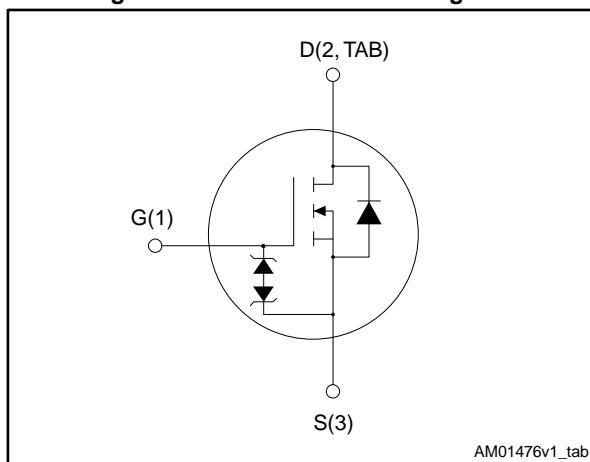


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STW72N60DM2AG	600 V	0.042 Ω	66 A	446 W



- AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW72N60DM2AG	72N60DM2	TO-247	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 TO-247 package information.....	9
5	Revision history	11

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	66	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	42	
$I_{DM}^{(1)}$	Drain current (pulsed)	264	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	446	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 66\text{ A}$, $di/dt=800\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

(3) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.28	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	10	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1500	mJ

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$			10	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 5	μA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 33\text{ A}$		0.037	0.042	Ω

Notes:

⁽¹⁾ Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	5508	-	pF
C_{oss}	Output capacitance		-	241	-	
C_{rss}	Reverse transfer capacitance		-	2.8	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	470	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	2	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 66\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	121	-	nC
Q_{gs}	Gate-source charge		-	26	-	
Q_{gd}	Gate-drain charge		-	61	-	

Notes:

⁽¹⁾ $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 33\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	32	-	ns
t_{r}	Rise time		-	67	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	112	-	
t_{f}	Fall time		-	10.4	-	

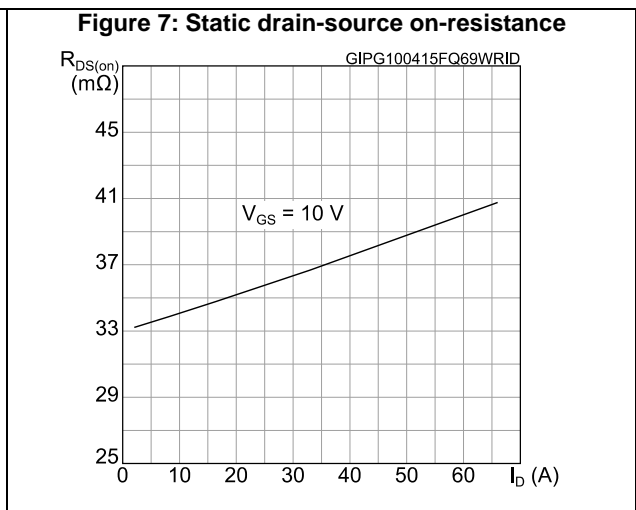
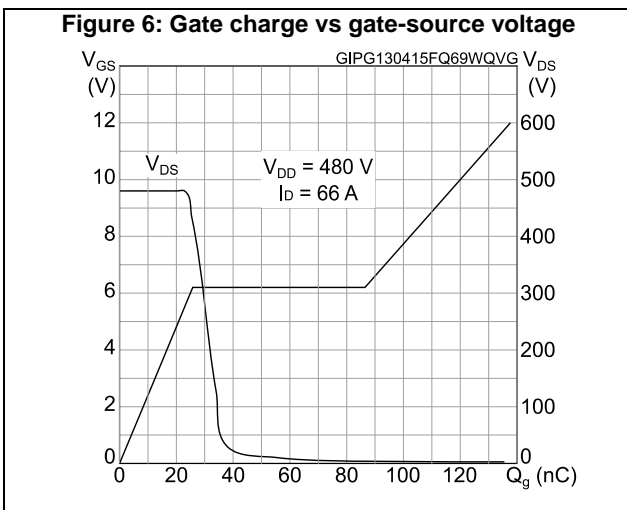
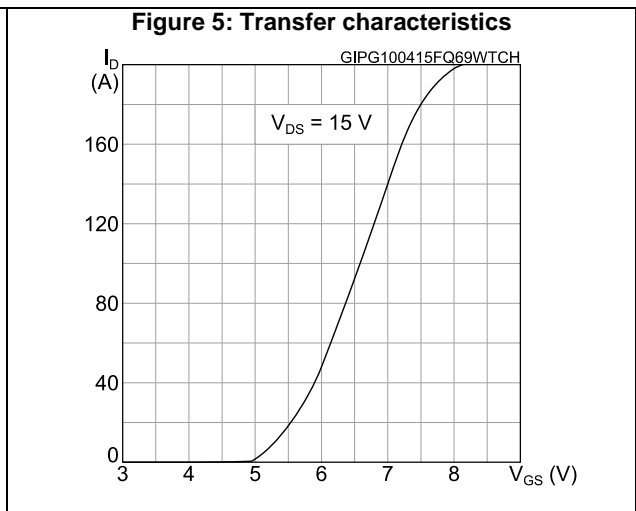
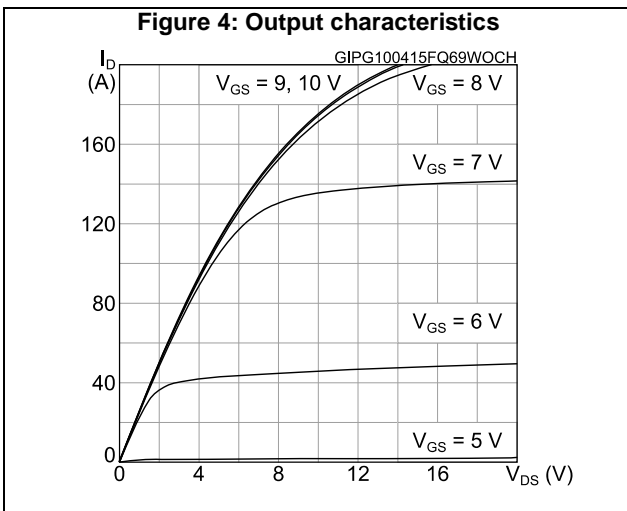
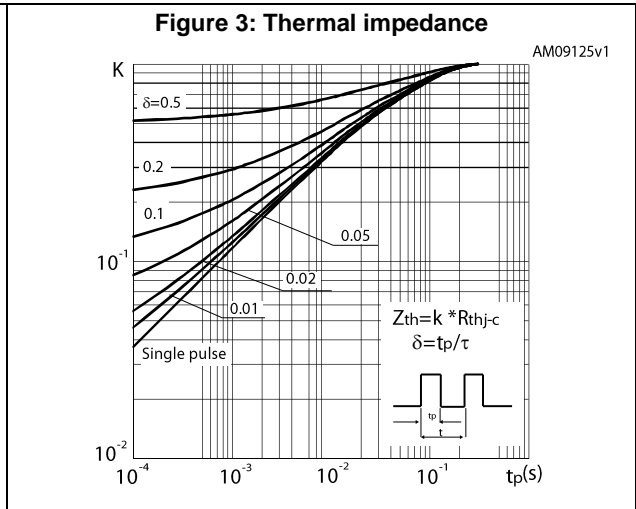
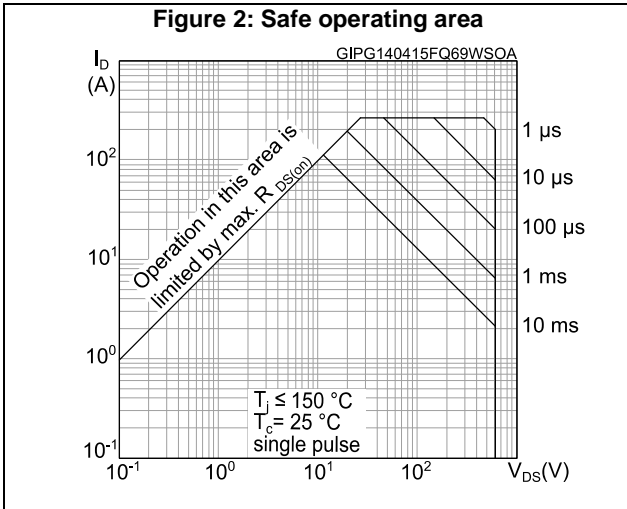
Table 8: Source-drain diode

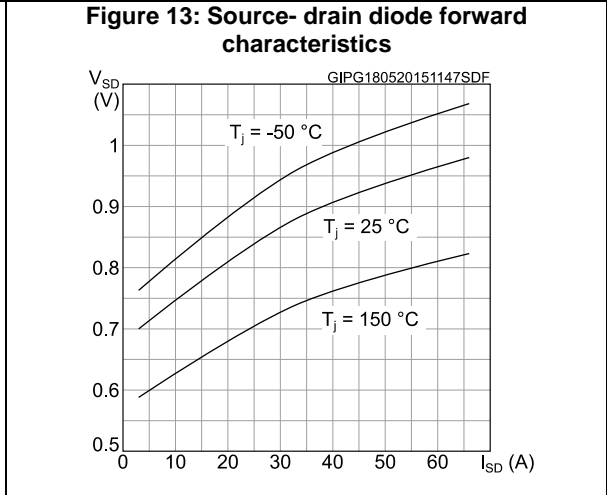
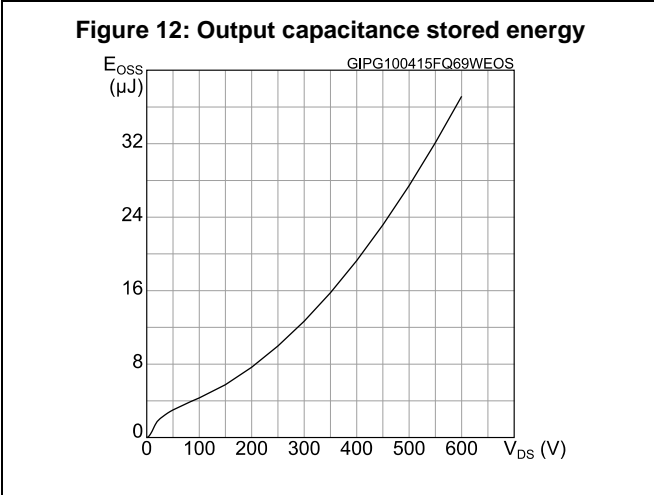
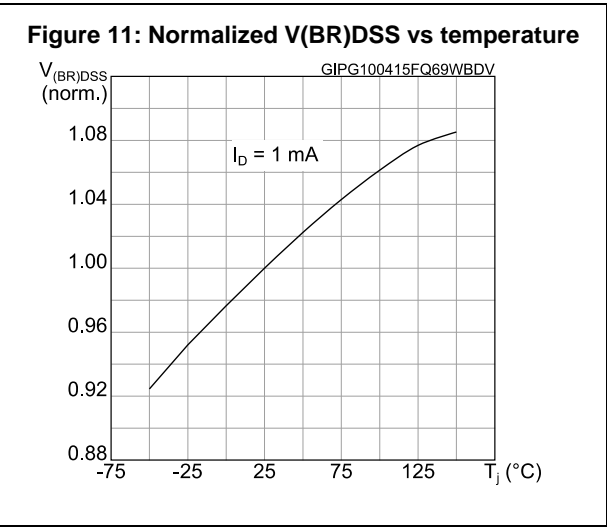
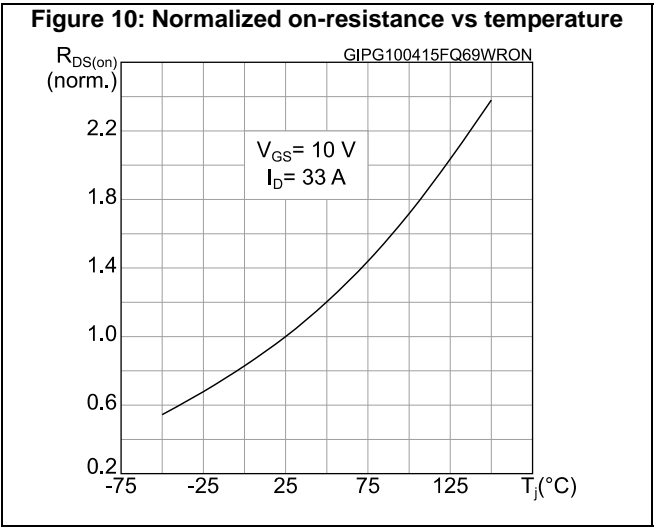
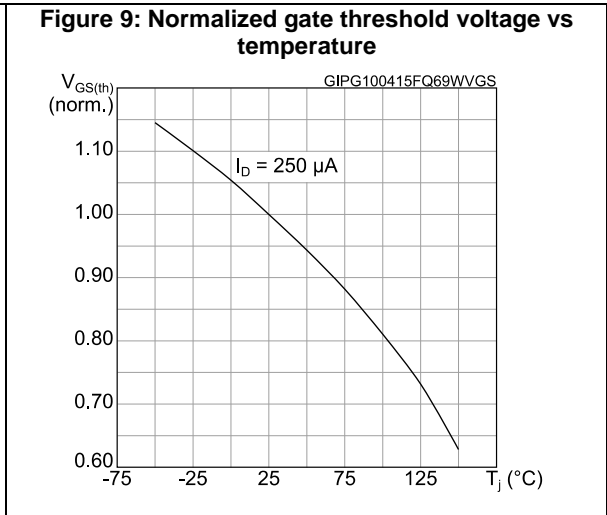
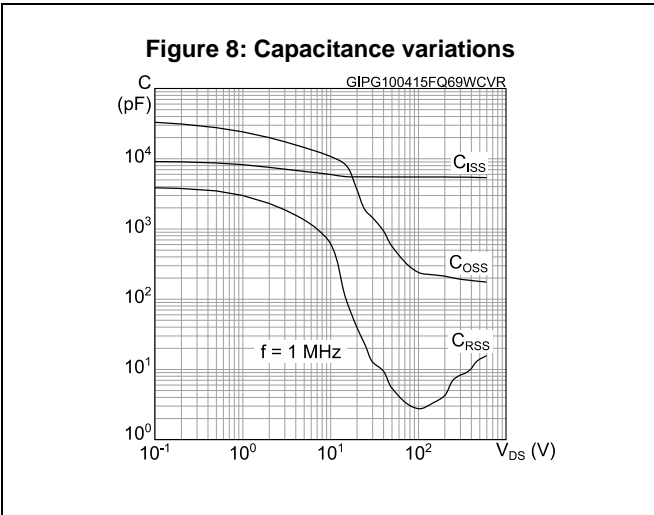
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		66	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		264	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 66\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 66\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 480\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	150		ns
Q_{rr}	Reverse recovery charge		-	0.75		μC
I_{RRM}	Reverse recovery current		-	10.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 66\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 480\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	250		ns
Q_{rr}	Reverse recovery charge		-	2.5		μC
I_{RRM}	Reverse recovery current		-	20.7		A

Notes:

- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

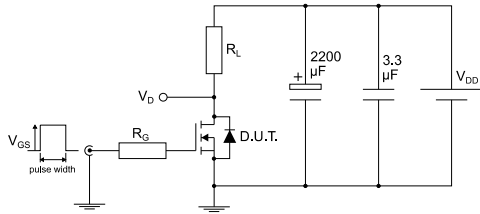
2.1 Electrical characteristics (curves)





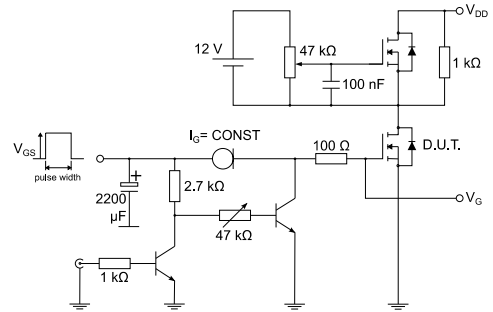
3 Test circuits

Figure 14: Test circuit for resistive load switching times



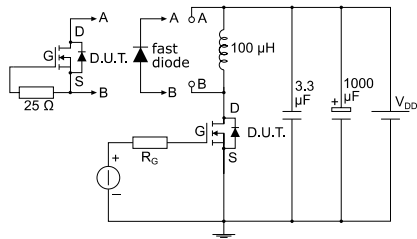
AM01468v1

Figure 15: Test circuit for gate charge behavior



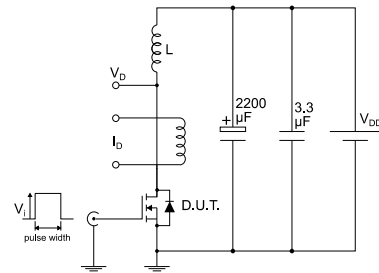
AM01469v1

Figure 16: Test circuit for inductive load switching and diode recovery times



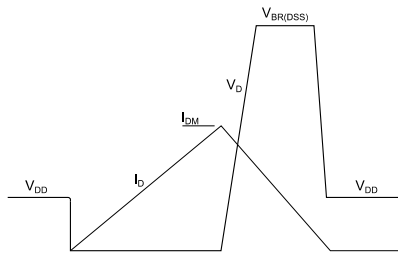
AM01470v1

Figure 17: Unclamped inductive load test circuit



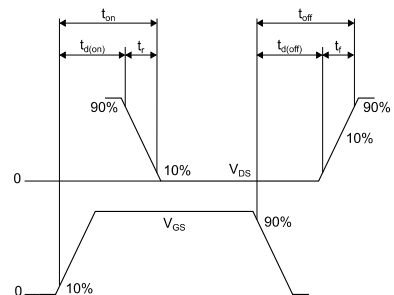
AM01471v1

Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

Table 9: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
27-Jan-2015	1	First release.
14-Apr-2015	2	Text edits and formatting changes throughout document Removed TO-247 long leads package data Added Section 2.1 Electrical characteristics (curves)
01-Jul-2015	3	Text edits and formatting changes throughout document On cover page: - updated title and features In Section Electrical ratings: - updated Table Absolute maximum ratings In Section Electrical characteristics: - updated Tables Static, Dynamic, Switching times and Source-drain diode Updated Section Electrical characteristics (curves)
09-Dec-2015	4	Updated Table 4: "Avalanche characteristics".
24-Oct-2016	5	Updated title and features in cover page. Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved