

General Description

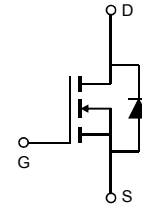
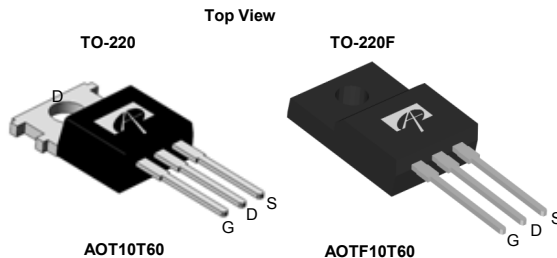
The AOT10T60 & AOTF10T60 are fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(ON)}$, C_{ISS} and C_{RSS} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:
 AOT10T60L & AOTF10T60L

Product Summary

$V_{DS} @ T_{j,max}$	700V
I_{DM}	40A
$R_{DS(ON),max}$	< 0.7 Ω
$Q_{g,typ}$	23nC
$E_{OSS} @ 400V$	3.4 μ J

100% UIS Tested
 100% R_g Tested


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	AOT10T60	AOTF10T60	AOTF10T60L	Units
Drain-Source Voltage	V_{DS}	600			V
Gate-Source Voltage	V_{GS}	± 30			V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	10	10*	10*
		$T_C=100^\circ\text{C}$	6.6	6.6*	6.6*
Pulsed Drain Current ^C	I_{DM}	40			A
Avalanche Current ^{C,J}	I_{AR}	10			A
Repetitive avalanche energy ^{C,J}	E_{AR}	50			mJ
Single pulsed avalanche energy ^G	E_{AS}	480			mJ
MOSFET dv/dt ruggedness	dv/dt	50			V/ns
Peak diode recovery dv/dt		5			
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	208	43	32
		Derate above 25 $^\circ\text{C}$	1.7	0.34	0.26
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150			$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300			$^\circ\text{C}$
Thermal Characteristics					
Parameter	Symbol	AOT10T60	AOTF10T60	AOTF10T60L	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	65	$^\circ\text{C}/\text{W}$
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	--	--	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	0.6	2.9	3.9	$^\circ\text{C}/\text{W}$

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	600			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		700		
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V		0.55		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V			1	μA
		V _{DS} =480V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3	4	5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5A		0.6	0.7	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =5A		9		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current				10	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C				40	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		1346		pF
C _{oss}	Output Capacitance				54	
C _{o(er)}	Effective output capacitance, energy related ^H	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz		40		pF
C _{o(tr)}	Effective output capacitance, time related ^I				72	
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		10		pF
R _g	Gate resistance	f=1MHz		3.8		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =10A		23	35	nC
Q _{gs}	Gate Source Charge			6.9		nC
Q _{gd}	Gate Drain Charge			6.7		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =300V, I _D =10A, R _G =25Ω		37		ns
t _r	Turn-On Rise Time			60		ns
t _{D(off)}	Turn-Off DelayTime			53		ns
t _f	Turn-Off Fall Time			35		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =10A, dI/dt=100A/μs, V _{DS} =100V		477		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =10A, dI/dt=100A/μs, V _{DS} =100V		6.7		μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=4A, V_{DD}=150V, R_G=25Ω, Starting T_J=25° C.

H. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

I. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. L=1.0mH, V_{DD}=150V, R_G=25Ω, Starting T_J=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

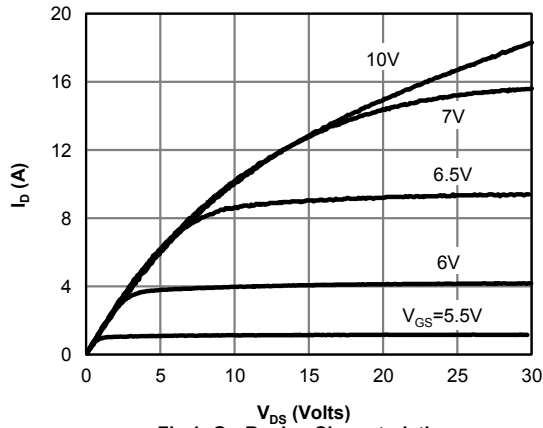


Fig 1: On-Region Characteristics

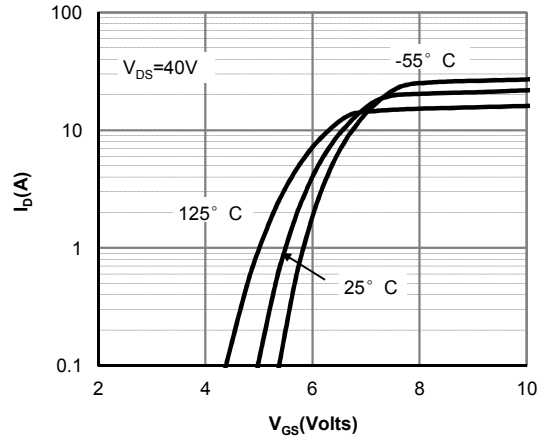


Figure 2: Transfer Characteristics

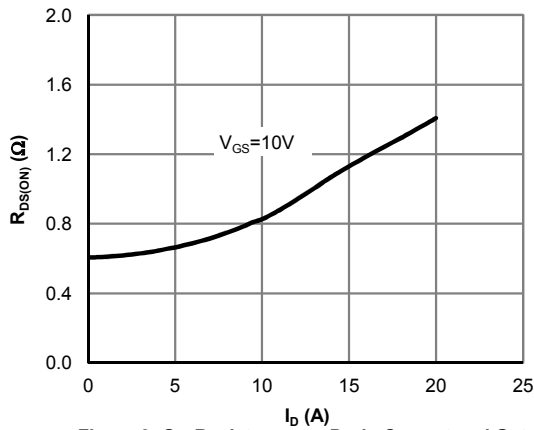


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

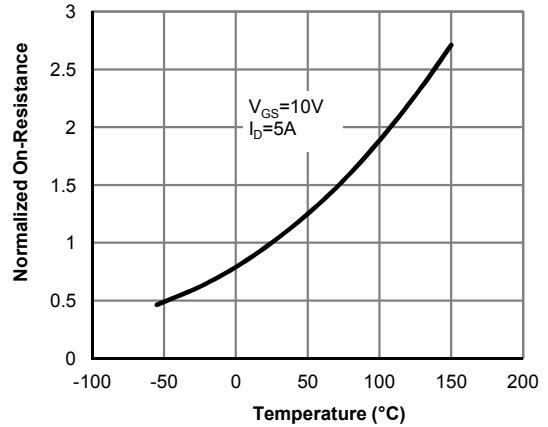


Figure 4: On-Resistance vs. Junction Temperature

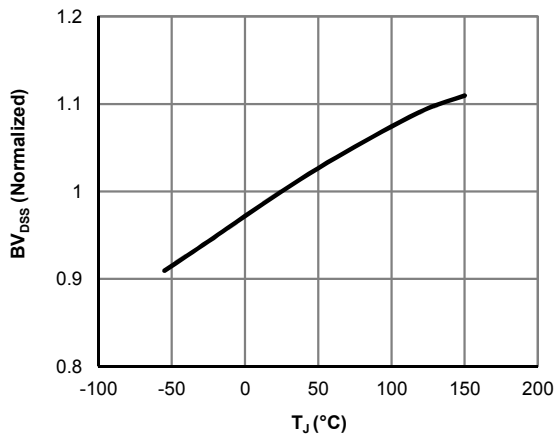


Figure 5: Break Down vs. Junction Temperature

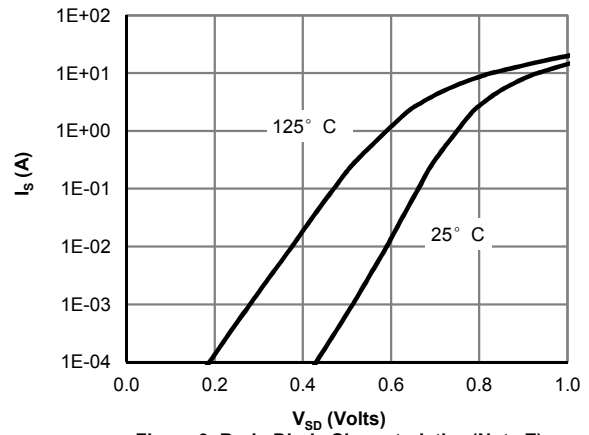


Figure 6: Body-Diode Characteristics (Note E)

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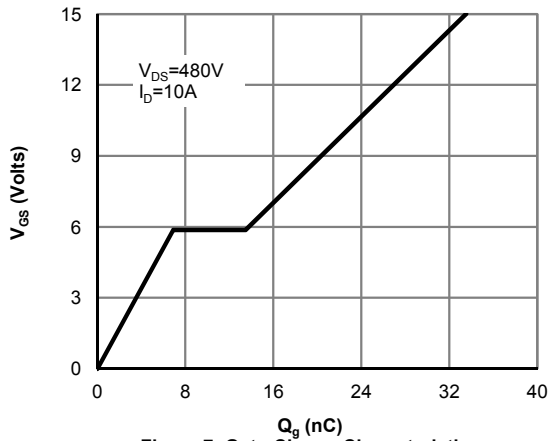


Figure 7: Gate-Charge Characteristics

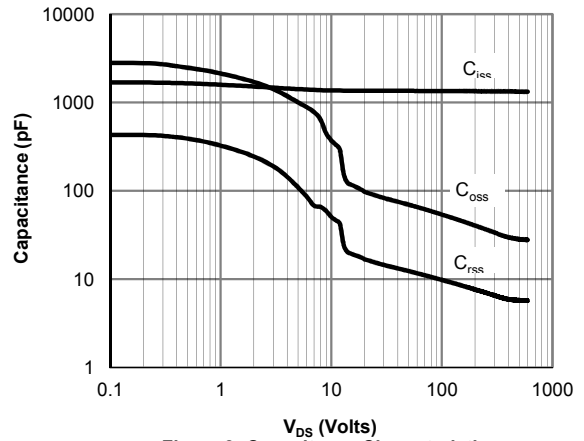


Figure 8: Capacitance Characteristics

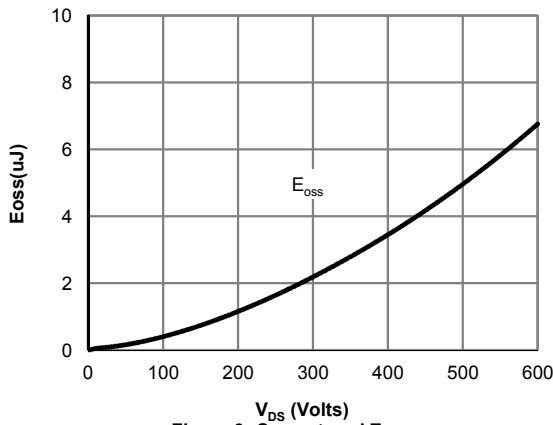


Figure 9: C_{oss} stored Energy

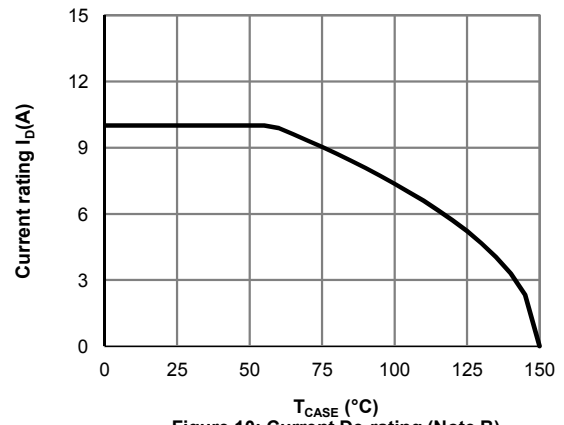


Figure 10: Current De-rating (Note B)

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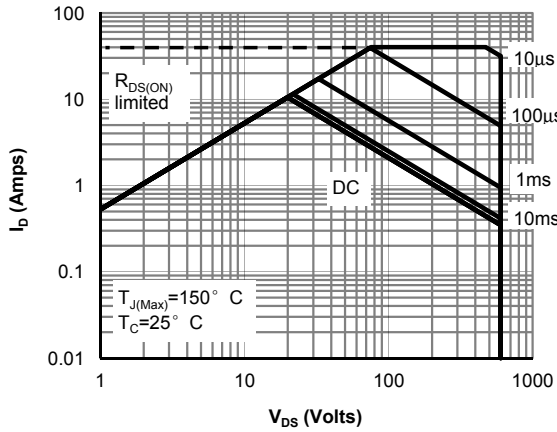


Figure 11: Maximum Forward Biased Safe Operating Area for AOT10T60 (Note F)

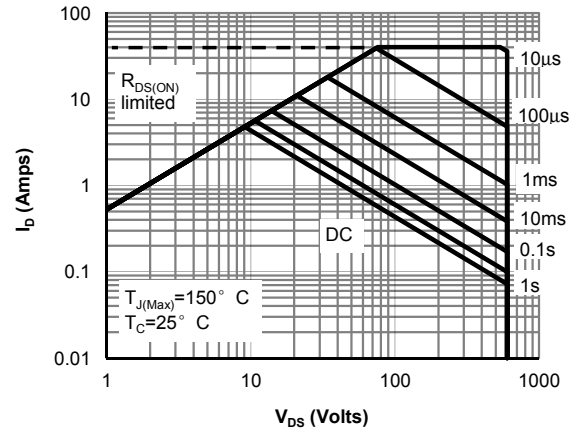


Figure 12: Maximum Forward Biased Safe Operating Area for AOTF10T60 (Note F)

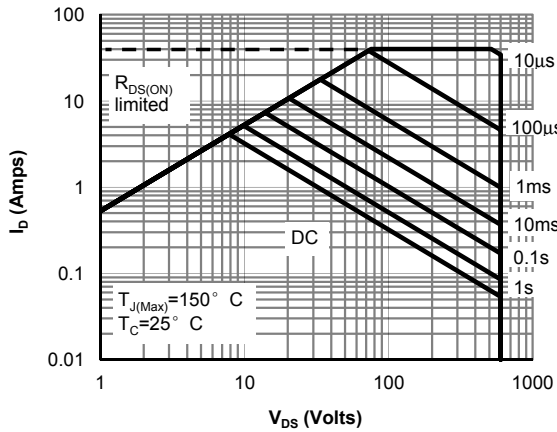


Figure 13: Maximum Forward Biased Safe Operating Area for AOTF10T60L (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

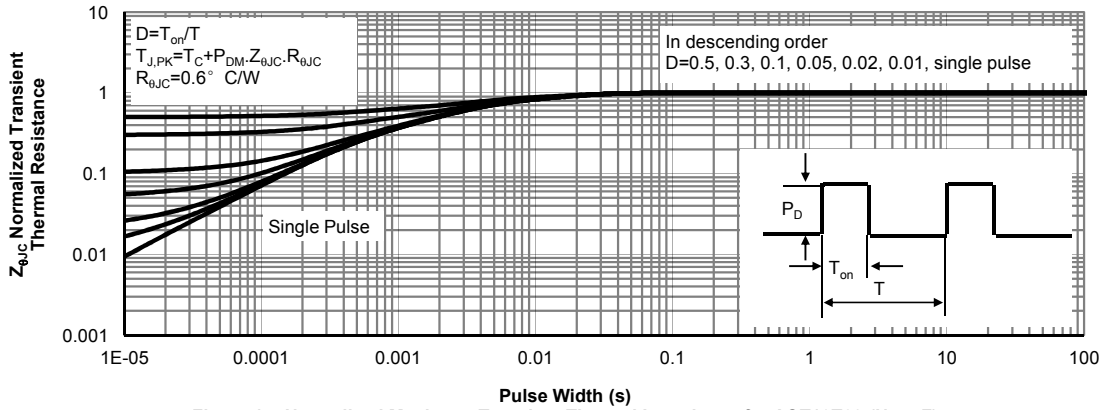


Figure 14: Normalized Maximum Transient Thermal Impedance for AOT10T60 (Note F)

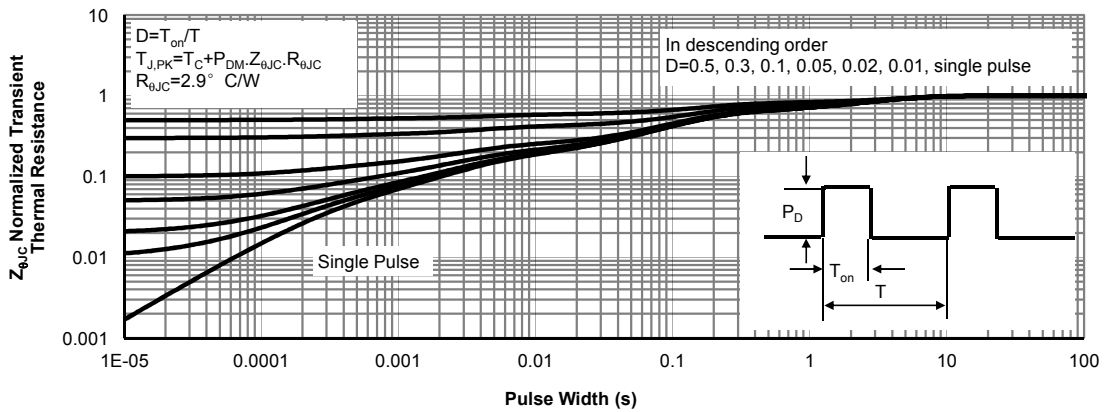


Figure 15: Normalized Maximum Transient Thermal Impedance for AOTF10T60 (Note F)

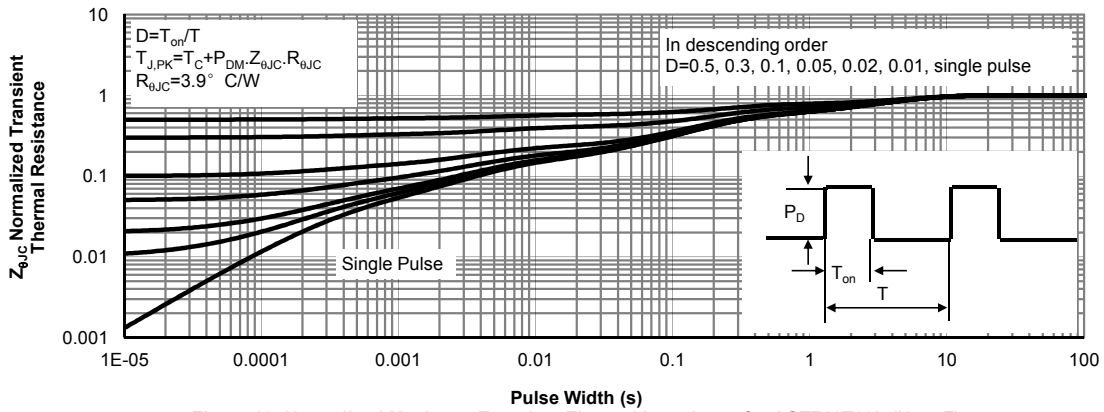
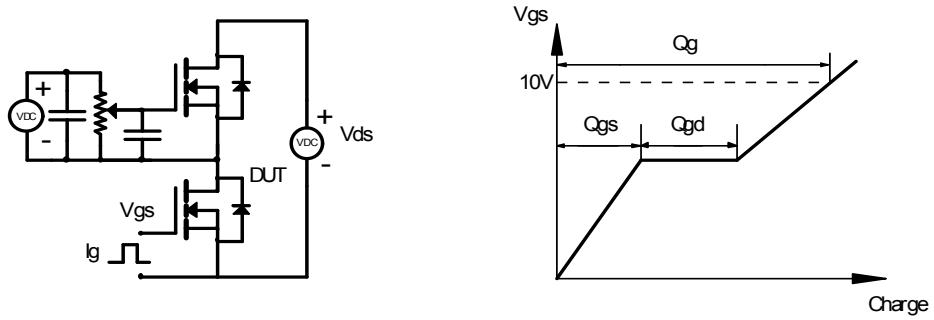
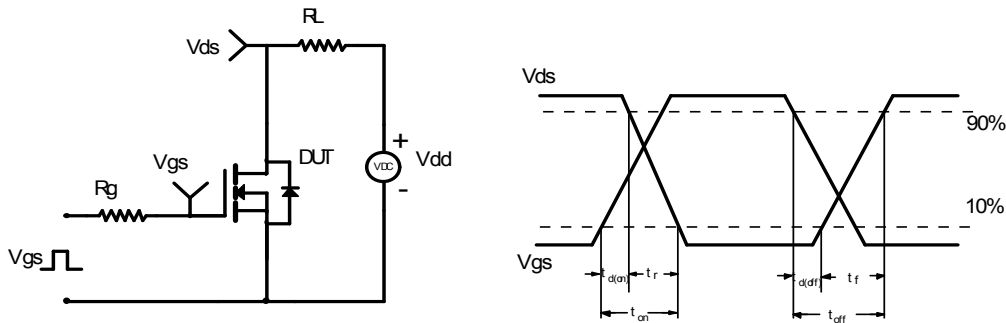


Figure 16: Normalized Maximum Transient Thermal Impedance for AOTF10T60L (Note F)

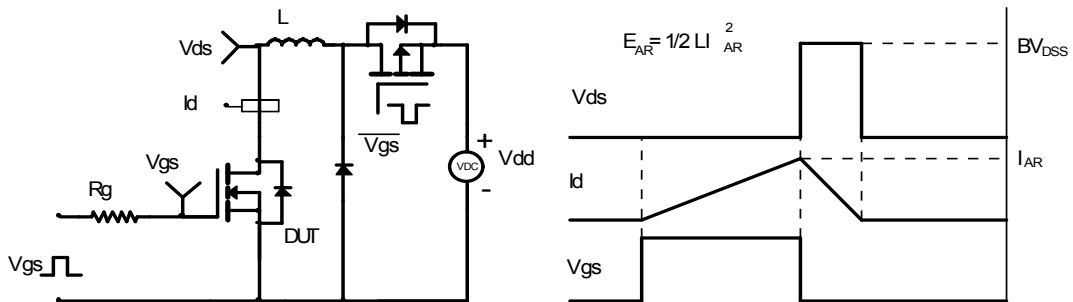
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

