# Lattice Diamond Design Software


Lattice Diamond design software offers leading-edge design and implementation tools optimized for cost sensitive, low-power Lattice FPGA architectures. Diamond is the next generation replacement for ispLEVER featuring design exploration, ease of use, improved design flow, and numerous other enhancements. The combination of new and enhanced features allows users to complete designs faster, easier, and with better results than ever before. See the **Lattice Diamond Versions** list for features introduced in each version of software.

## Diamond Software

Lattice Diamond is the new flagship logic design environment for Lattice FPGA products. Diamond is available as a download from the Lattice website for both Windows and Linux. Once downloaded and installed, it can be used with either a free license or a subscription license. Diamond software only needs to be downloaded and installed once.

### Diamond Software Free License

A **free license can be requested** from the Lattice website. This license provides access to many popular Lattice devices such as MachXO2, MachXO, and LatticeECP2 at no cost. It also includes Synopsys Synplify Pro for Lattice synthesis and Aldec Lattice Edition II mixed language simulation software.

### Diamond Software Subscription License

A **subscription license can be purchased** which adds support for all Lattice FPGAs including the latest LatticeECP3 devices. It includes Synopsys Synplify Pro for Lattice synthesis and Aldec Lattice Edition II mixed language simulator. The subscription license also enables both the new Diamond software and existing ispLEVER software from a single license.

## Powerful New Features

### Design Exploration Made Easy

**Projects / Implementations / Strategies**
Design projects in Diamond offer an order of magnitude increased functionality by allowing more robust projects and capabilities that allow design exploration. Key improvements to Diamond projects include the following:

- Allow the mixing of Verilog, VHDL, EDIF, and schematic sources
- Implementations, allow multiple versions of a design within a single project
- Strategies allow implementation “recipes” to be applied to any implementation within a project or shared between projects
- Manage and choose files for constraints, timing analysis, power calculation, and hardware debug
- Use Run Manager view to allow parallel processing of multiple implementations in order to explore design alternatives for the best results.

**Analyzing Your Design with HDL Code Checking**
Save time by analyzing your design prior to synthesis with the integrated HDL code checking capability.

**Synthesis Options for Exploring Results**
Lattice Diamond includes Synopsys Synplify Pro for all FPGA families. Additionally, for MachXO2 and MachXO device families the new Lattice Synthesis Engine (LSE) is also available for exploring how to achieve the best results. LSE is the result of several years of development initially focused on Lattice's internal FPGA architecture development. LSE supports both Verilog and VHDL languages and uses SDC format for constraints. It is integrated into the Lattice Diamond design software as a synthesis tool choice when a supported device family is selected.

### Ease of Use Throughout

**User Interface for a New Generation of Tools**
The Diamond user interface combines leading edge features and customization while offering better ease of use. All the tools in Diamond now open in “Views” integrated into a common Diamond user interface and have the ability to be detached in separate windows. Once the operation for a single tool view is learned, this knowledge can be applied to other views. New features like the Start Page and Reports view allow easy access to information.

**Speeding Common Functions**
ECO Editor provides quick access to commonly used netlist editing functions such as sysIO settings, PLL parameters, and memory initialization. With release 1.3, Programmer allows fast "normal" programming of single or multiple FPGAs within the Diamond User Interface and Reveal Analyzer is more than 10 times faster to download large trace data amounts and to configure complex trigger setups. Getting the job done more quickly is the goal of these tools

### More Efficient Design Flow

**Timing Analysis Easier and Faster**
The new Timing Analysis view offers an easy to use graphical environment for navigating timing information. A key new benefit in Timing Analysis view is rapidly updated analysis when timing constraints are changed, including clock jitter analysis. No longer must you re-implement your design to re-run a TRACE report.

**Easy Design Export to Simulators**
Diamond provides easy export of designs to simulators through the Simulation Wizard including support for multi-file testbenches.

**Scripting with TCL**
Diamond software adds capabilities for scripting the design flow. Diamond specific TCL command dictionaries are available for projects, netlists, HDL code checking, power calculation, and hardware debug insertion and analysis.

## Complete Design Environment

Diamond software is a robust and complete software environment from entering the design to programming your Lattice device. It uses proven implementation engine technology developed for six generations of tools. Diamond includes a complete set of tools covering all aspects of FPGA design.

- Design Entry
- Synthesis
- Implementation
- Analysis
- On-chip Debug Hardware Analysis
- Simulation
- Programming

## Powerful Third-Party Tools

### Synopsys Synplify® Pro for Lattice Synthesis

Lattice Diamond includes the industry-leading synthesis solution, Synopsys Synplify Pro for Lattice, with a range of tools and features that help you manage large designs, and extract the very best fit and performance, optimized for Lattice FPGAs. Synplify Pro for Lattice also includes HDL Analyst, which automatically produces an RTL schematic of your design for analysis and cross-probing with RTL source code. Other advanced features include mixed VHDL and Verilog synthesis support, compile points, automatic re-timing (balancing registers across combinatorial logic) for improved performance, and automatic gated-clock and generated clock conversion for efficient implementation of RTL written for an ASIC into an FPGA.

### Aldec Active-HDL® Simulation

Lattice Diamond includes the fast, comprehensive and feature-rich simulation environment Active-HDL Lattice Edition II from Aldec. Active-HDL Lattice Edition II features mixed language simulation of VHDL and Verilog, and many advanced verification and debug features such as Language Assistant, Code Execution Tracing, Advanced Breakpoint Management and Memory Viewing. Aldec Active-HDL Lattice Edition II is available on Windows platforms only.

## Learn More About Diamond

- Learn more about **Diamond New Features & Benefits**
- Learn more about **Diamond Key Concepts**
- Learn more about **Diamond Complete Feature List**
- Learn more about the **Diamond Videos**
- Learn everything available to download for **Diamond Software**

## Choosing The Right Software Tool

The following matrix summarizes some of the more important features of the current Lattice FPGA & logic design software tools. For current Lattice FPGA devices, Lattice Diamond is the recommended design software. For Lattice CPLD devices, ispLEVER Classic is the required design software.

| | **Lattice Diamond** (subscription license) Windows/Linux | **Lattice Diamond** (free license) Windows/Linux | **ispLEVER Classic** Windows |
|---|---|---|---|
| **Lattice FPGA/CPLD Support** | | | |
| LatticeECP3 | ✓ | | |
| LatticeECP2M/S | ✓ | | |
| LatticeECP2S | ✓ | | |
| LatticeSC/M | ✓ | | |
| MachXO2 | ✓ | ✓ | |
| MachXO | ✓ | ✓ | |
| LatticeXP2 | ✓ | ✓ | |
| LatticeECP2 | ✓ | ✓ | |
| LatticeECP & EC | ✓ | ✓ | |
| LatticeXP | ✓ | ✓ | |
| ispMACH 4000B/C/V/Z/ZE | | | ✓ |
| ispMACH 5000VG | | | ✓ |
| ispXPGA | | | ✓ |
| ORCA FPGA | | | ✓ |
| ORCA FPSC | | | ✓ |
| ispXPLD 5000MX | | | ✓ |

| | | | |
|---|---|---|---|
| MACH 4A3 / 4A5 | | | ✓ |
| ispLSI2000/5000 | | | ✓ |
| ispGDX/2 | | | ✓ |
| ispGAL / GAL | | | ✓ |
| **Software Features** | | | |
| Design Exploration | ✓ | ✓ | |
| Project Management | ✓ | ✓ | ✓ |
| VHDL & Verilog Support | ✓ | ✓ | ✓ |
| EDIF Support | ✓ | ✓ | ✓ |
| Schematic Support | ✓ | ✓ | ✓ |
| sysDSP Library for MATLAB/Simulink / ispLeverDSP | ✓ | ✓ | |
| ABEL | | | ✓ |
| Synopsys Synplify Pro for Lattice Synthesis | ✓ | ✓ | ✓ |
| Lattice Synthesis Engine (LSE) | MachXO2/MachXO only | MachXO2/MachXO only | |
| IP and Module configuration | ✓ | ✓ | Module Only |
| Power Estimation & Calculation | ✓ | ✓ | |
| Timing Analysis | ✓ | ✓ | ✓ |
| Integrated HDL Analysis | ✓ | ✓ | |
| Floorplanning | ✓ | ✓ | ✓ |
| EPIC Device Editor | ✓ | ✓ | ORCA FPGA only |
| Reveal Hardware Debugger | ✓ | ✓ | ispXPGA only |
| TCL Scripting Dictionaries | ✓ | ✓ | |
| Aldec Active-HDL Lattice Edition Simulation | Windows Only | Windows Only | |
| Aldec Active-HDL Lattice Web Edition Simulation | | | ✓ |
| **Operating Systems** | | | |
| Windows 7 (32-bit app, 32 & 64-bit OS) | ✓ | ✓ | ✓ |
| Windows XP, Vista (32-bit app, 32 & 64-bit OS) | ✓ | ✓ | ✓ |
| Linux (Redhat Enterprise v4, v5; Novell SUSE Enterprise v10 ) | ✓ | ✓ | |
| **Licensing & Updates** | | | |
| License Terms | 1 Year Subscription | 1 Year - Renewable | 1 Year - Renewable |

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|---|---|---|---|
| Node-Locked License | ✔ | ✔ | ✔ |
| Floating License | ✔ | | |

Note: Lattice Diamond subscription license allows either Diamond or the previous ispLEVER software to be run. Aldec simulation for Windows floating license requires a USB ID Key (ALDEC-USBKEY). Both of these products are available via the Lattice on-line store.