Si5040

10 Gbps XFP Transceiver

Description

The Si5040 is a high performance, protocol agnostic 10 Gbps XFP transceiver featuring integrated jitter attenuating capability based on Silicon Laboratories' proven DSPLL technology. The device is designed to perform reshaping, re-amplifying, and retiming of the bi-directional 10 Gbps serial data by integrating two independent Clock and Data Recoveries (CDRs), two DSPLL-based Clock Multiplier Units (CMUs), and data re-timers in both transmit and receive directions. The DSPLL-based CMU and the data re-timer in the transmit direction eliminate the need for external jitter clean up circuitry to achieve compliance with telecom and datacom jitter specifications. The same DSPLL technology minimizes jitter in the receive path ensuring error free operation with ASICs or FPGAs connected via the XFI interface. The Si5040 provides three receive signal quality monitors including analog loss-of-signal (LOS) detection, consecutive identical digit (CID) detection, and a proprietary digital measure of receive eye opening. Comprehensive diagnostics are also supported via two loop back modes as well as pattern generation and check capability on both the receive and transmit data paths. The Si5040 provides industry leading jitter performance for all telecom and datacom protocols between 9.9 and 11.4 Gbps, including OC-192/STM-64, 10 GbE, 10 G Fiber Channel, and their associated forward error correction (FEC) data rates:

- OC192/STM64: 9.95 Gbps
- 10 Gbps Ethernet LAN PHY: 10.3125 Gbps
- 10 Gbps Fibre Channel: 10.51875 Gbps
- G.709 OTU2: 10.709 Gbps
- 10 Gbps Ethernet + FEC: 11.0957 Gbps
- 10 Gbps Fibre Channel + FEC: 11.3176 Gbps

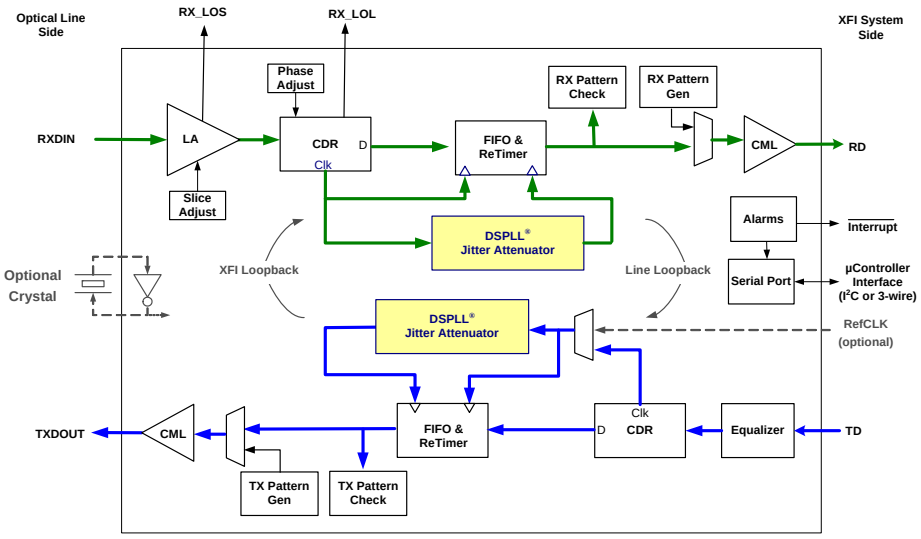
To address XFP module space and power constraints, the Si5040 comes in a 5 x 5 mm LGA package and only consumes 575 mW typ.

Summary of Key Features

- Continuous operation from 9.95 to 11.4 Gbps
- Transmit jitter attenuation with selectable loop bandwidths from 200 Hz to 1.2 MHz
- SONET jitter generation 2.5 mUI RMS
- SONET jitter tolerance > 0.55UIpp (0.15UIpp spec)
- Integrated limiting amplifier with high input sensitivity: 5 mV ppd Typ
- Auto-slice adjustment (programmable adjust optional)
- Programmable sample phase adjust
- Three signal quality monitors: loss-of-signal (LOS) detector, consecutive identical digit (CID) detector, and a receive eye opening monitor
- PRBS or user-defined pattern generation and checking in both TX and RX directions
- Operation over wide power supply variation (–10% to +5%)
- Industrial temperature operation (–40 to +85 °C)
- Adjustable output swing
- Low power: 575 mW (typ)
- Small size: 5 x 5 mm LGA
- Serial microcontroller interface

Applications

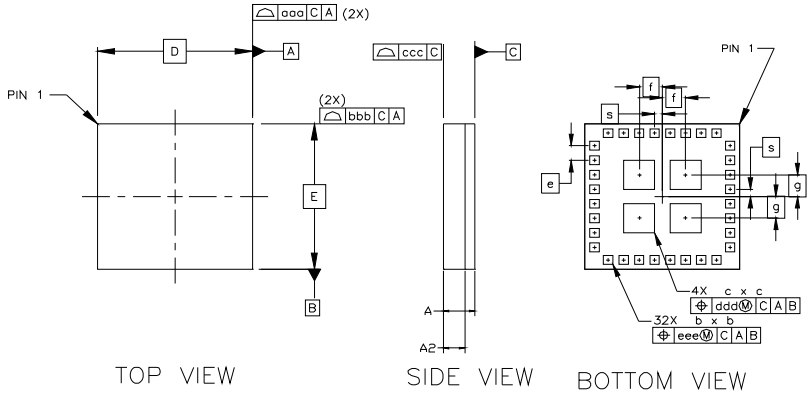
- XFP Optical Module
- Line card and Backplane
  - Regenerate 10 Gbps electrical signal for longer reach of the PCB trace
  - Added jitter attenuation with jitter transfer compliance
  - Added jitter tolerance
- CWDM
  - Complete regeneration of the 10 Gbps signal in O/E/O applications
- Optical Test Equipment
  - 10 Gbps Standalone Clock and Data Recovery
  - 10 Gbps Standalone Optical Transmitter



Selected Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Supply Voltage	V_{DD}		1.62	1.80	1.89	V
LVTTL I/O Supply Voltage	V_{DDIO}		1.62	—	3.63	V
Power Dissipation	P_D	VDD = 1.89 V VDDIO = 3.3 V	—	575	—	mW
Data Rate			9.90	9.95	11.4	Gbps
RXDIN						
Differential Input Swing	V_{ID}	At BER = 1E-12	8	—	1000	mV
Analog LOS Range			10	—	400	mV_{PPD}
Analog LOS Accuracy			1	—	—	
Consecutive Identical Digit Detection (CID) Range			0.5	—	100	uS
Consecutive Identical Digit Detection (CID) Accuracy			0.5	—	—	uS
Jitter Tolerance (OC-192 at BER = 1E-12)	$J_{TOL(PP)}$	F = 2.0 KHz	1.5	3.0	—	UI_{PP}
		F = 20 KHz	1.5	3.0	—	UI_{PP}
		F = 400 KHz	1.5	3.0	—	UI_{PP}
		F = 4 MHz	0.4	—	—	UI_{PP}
		F = 400 MHz	0.55	—	—	UI_{PP}
TXDOUT						
Random RMS Jitter Generation	$J_{GEN(RMS)}$	With PRBS31 at 50 kHz–80 MHz	—	2.5	—	mUI_{RMS}
Total Peak-to-Peak Jitter Generation	$J_{GEN(PP)}$	With PRBS31 at 50 kHz–80 MHz	—	20	—	mUI_{PP}
Jitter Transfer Bandwidth (Programmable)	J_{BM}		200	—	1.2 M	Hz
Input Reference Clock Frequency	RC_{FREQ}	Data Rate/16 or Data Rate/64	622 or 155	—	712.5 or 178.125	MHz

Package Information



Dimension	MIN (mm)	NOM (mm)	MAX (mm)
A	0.75	0.85	0.95
A2	0.48	0.53	0.58
b	0.25	0.30	0.35
c	0.92	1.00	1.08
D	5.00 BSC.		
e	0.50 BSC.		
E	5.00 BSC.		
f	0.735 BSC.		
g	0.735 BSC.		
s	0.25 BSC.		
aaa	--	--	0.10
bbb	--	--	0.10
ccc	--	--	0.10
ddd	--	--	0.10
eee	--	--	0.10